INTEGRATED CIRCUITS

BiCMOS
Bus Interface Logic

Data Handbook IC23
1998

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Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

BiCMOS Bus Interface Logic Data Handbook

5.0V – ABT, ABT16, MULTIBYTE™, PLD
3.3V – LVT, LVT16, ALVT, PLD, BTL, FBL, GTL
2.5V – ALVT

CONTENTS

DEFINITIONS

Data Sheet Identification	Product Status	Definition (Note)
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.
Short-form specification	—	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification

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NOTE: Always check with your local Philips Semiconductors Sales Office to be certain that you have the latest data sheet(s) before completing a design.

Preface

BiCMOS Bus Interface Logic

Philips Semiconductors Logic Products Group thanks you for continued interest in our BiCMOS product lines. This handbook contains specifications for many new high performance, low power products from Philips.

This handbook replaces and updates the 1996 BiCMOS Bus Interface Logic Data Handbook (IC23). Specifications for a wide range of high performance

BiCMOS 2.5V, 3.3V, 5V, BTL, and GTL level products are included in this manual including the fastest available 2.5V/3.3V family – ALVT; a new family of low voltage BTL transceivers; two new GTL compatible part types; and several new ALVT memory board address drivers, ALVT16344, ALVT16731, and ALVT16260.

Product families included in this handbook include ABT 8-bit(5V), ABT 16-bit(5V), MULTIBYTE(16-bit ABT in the QFP package), LVT 8-bit(3.3V), LVT 16-bit(3.3V), ALVT 16-bit (2.5V/3.3V), FBL (Low voltage BTL), GTL, and PLD products. The products utilize Philips patented QUBIC processes which are truly integrated and incorporate the best features of CMOS and Bipolar technology – very high speed, high output drive, excellent noise immunity, all combined in a wide range of space saving surface mounted packages.

Other support material available from your local distributor, sales office, or sales representative includes a comprehensive SPICE I/O Model Manual and IBIS Models on newer part types.

On-Line support includes a Fax-On-Demand toll free number 800–282–2000 in North America, and a Web Page for Logic Products at "www.philipslogic.com".

Our ongoing goal is to become your first choice for Logic Products.

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BiCMOS Bus Interface Logic

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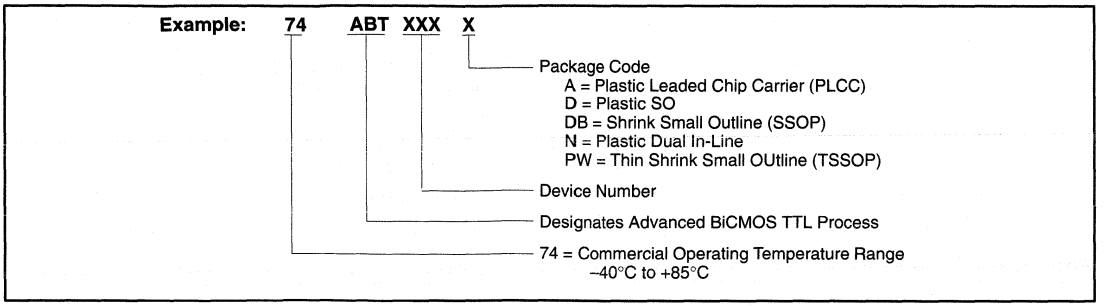
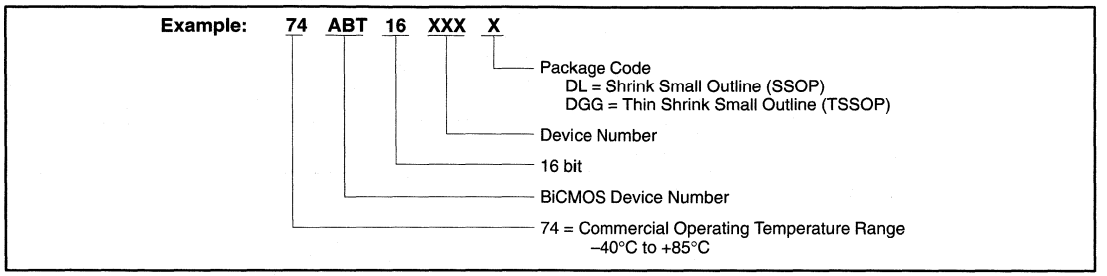
BiCMOS PRODUCTS – ABT



BiCMOS PRODUCTS – ABT16



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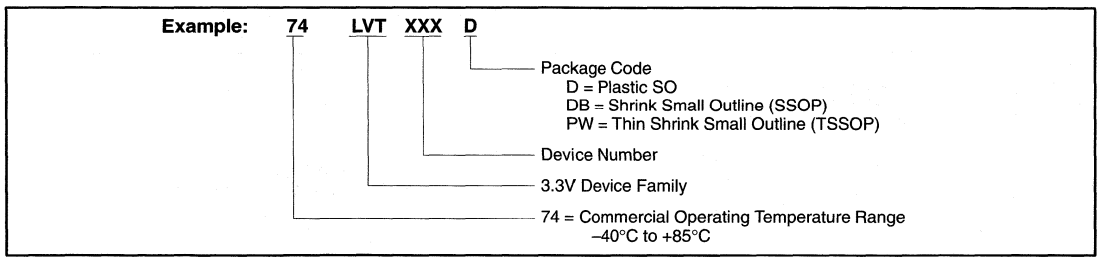
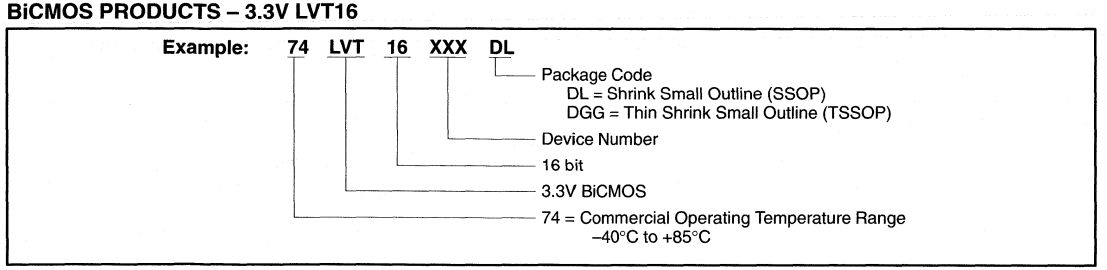


BiCMOS PRODUCTS – 3.3V LVT16



Ordering Information

BiCMOS PRODUCTS – 3.3V ALVT16

Example: 74 ALVT 16 XXX DL

- DL = Shrink Small Outline (SSOP); DGG = Thin Shrink Small Outline (TSSOP) — Package Code
- Device Number
- 16 bit
- Advanced 3.3V BiCMOS
- 74 = Commercial Operating Temperature Range –40°C to +85°C

MULTIBYTE™ PRODUCTS

Example: MB 2 XXX BB

- BB = Quad Flat Pack (QFP) — Package Code:
- Device Number
- Byte-width (2)
- Designates MULTIBYTE™ Product. Temperature Range: –40°C to +85°C

MULTIBYTE is a registered trademark of Philips Semiconductors.

LOW VOLTAGE BACKPLANE TRANSCEIVER

Example 4: FBL XXXX BB

- A = Plastic Leaded Chip Carrier (PLCC); BB = Quad Flat Pack (QFP) — Package Code:
- Device Number
- Designates Futurebus+ Product. Temperature Range: 0°C to +70°C

BiCMOS PRODUCTS – GTL

Example: 74 GTL 16 XXX DL

- DL = Shrink Small Outline (SSOP); DGG = Thin Shrink Small Outline (TSSOP) — Package Code
- Device Number
- 16 bit
- Gunning Transistor Logic
- 74 = Commercial Operating Temperature Range –40°C to +85°C

BiCMOS PRODUCTS – PLD

Example: XXX 22V10 Q K

- A = 28-lead Plastic Leaded Chip Carrier (PLCC); D = 24-pin Plastic Small Outline / Large (SO-L); N = 24-pin-600mil Plastic Dual In-Line — Package Designator
- Performance indicator = max t_{pd}
- Basic Part Number
- Philips Semiconductors Programmable Logic & Process or Architecture Indicator
  - ABT = High Speed 5V QUBiC/BiCMOS with Lateral Fuse
  - LVT = High Speed 3V QUBiC/BiCMOS with Lateral Fuse
- Operating temperature range = 0 to +70°C

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, components reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the product reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

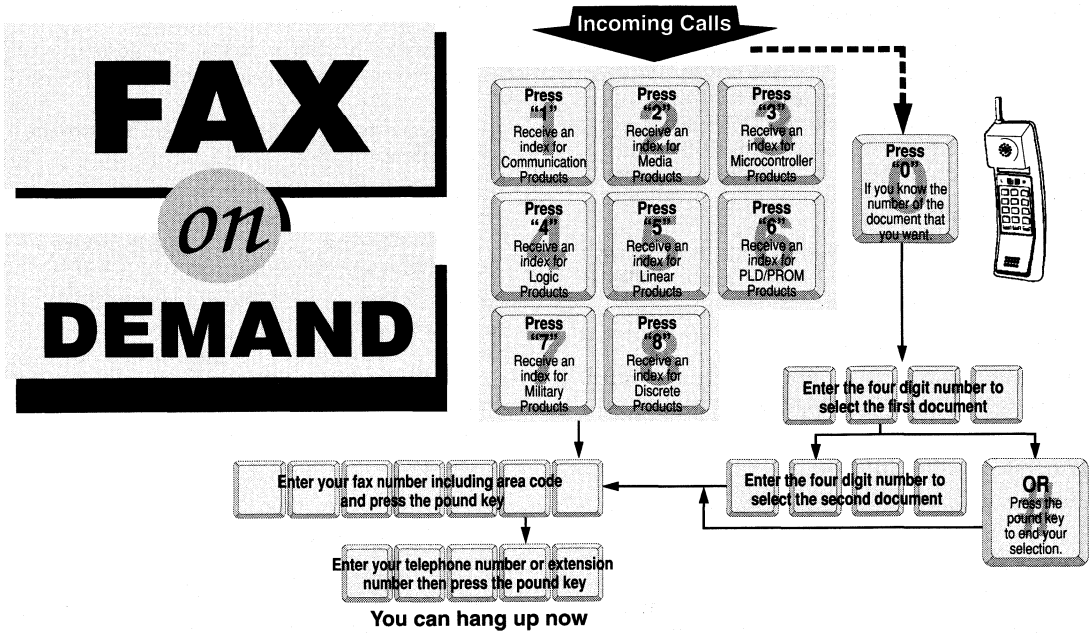
CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

FAX-on-DEMAND System / Internet WWW / Bulletin Board



What is it?

The FAX-on-DEMAND system is a computer facsimile system that allows customers to receive selected documents by fax automatically.

How does it work?

To order a document, you simply enter the document number. This number can be obtained by asking for an index of available documents to be faxed to you the first time you call the system.

Our system has a selection of the latest product data sheets from Philips with varying page counts. As you know, it takes approximately one minute to FAX one page. This isn't bad if the number of pages is less than 10. But if the document is 37 pages long, be ready for a long transmission!

Philips Semiconductors also maintains product information on the World-Wide Web. Our home page can be located at:
http://www.semiconductors.philips.com

Who do I contact if I have a question about FAX-on-DEMAND?

Contact your local Philips sales office.

FAX-on-DEMAND phone numbers:

United Kingdom, Ireland, Benelux & Scandinavia	+44-181-730-5020
North America	1-800-282-2000
Asia/Pacific (Australia, China/HK, India, Indonesia, Japan, Korea, Malaysia, New Zealand, Philippines, Singapore, Taiwan, and Thailand)	+852 2811 9990

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Philips Semiconductors World Wide Web:

http://www.semiconductors.philips.com *(click on LOGIC)*
or, http://www.philipslogic.com

BULLETIN BOARD access

To better serve our customers, Philips maintains a Bulletin Board. This computer Bulletin Board system features SPICE Model updates, a PSPICE demo, and a PLL design guide

The telephone number is:

+31 40 2721102
MAX 14,400 baud
Standards V32/V42/V42.bis/HST
(The Netherlands)

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor
- All mains-powered electrical equipment should be connected via an earth leakage switch
- Equipment cases should be earthed
- Relative humidity should be maintained between 50 and 65%
- An ionizer should be used to neutralize objects with immobile static charges

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

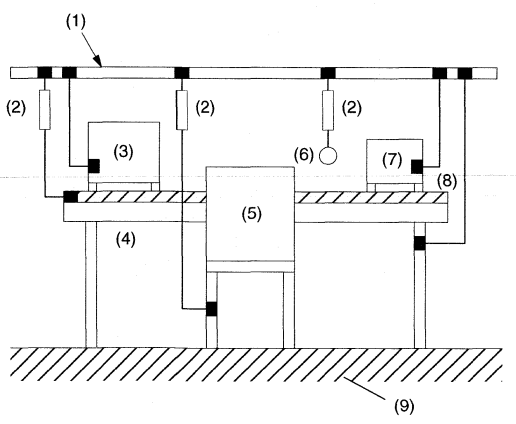
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time.
Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair
(6) Wrist strap.
(7) Electrical equipment.
(8), (9) Conductive surface/antistatic sheet.

Figure 1. Protected work station

Introduction to Advanced BiCMOS Logic Products

INTRODUCTION

A true BiCMOS process, such as QUBiC, gives an integrated circuit designer a great deal of freedom in approaching the optimum requirement goals of the systems designer. The input and output structures can be designed in such a way that they are optimum from a system standpoint. Noise characteristics such as ground bounce and EMI can be minimized without performance degradation. Speed can be maximized towards that of the fastest bipolar devices and power dissipation can be greatly reduced below even pure CMOS approaches.

QUBiC PROCESS

The QUBiC BiCMOS process from Philips Semiconductors is truly a major achievement in semiconductor technology. With equal emphasis on optimization of the CMOS as well as the bipolar devices, the process offers 13 GHz bipolar NPN devices, one micron NMOS devices, and one micron NMOS devices, altogether with three layers of Al/Cu interconnect. The devices are completely free of latch-up, have high ESD protection, show no electromigration, and, due to low bipolar reverse leakage currents and lightly doped CMOS drains, show extremely long reliability lifetimes. From an electrical performance standpoint, the results of this process are clear.

AC CHARACTERISTICS

Speed is almost always the first characteristic considered when choosing an integrated circuit. With bus frequencies constantly on the rise and the demand for greater data transfer rates continuously increasing, bus interface devices have become especially sensitive to speed. Figure 2 clearly shows the advantage of Philips Semiconductors Advanced BiCMOS interface devices.

Supply voltage and temperature stability is also an important feature of a product. Figure 1 shows the propagation delay versus change in the supply voltage and change in temperature. The temperature stability of devices is again a by-product of the process technology. A bipolar transistor generally becomes faster with increases in temperature and a CMOS transistor slows down with an increase in temperature. The effective addition of these two phenomena create the desirable feature in the figure. The flat slope of these curves essentially removes the variables of power supply and temperature from a designer's list of considerations. It also ensures that the device will be more resistant to unexpected system deviations from supply and temperature norms.

INPUT CHARACTERISTICS

The Advanced BiCMOS bus interface devices have TTL input input electrical levels, guaranteeing switching between 0.8V and 2.0V (typically 1.6V) in order to be driven by TTL or CMOS level buses. They have the desired CMOS characteristic of very low input current loading and input capacitance in the 3-4pF range. This feature ensures that the devices lightly load the buses they are interfacing to, allowing the devices to be driven from lower output current devices on a local bus, thus allowing higher system integration.

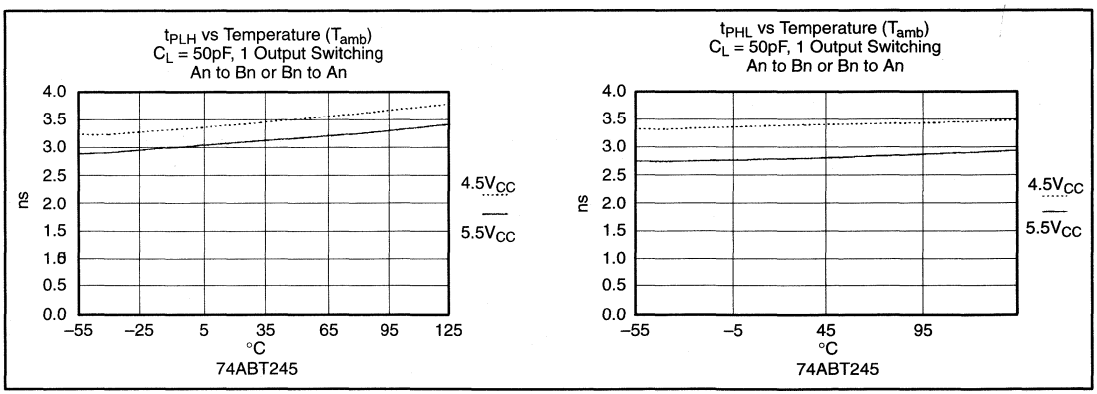


Figure 1. Propagation Delay

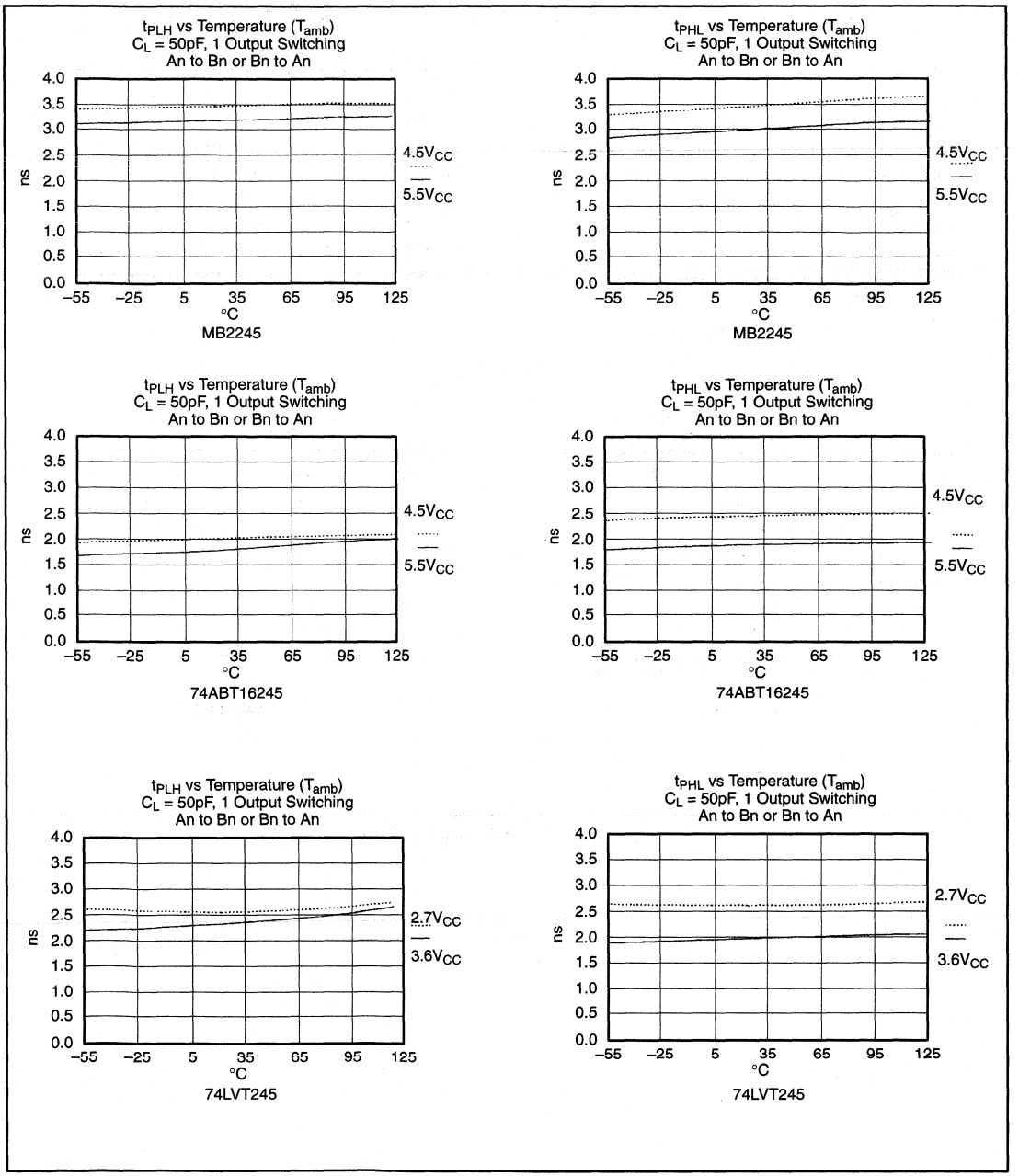


Figure 1. (Continued) Propagation Delay

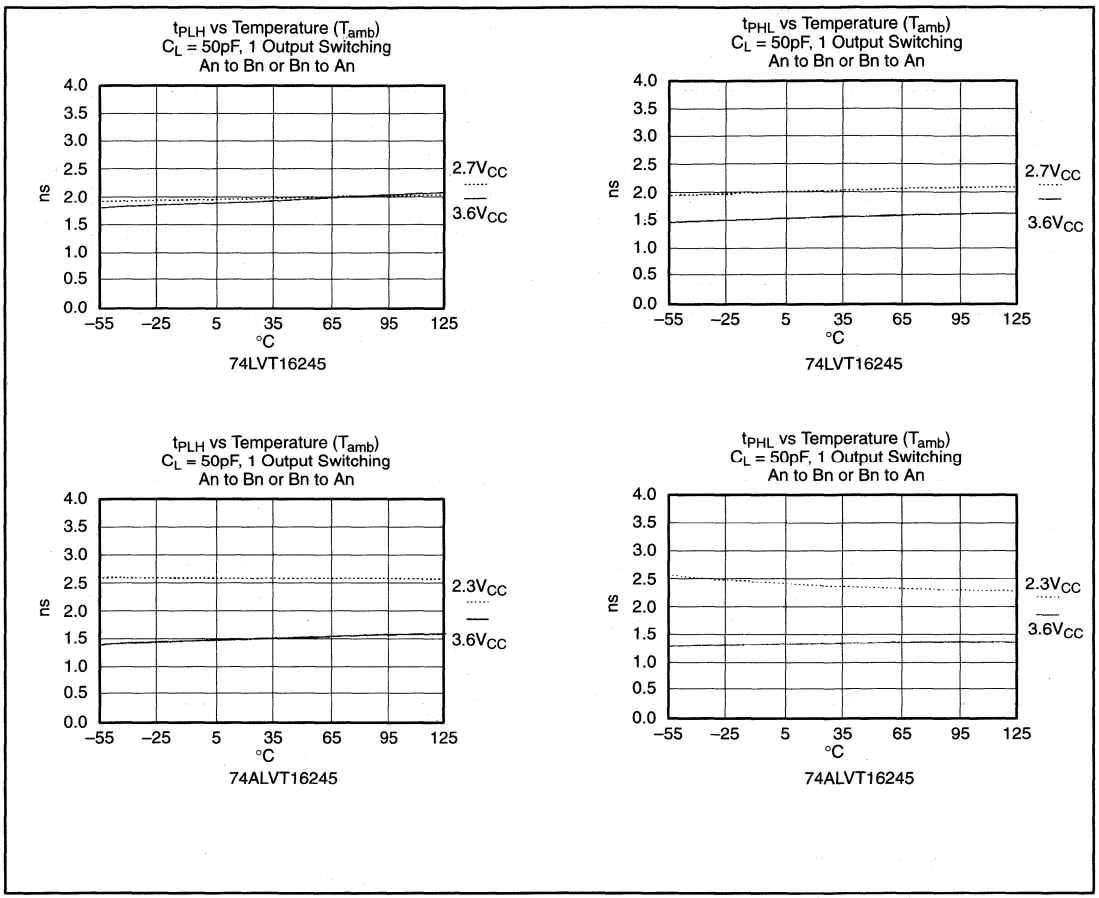
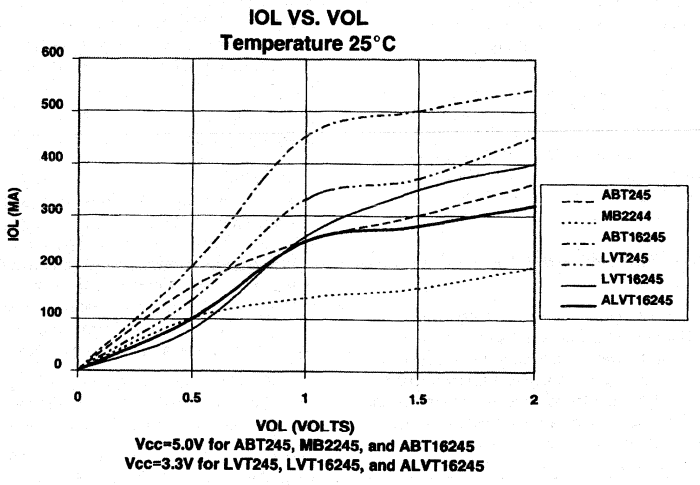


Figure 1. (Continued) Propagation Delay



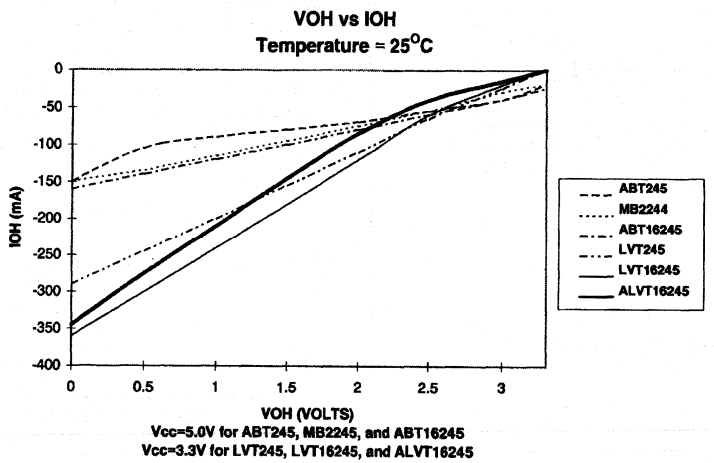


Figure 2. Voltage vs Current

OUTPUT CHARACTERISTICS

The BiCMOS interface devices have TTL output electrical levels, guaranteeing a V_{OL} of 0.55V while sinking 64mA and guaranteeing a V_{OH} level of 2.0V while sourcing 32mA. Unlike a pure bipolar output structure, these outputs will effectively "turn-off" when the output is in the High state or the disabled state and will not contribute to I_{CC}. This causes I_{CCH} and I_{CCZ} values to be very small (μA). When the output is in the Low state, the device will show some I_{CCL} but this value is less than most equivalent bipolar devices by a factor of three to four.

In order to effectively drive heavily loaded local bus applications or almost all backplane or system bus applications, high output current drivers are required. The Philips Semiconductors Advanced BiCMOS devices provide as standard 64mA I_{OL}, enough current for nearly all bus driving applications. Figure 2 shows the output current versus voltage characteristics for Philips Semiconductors Advanced BiCMOS devices. This clearly shows the ability of the output to source and sink large amounts of current to and from the bus to which it is interfaced.

Advanced BiCMOS features

Advanced BiCMOS Features

With the advent of the newer BiCMOS and 3 volt technologies, product feature sets have been enhanced from the standard features found in previous logic families. With the newer technologies came capabilities of hot plugging and operating in mixed voltage systems just to name a couple. Special features and device parameters exist for these newer families such as Power-up 3-State, Power-up Reset, Bus Hold, Input Disable, and 5 volt tolerant I/O's in addition to existing parameters. Following is a summary of these features and their associated data sheet parameters. Tables on following pages show which features are available for the various part types.

Live Insertion Capability and Power-up/Down 3-State

Glitches or signal degradation can occur on an active bus when circuit boards are plugged into or extracted from a powered up system or when a power-up and down cycle is used during system maintenance. Signal degradation is kept to a minimum by keeping the outputs of devices in the high impedance state where the current is very low. The advanced BiCMOS logic families employ a power-up and power-down 3-State circuit that facilitates live insertion up to 1.2 V V_{CC} or 2.1 V V_{CC} as shown in Figure 1.

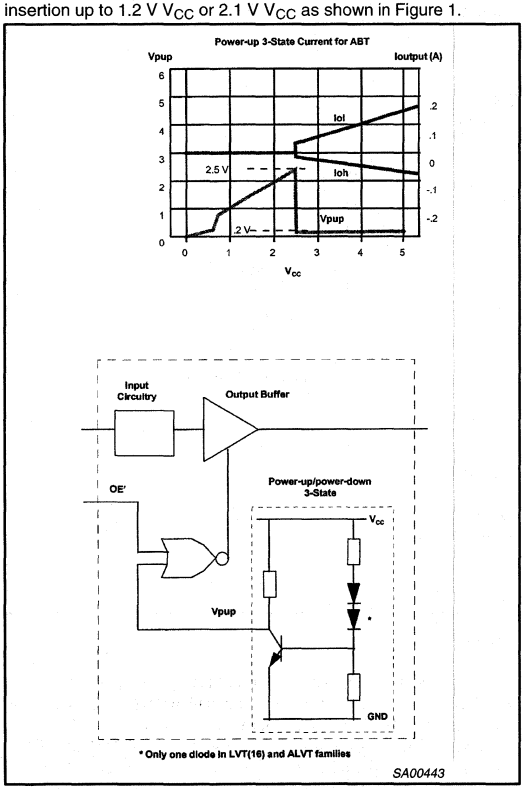


Figure 1. Power-up/power-down 3-State circuit and output 3-State current

During V_{CC} ramp up or ramp down, the outputs are guaranteed to remain 3-State up to 2.1 V for ABT and MULTIBYTE™ families and 1.2 V for LVT(16) and ALVT families, regardless of the voltage level of the data or enable input pins. Output leakage current is limited to ±100 µA depending on the product family. Refer to the I_{PU}/I_{PD} specification in the data sheet.

Live insertion capability is available on most of the 3-State bus interface functions.

Bus Hold

Used or unused CMOS device inputs should not be left floating. Floating inputs can cause extra current to flow through the input structure, causing extra wasted power dissipation, or they can cause high frequency oscillations, generating heat that may eventually damage the part. A common solution for this is to connect the input to V_{CC} or ground through a pull-up or pull-down resistor. The disadvantage of this is an extra component is needed as well as extra board space, and the resistor dissipates extra power.

The ABT16 and low voltage BiCMOS logic families use an integrated bus hold circuit which eliminates the need for external resistors and saves board space. The circuit is shown in Figure 2.

The bus hold circuit holds the last known valid state of the input when the bus starts to float. There is a minimum hold current (I_{HOLD}) of 75 µA at the input switching levels of 2.0 V and 0.8 V. An overdrive current of +450 µA/–450 µA is required to toggle the bus hold cell into the LOW or HIGH state. The circuit has minimal impact to input/output capacitance and is about 0.5 pF. This adds a slight increase to the driver's propagation delay of about 40 ps for 8 mA drivers and about 15 ps for 24 mA drivers per each bus hold input. For further reference, please refer to Application Note 2022, *The Behavior of Integrated Bus Hold Circuits*, document number 9397–750–00798.

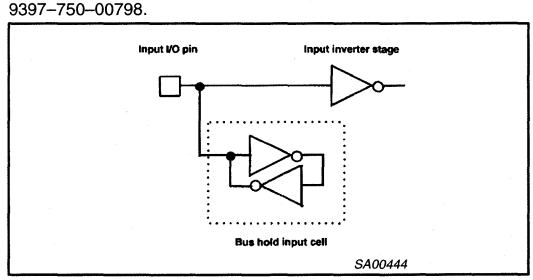


Figure 2. Integrated bus hold circuit

Input Disable Circuit

ABT and MULTIBYTE™ products provide a solution for floating CMOS inputs different from the bus hold solution. They employ a feature called Input Disable which disables the input structure whenever the output is in the 3-State condition. When disabled, no current flows through the input structure from V_{CC} to ground. This allows inputs to float without the need for an input pull-up or pull-down resistor to V_{CC} or ground. This feature is included only on buffers and transceivers and not on parts with latches or flip-flops.

Power-up Reset

The Power-up Reset feature is found in parts with latches or flip-flops. This feature ensures that the output is in the logic LOW state after power-up. This provides a known valid state after power-up and eliminates any need for a reset cycle. The guaranteed V_{OL} voltage (V_{RST}) is 0.55 V.

I_{OFF}

I_{OFF} is the power-off leakage current on the input or output when V_{CC} is 0 V. The current is limited to 100 µA or less, depending on the product family, and the feature helps support applications that have a suspend or power-down mode.

5 V Tolerant I/O's

With the trend of 3.3 V and lower processors, memories, and ASIC's comes the need for devices to operate in mixed voltage systems. Current systems often use a mix of 3 V and 5 V components besides using only pure 5 V or pure 3 V components. This requires a 3 V device's input and output pins to be able to reliably tolerate 5 V signals as well as 3 V signals. Pure bipolar structures have no problem with this, however, parts with classic CMOS input and output structures have diodes—thus a current path—to VCC, thereby not allowing 5 V signals.

The 3 V BiCMOS logic families use designs that allow 5 V signals on inputs and outputs shown in Figures 3 and 4.

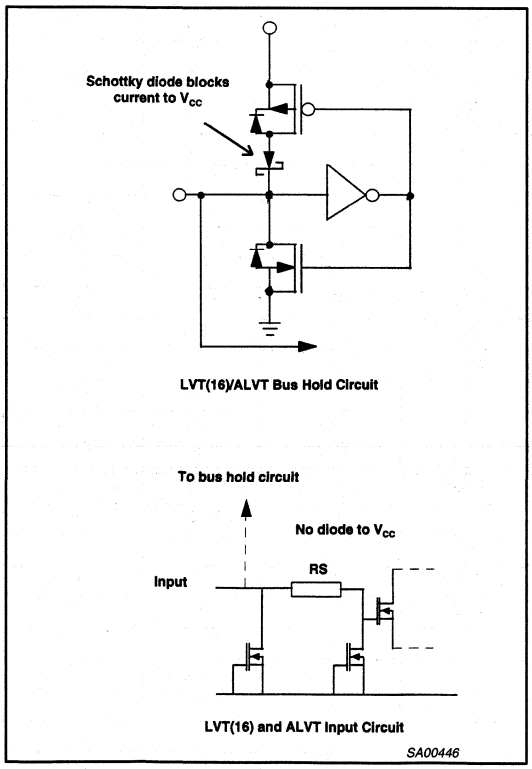


Figure 3. 5 V tolerant input circuits

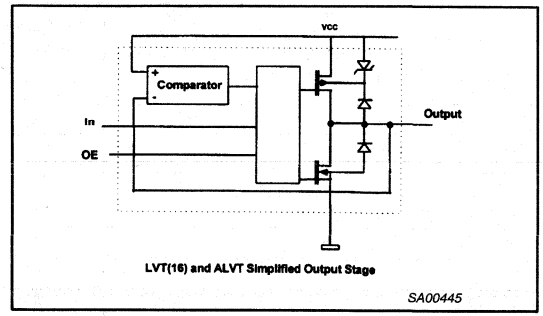


Figure 4. 5 V tolerant output circuit

The comparator turns off and protects the LVT and ALVT upper PMOS transistor in the active HIGH state when the output is 0.5 V greater than V_{CC}. The output current (I_{EX}) is limited to 125 µA. In the 3-State mode, the reversed biased Schottky diode prevents current flow to the 3.3 V supply if a 5 V signal is applied to the output. For further reference, please refer to Application Note 240, *Interfacing 3V and 5V Systems*, document number 9397–750–00282.

Advanced BiCMOS features

PRODUCT	INPUT DISABLE CIRCUIT	LIVE INSERTION CAPABILITY	POWER-UP RESET	SPLIT-LEAD GROUND	INPUT BUS HOLD CIRCUIT	64 mA OUTPUT DRIVE	5-VOLT COMPATIBLE I/O
74ABT00	NO	NO	NO	NO	NO	NO	YES
74ABT02	NO	NO	NO	NO	NO	NO	YES
74ABT04	NO	NO	NO	NO	NO	NO	YES
74ABT08	NO	NO	NO	NO	NO	NO	YES
74ABT10	NO	NO	NO	NO	NO	NO	YES
74ABT20	NO	NO	NO	NO	NO	NO	YES
74ABT32	NO	NO	NO	NO	NO	NO	YES
74ABT74	NO	NO	NO	NO	NO	NO	YES
74ABT125	YES	YES	NO	YES	NO	YES	YES
74ABT126	YES	YES	NO	YES	NO	YES	YES
74ABT240	NO	YES	NO	YES	NO	YES	YES
74ABT2240	NO	YES	NO	YES	NO	NO	YES
74ABT241	YES	YES	NO	YES	NO	YES	YES
74ABT2241	YES	YES	NO	YES	NO	NO	YES
74ABT244	YES	YES	NO	YES	NO	YES	YES
74ABT2244	YES	YES	NO	YES	NO	NO	YES
74ABT245	YES	YES	NO	YES	NO	YES	YES
74ABT2245	YES	YES	NO	YES	NO	NO	YES
74ABT273A	NO	NO	YES	YES	NO	YES	YES
74ABT373A	NO	YES	YES	YES	NO	YES	YES
74ABT374A	NO	YES	YES	YES	NO	YES	YES
74ABT377A	NO	NO	YES	YES	NO	YES	YES
74ABT534A	NO	YES	YES	YES	NO	YES	YES
74ABT540	NO	YES	NO	YES	NO	YES	YES
74ABT541	YES	YES	NO	YES	NO	YES	YES
74ABT543A	NO	YES	YES	YES	NO	YES	YES
74ABT544	NO	YES	YES	NO	NO	YES	YES
74ABT573A	NO	YES	YES	YES	NO	YES	YES
74ABT574A	NO	YES	YES	YES	NO	YES	YES
74ABT620	NO	YES	NO	YES	NO	YES	YES
74ABT623	YES	YES	NO	YES	NO	YES	YES
74ABT640	NO	YES	NO	YES	NO	YES	YES
74ABT646A	NO	YES	YES	YES	NO	YES	YES
74ABT648	NO	YES	YES	NO	NO	YES	YES
74ABT651	NO	YES	YES	YES	NO	YES	YES
74ABT652A	NO	YES	YES	YES	NO	YES	YES
74ABT657	YES[2]	NO	NO	NO[3]	NO	YES	YES
74ABT821	NO	NO	NO	YES	NO	YES	YES
74ABT823	NO	NO	NO	YES	NO	YES	YES
74ABT827	YES	NO	NO	YES	NO	YES	YES
74ABT833	NO	YES	NO	YES	NO	YES	YES
74ABT841	NO	NO	NO	YES	NO	YES	YES

Advanced BiCMOS features

PRODUCT	INPUT DISABLE CIRCUIT	LIVE INSERTION CAPABILITY	POWER-UP RESET	SPLIT-LEAD GROUND	INPUT BUS HOLD CIRCUIT	64 mA OUTPUT DRIVE	5-VOLT COMPATIBLE I/O
74ABT845	NO	NO	NO	YES	NO	YES	YES
74ABT853	NO	YES	NO	YES	NO	YES	YES
74ABT861	YES	NO	NO	YES	NO	YES	YES
74ABT863	YES	YES	NO	NO	NO	YES	YES
74ABT899	NO	YES	YES	YES	NO	YES	YES
74ABT2952	NO	YES	YES	YES	NO	YES	YES
74ABT2953	NO	YES	YES	NO	NO	YES	YES
74ABT5074	NO	NO	NO	NO	NO	NO	YES
74ABTH16240A	NO	YES	NO	NO[3]	YES	YES	YES
74ABTH162240	NO	YES	NO	NO[3]	YES	NO	YES
74ABTH16241A	NO	YES	NO	NO[3]	YES	YES	YES
74ABTH16244A	NO	YES	NO	NO[3]	YES	YES	YES
74ABTH162244	NO	YES	NO	NO[3]	YES	NO	YES
74ABTH16245B	NO	YES	NO	NO[3]	YES	YES	YES
74ABTH162245A	NO	YES	NO	NO[3]	YES	NO	YES
74ABTH16260	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16273	NO	NO	YES	NO[3]	YES	YES	YES
74ABTH16373B	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16374B	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16500C	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16501A	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16541	NO	YES	NO	NO[3]	YES	YES	YES
74ABTH16543	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH161543	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16646	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16652	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16821A	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16823A	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16825A	NO	YES	NO	NO[3]	YES	YES	YES
74ABTH16827A	NO	YES	NO	NO[3]	YES	YES	YES
74ABTH162827A	NO	YES	NO	NO[3]	YES	NO	YES
74ABTH16841A	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16899	NO	YES	YES	NO[3]	YES	YES	YES
74ABTH16952	NO	YES	YES	NO[3]	YES	YES	YES
74ABT16240A	NO	YES	NO	NO[3]	NO	YES	YES
74ABT162240	NO	YES	NO	NO[3]	NO	YES	YES
74ABT16241A	NO	YES	NO	NO[3]	NO	YES	YES
74ABT16244A	YES	YES	NO	NO[3]	NO	YES	YES
74ABT162244	YES	YES	NO	NO[3]	NO	YES	YES
74ABT16245B	YES	YES	NO	NO[3]	NO	YES	YES
74ABT162245A	YES	YES	NO	NO[3]	NO	YES	YES
74ABT16260	NO	YES	YES	NO[3]	NO	YES	YES

Advanced BiCMOS features

PRODUCT	INPUT DISABLE CIRCUIT	LIVE INSERTION CAPABILITY	POWER-UP RESET	SPLIT-LEAD GROUND	INPUT BUS HOLD CIRCUIT	64 mA OUTPUT DRIVE	5-VOLT COMPATIBLE I/O
74ABT16273	NO	NO	YES	NO[3]	NO	YES	YES
74ABT16373B	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16374B	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16500C	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16501A	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16541	NO	YES	NO	NO[3]	NO	YES	YES
74ABT16543	NO	YES	YES	NO[3]	NO	YES	YES
74ABT161543	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16646	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16652	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16821A	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16823A	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16825A	NO	YES	NO	NO[3]	NO	YES	YES
74ABT16827A	NO	YES	NO	NO[3]	NO	YES	YES
74ABT162827A	NO	YES	NO	NO[3]	NO	NO	YES
74ABT16841A	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16899	NO	YES	YES	NO[3]	NO	YES	YES
74ABT16952	NO	YES	YES	NO[3]	NO	YES	YES
MB2052	NO	YES	YES	NO[3]	NO	YES	YES
MB2240	NO	YES	NO	NO[3]	NO	YES	YES
MB2241	YES	YES	NO	NO[3]	NO	YES	YES
MB2244	YES	YES	NO	NO[3]	NO	YES	YES
MB2245	YES	YES	NO	NO[3]	NO	YES	YES
MB2373	NO	YES	YES	NO[3]	NO	YES	YES
MB2374	NO	YES	YES	NO[3]	NO	YES	YES
MB2377	NO	NO	YES	NO[3]	NO	YES	YES
MB2541	YES	YES	NO	NO[3]	NO	YES	YES
MB2543	NO	YES	YES	NO[3]	NO	YES	YES
MB2623	YES	YES	NO	NO[3]	NO	YES	YES
MB2646	NO	YES	YES	NO[3]	NO	YES	YES
MB2652	NO	YES	YES	NO[3]	NO	YES	YES
MB2821	NO	YES	YES	NO[3]	NO	YES	YES
MB2823	NO	YES	YES	NO[3]	NO	YES	YES
MB2827	NO	YES	NO	NO[3]	NO	YES	YES
MB2841	NO	YES	YES	NO[3]	NO	YES	YES
MB2861	NO	YES	NO	NO[3]	NO	YES	YES
74LVT00	NO	NO	NO	NO	NO	NO	YES
74LVT02	NO	NO	NO	NO	NO	NO	YES
74LVT04	NO	NO	NO	NO	NO	NO	YES
74LVT08	NO	NO	NO	NO	NO	NO	YES
74LVT10	NO	NO	NO	NO	NO	NO	YES
74LVT14	NO	NO	NO	NO	NO	NO	YES

Advanced BiCMOS features

PRODUCT	INPUT DISABLE CIRCUIT	LIVE INSERTION CAPABILITY	POWER-UP RESET	SPLIT-LEAD GROUND	INPUT BUS HOLD CIRCUIT	64 mA OUTPUT DRIVE	5-VOLT COMPATIBLE I/O
74LVT20	NO	NO	NO	NO	NO	NO	YES
74LVT32	NO	NO	NO	NO	NO	NO	YES
74LVT74	NO	NO	NO	NO	NO	NO	YES
74LVT86	NO	NO	NO	NO	NO	NO	YES
74LVT125	NO	YES	NO	YES	YES	YES	YES
74LVT126	NO	YES	NO	YES	YES	YES	YES
74LVT240	NO	YES	NO	YES	YES	YES	YES
74LVT241	NO	YES	NO	YES	YES	YES	YES
74LVT2241	NO	YES	NO	YES	YES	YES	YES
74LVT244A	NO	YES	NO	YES	YES	YES	YES
74LVT2244	NO	YES	NO	YES	YES	NO	YES
74LVT245	NO	YES	NO	YES	YES	YES	YES
74LVT2245	NO	YES	NO	YES	YES	NO	YES
74LVT273	NO	NO	YES	YES	YES	YES	YES
74LVT374	NO	YES	YES	YES	YES	YES	YES
74LVT534	NO	YES	YES	YES	YES	YES	YES
74LVT543	NO	YES	YES	YES	YES	YES	YES
74LVT573	NO	YES	YES	YES	YES	YES	YES
74LVT574	NO	YES	YES	YES	YES	YES	YES
74LVT623	NO	YES	NO	YES	YES	YES	YES
74LVT640	NO	YES	NO	YES	YES	YES	YES
74LVT646	NO	YES	YES	YES	YES	YES	YES
74LVT652	NO	YES	YES	YES	YES	YES	YES
74LVT2952	NO	YES	YES	YES	YES	YES	YES
74LVT16240A	NO	YES	NO	NO[3]	YES	YES	YES
74LVT162240A	NO	YES	NO	NO[3]	YES	YES	YES
74LVT16244B	NO	YES	NO	NO[3]	YES	YES	YES
74LVT162244B	NO	YES	NO	NO[3]	YES	YES	YES
74LVT16245B	NO	YES	NO	NO[3]	YES	YES	YES
74LVT162245B	NO	YES	NO	NO[3]	YES	YES	YES
74LVT16373A	NO	YES	YES	NO[3]	YES	YES	YES
74LVT16374A	NO	YES	YES	NO[3]	YES	YES	YES
74LVT16500A	NO	YES	YES	NO[3]	YES	YES	YES
74LVT16501A	NO	YES	YES	NO[3]	YES	YES	YES
74LVT16543A	NO	YES	YES	NO[3]	YES	YES	YES
74LVT16646A	NO	YES	YES	NO[3]	YES	YES	YES
74LVT16652A	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16240	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT162240	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT16241	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT162241	NO	YES	NO	NO[3]	YES	NO	YES
74ALVT16244	NO	YES	NO	NO[3]	YES	YES	YES

Advanced BiCMOS features

PRODUCT	INPUT DISABLE CIRCUIT	LIVE INSERTION CAPABILITY	POWER-UP RESET	SPLIT-LEAD GROUND	INPUT BUS HOLD CIRCUIT	64 mA OUTPUT DRIVE	5-VOLT COMPATIBLE I/O
74ALVT162244	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT16245	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT162245	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT16344	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT162344	NO	YES	NO	NO[3]	YES	NO	YES
74ALVT16373	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16374	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16500	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16501	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16541	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT16543	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16600	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16601	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16646	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16652	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16731	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT162731	NO	YES	YES	NO[3]	YES	NO	YES
74ALVT16821	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT162821	NO	YES	YES	NO[3]	YES	NO	YES
74ALVT16823	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT162823	NO	YES	YES	NO[3]	YES	NO	YES
74ALVT16827	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT162827	NO	YES	NO	NO[3]	YES	YES	YES
74ALVT16841	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16899	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16952	NO	YES	YES	NO[3]	YES	YES	YES
74ALVT16953	NO	YES	YES	NO[3]	YES	YES	YES

NOTES:
1. OE inputs must be at the proper level for the outputs to be in the 3-State condition.
2. Only on Bn I/O pins.
3. These devices have multiple GROUND pins.

Introduction to Advanced Low-Voltage Technology

INTRODUCTION

ALVT, Advanced Low-Voltage Technology, provides the designer with a family of very high speed TTL and LVTTL design options. The selection of devices included in this family allow the engineer to utilize standard bus interface logic functions in speed critical applications. Some features of the ALVT family are:

- Output drive I_{OH}/I_{OL} = 32/64mA at V_{CC} = 3.3V and V_{CC} = 2.5V
- Fully I/O compatible from 2.3 to 5.5V
- Output overvoltage protection allows forcing the outputs to 5.5V without additional interfacing. This maintains compatibility with 5V TTL logic without requiring additional components.
- Supports live insertion
- Available in SSOP and TSSOP packaging
- Bus Hold eliminates the need for external pull-up resistors

APPLICATIONS

The ALVT product family offers a number of part types useful in many applications. One such application is driving DRAM arrays.

The variety of 18 and 20 bit devices, coupled with the high drive feature, makes ALVT especially suited for driving large DRAM arrays. In dense DRAM applications, it is useful to buffer CAS, RAS, and address lines through the same part. This reduces the skew between the individual signals, allowing tighter timing margins. Also, the ALVT162XXX functions feature a 30 ohm series termination resistor on each output. This termination is very effective in reducing the transmission line effects seen in large DRAM arrays. The result of ALVT's high speed, incident wave switching, minimal transmission line effects, and low skew signaling is fast DRAM access in 5V/3.3V TTL or LVTTL applications.

Another useful application of ALVT is in heavily loaded high bandwidth busses. The high drive of ALVT makes the family a logical choice for use in heavily loaded buses (35-50 ohm). The more popular bus transceiver functions (ALVT162XXX) are available with 30 ohm series output resistors. These resistors help match the impedance of heavily loaded buses, reducing transmission line induced reflections. Other features supplementing the bus interface application are 5V tolerance on I/Os and LVTTL switching level compatibility. 5V tolerance on inputs and outputs allows ALVT parts to be connected to 5V TTL ar CMOS devices, i.e., a computer bus with 5V interface boards. These features offer flexibility and backward compatibility for use in existing designs.

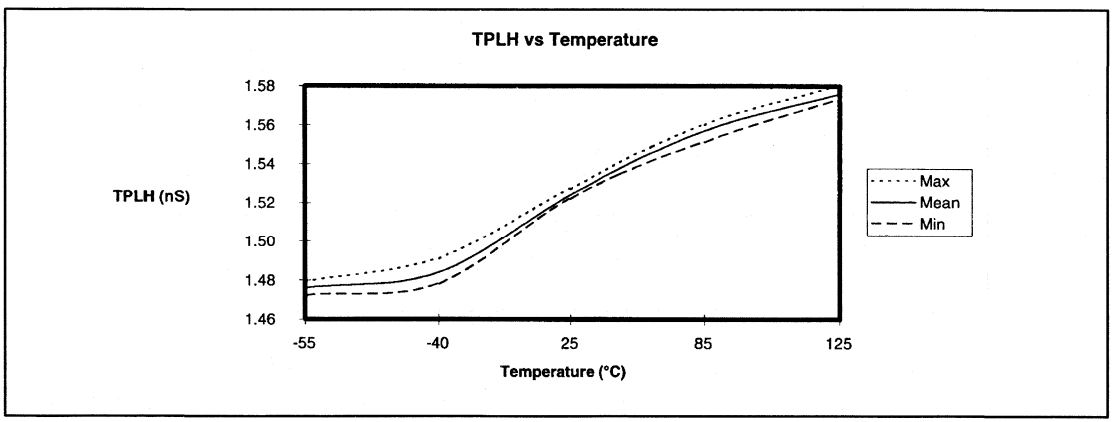


Figure 1.

ALVT16245

t_{PS} (Pin Skew or Transition Skew

$t_{PS} = | t_{PHL} - t_{PLH} |$

	V_{CC} = 2.3	V_{CC}= 2.5	V_{CC} = 2.7	V_{CC} = 3.0	V_{CC} = 3.3	V_{CC} = 3.6
t_{PS} Max (ps)	429	469	430	526	267	336
t_{PS} Min (ps)	39	79	117	73	0	100
t_{PS} Median(ps)	234	274	274	260	97	129

NOTE: One output switching, Temp = 25°C, 9 parts

Introduction to Advanced Low-Voltage Technology

PROCESS TECHNOLOGY

The fabrication of ALVT uses an advanced BiCMOS process called QUBiC-LP. This process is a low voltage/low power version of the popular QUBiC process. Some features of QUBiC-LP include:

- 13 GHz bipolar NPN devices
- 0.65µm L_{EFF} CMOS devices
- Complementary temperature characteristics of the bipolar and CMOS devices ensure stable speed performance over temperature
- High impedance, low capacitance (4-5pF) inputs
- Bipolar output structure results in high drive capability
- Lower dynamic power dissipation than competing technologies
- Low V_{CC} and ground bounce

AC CHARACTERISTICS

The most desirable characteristic of ALVT is high speed. This family of logic represents a 20% improvement over LVT devices. This feature coupled with the TTL-LVTTL compatibility makes ALVT a very effective solution in mixed voltage applications. Another desirable AC characteristic is very low pulse skew. The low pulse skew – the difference between t_{PHL} and t_{PLH} – ensures the system designer that a 50% duty cycle input signal will retain the same duty cycle on the output. This makes the designer's timing analysis much easier and results in a tighter system timing.

ALVT is the world's first BiCMOS standard logic family specified for operation in the 2.5V V_{CC} range. At 2.5V, ALVT's speed is comparable to that of LVT. This coupled with the pin for pin compatibility with LVT allows the system designer to easily migrate existing 3.3V, or even 5V, designs to 2.5V.

INPUT CHARACTERISTICS

ALVT offers both TTL and LVTTL switching level compatibility. In the 3.3V V_{CC} range TTL switching levels are used, while the 2.5V range switches at LVTTL levels. The low input capacitance, 4pF per input, along with the low input current requirement results in a high input impedance, a very desirable feature in high fanout situations. The bus hold circuit operates in the 3.3V V_{CC} range, providing pin for pin and feature for feature compatibility with the LVT family. The bus hold circuit shuts down in the 2.5V range, allowing for extra power savings due to reduced input leakage current.

OUTPUT CHARACTERISTICS

The BiCMOS technology used in the design of ALVT enables the IC designer to create very quick, very powerful output structures. The use of the bipolar devices enhances the speed of output switching while the slower CMOS devices provide high output drive. The use of a Philips Semiconductors patented circuit technology called Pass-NMOS BiCMOS Logic enhances the speed of the conventional output structure design. This innovation enables the bipolar devices in the output structure to begin their switching cycle sooner, enabling the fast speeds of ALVT devices.

As shown in Figure 2, the propagation delays of ALVT are very consistent whether switching one output or all sixteen.
Another feature of ALVT, live insertion and extraction, is really not a feature anymore, but an industry standard. This feature includes 3-State power-up and reset on power-up. These features combine to make ALVT an excellent choice in fault-tolerant computer or telecom bus applications.

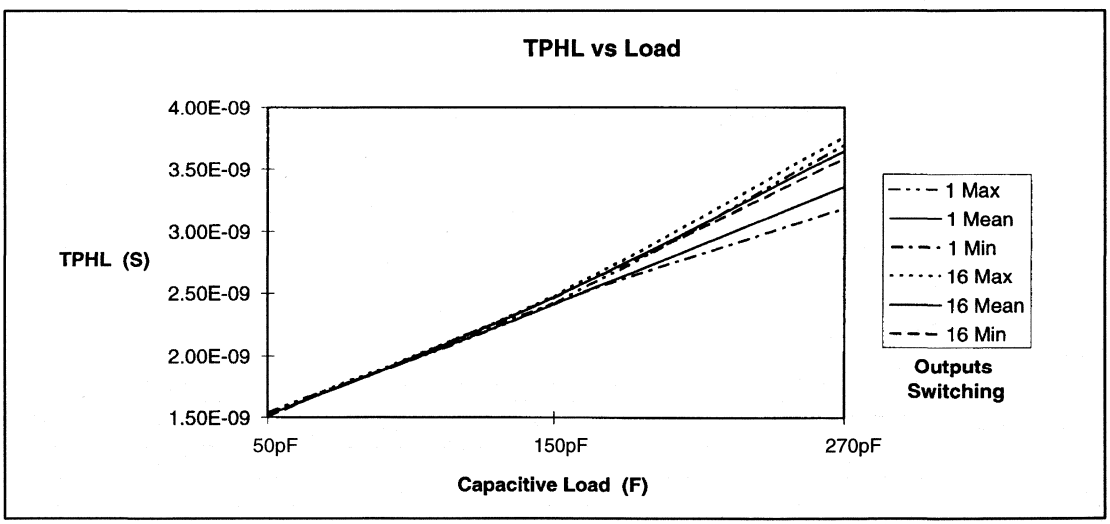


Figure 2.

POWER DISSIPATION

The primary reason for the push to lower supply voltages revolves around smaller fabrication process geometries. Another important reason is power dissipation on the chip level. From a system point of view, power dissipation at the package and part level are also very important. The design of the ALVT provides high output drive currents while maximizing overall power consumption.

Figure 3 shows I_{CC} vs frequency with the standard TTL load.

NOISE

Ground bounce and V_{CC} bounce, also called simultaneous switching noise, are critical sources of noise in logic products. The design of ALVT keeps this fact in mind. The combination of package style, pin configuration, and edge rate control helps keep the effects of simultaneous switching noise. ALVT attacks this problem through use of SSOP and TSSOP packages, industry standard flow through pinout with multiple ground and V_{CC} pins, and advanced circuit design to actively control edge rates.

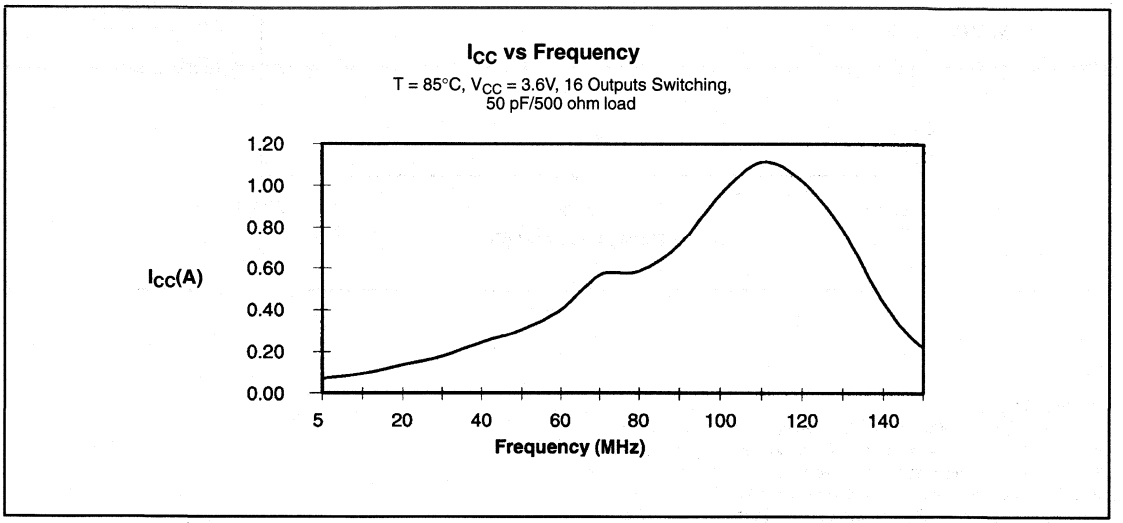


Figure 3.

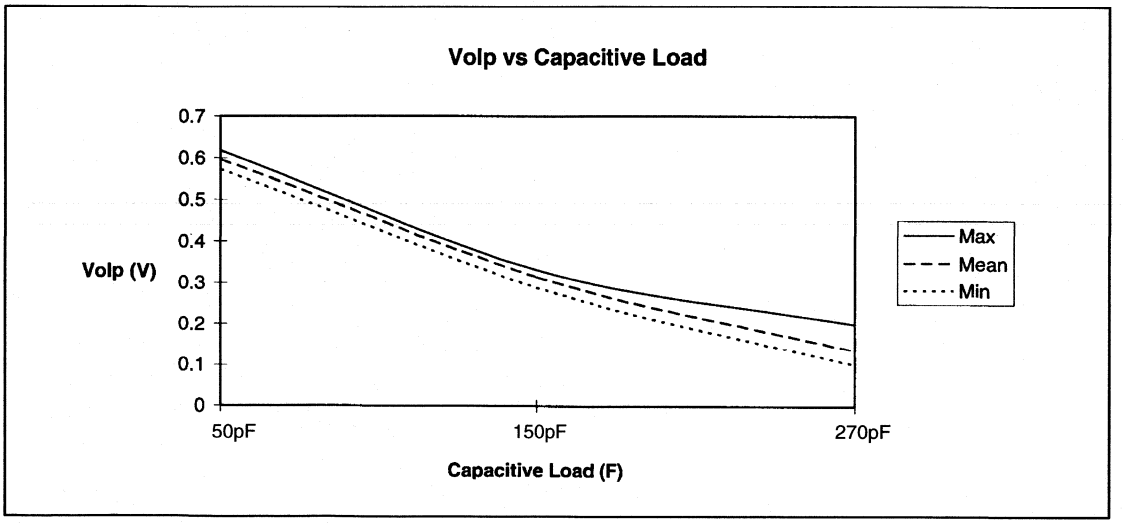


Figure 4.

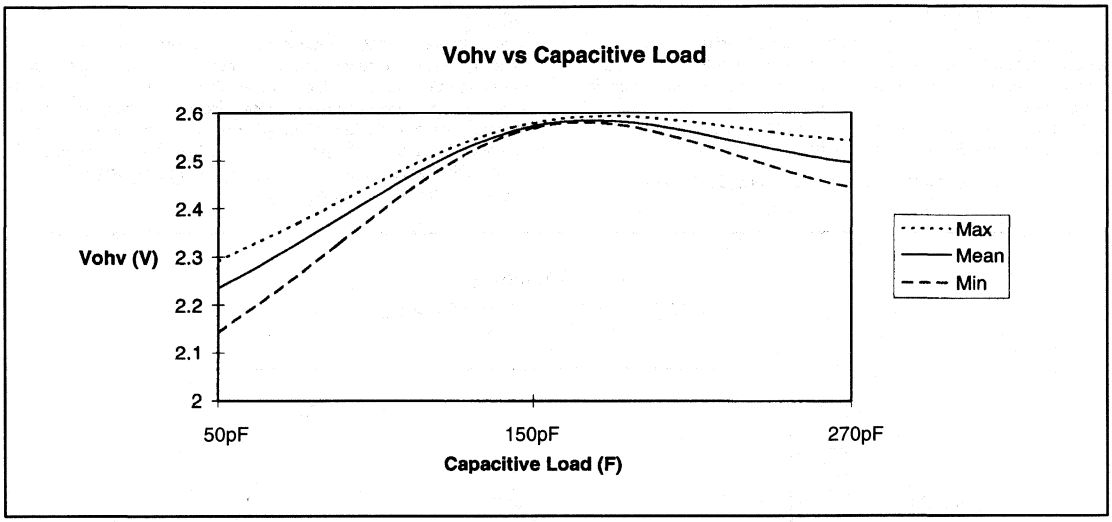


Figure 5.

CONCLUSION

ALVT represents another step in the evolution of standard logic products. The high speed, mixed voltage compatibility, and high drive make the family a superior choice in lower voltage, high speed CPU designs. The feature set included in the ALVT family and the selection of functions will allow system designers to extend their existing designs well into the future.

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire 74ABT family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74ABT Advanced BiCMOS families combines the low power dissipation and low noise of BiCMOS with the high speed and high output drive of bipolar products.

The basic family of devices designated as 74ABTXXX will operate at TTL logic input levels or CMOS logic input levels. The devices operate from a power supply of 4.5 to 5.5V.

HANDLING BICMOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

However, to be totally safe, it is wise to use ESD handling precautions at all times.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

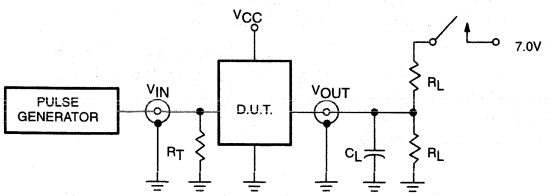
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

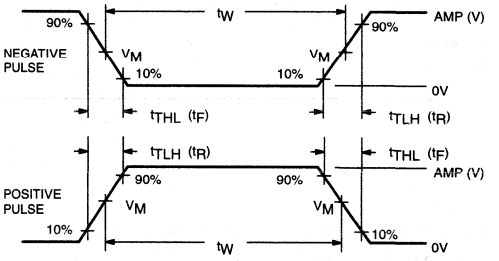
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = V_{CC} or GND		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		39	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
All	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00057

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire 74ABT/H16 family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74ABT/H16 Advanced BiCMOS families combine the low power dissipation and low noise of BiCMOS with the high speed and high output drive of bipolar products.

The basic family of devices designated as 74ABT/H16XXXA will operate at TTL logic input levels or CMOS logic input levels. The devices operate from a power supply of 4.5 to 5.5V.

HANDLING BICMOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

However, to be totally safe, it is wise to use ESD handling precautions at all times.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

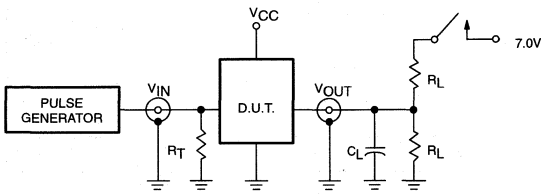
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

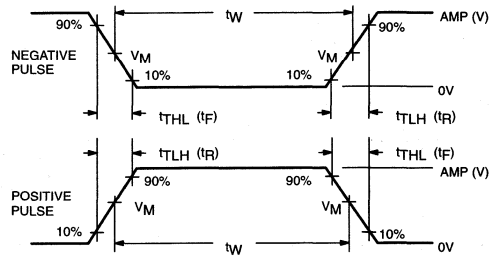
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.8	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.35	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = V_{CC} or GND		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current	V_{CC} = 4.5V; V_I = 0.8V	35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V	–75			–75		µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±2	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V or V_{CC}; V_I = GND or V_{CC}; V_{OE} = Don't care		±2	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		1.0	10		10	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		2.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.5	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		5.0	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		200	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire MB family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The MB Advanced BiCMOS family combines the low power dissipation and low noise of BiCMOS with the high speed and high output drive of bipolar products.

The basic family of devices designated as 74ABTXXX will operate at TTL logic input levels or CMOS logic input levels. The devices operate from a power supply of 4.5 to 5.5V.

HANDLING BiCMOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

However, to be totally safe, it is wise to use ESD handling precautions at all times.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

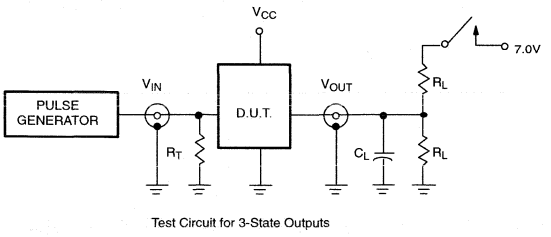
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

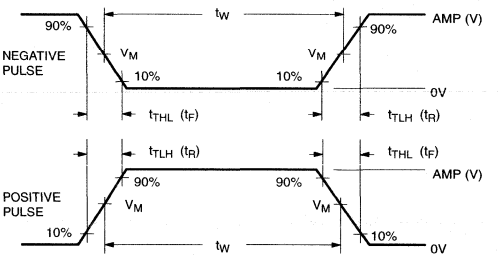
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_{OL} = 1mA; V_I = V_{CC} or GND		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{cc}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		39	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

FAMILY DESCRIPTION

The LVT family comprises very fast low-power logic ICs fabricated in an advanced sub-micron BiCMOS process.

LVT ICs at a supply voltage of 3.3V operate at the same speed as ABT BiCMOS logic at V_{CC} = 5V and they consume considerably less power.

The LVT family functions down to V_{CC} = 2.7V for application in unregulated systems and provides a number of extra features not found in other logic families.

The reduction from the standard 5.0V to 3.3V reduces the output swing, leading to a much lower power dissipation. Pin and function compatibility with ABT ensure an easy transfer of existing systems into new 3.3V systems.

HANDLING BiCMOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

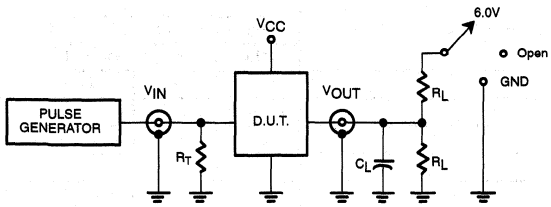
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

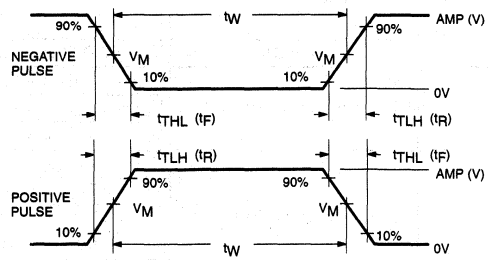
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = −18mA			−0.9	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = −100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = −8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = −32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND			0.1	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V	Control pins		1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±0.1	±1	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	10	
		V_{CC} = 3.6V; V_I = 0			−1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current Data inputs	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		−75	−150		µA
I_{EX}	Current into an ouptut in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	−5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = +25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV00092

FAMILY DESCRIPTION

The LVT16 family comprises very fast low-power logic ICs fabricated in an advanced sub-micron BiCMOS process.

LVT16 ICs at a supply voltage of 3.3V operate at the same speed as ABT BiCMOS logic at V_{CC} = 5V and they consume considerably less power.

The LVT16 family functions down to V_{CC} = 2.7V for application in unregulated systems and provides a number of extra features not found in other logic families.

The reduction from the standard 5.0V to 3.3V reduces the output swing, leading to a much lower power dissipation. Pin and function compatibility with ABT16 ensure an easy transfer of existing systems into new 3.3V systems.

HANDLING BICMOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

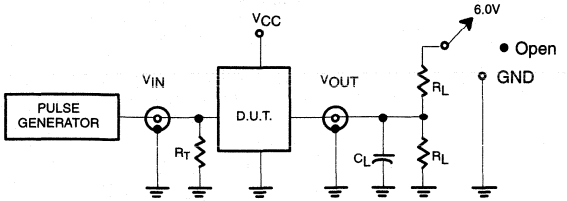
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

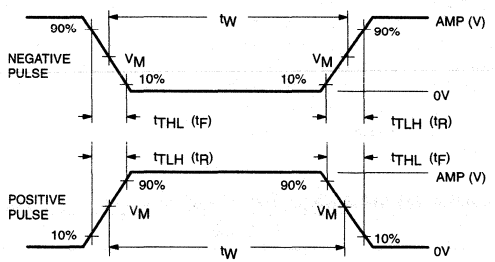
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.55		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.30		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.36	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND			0.1	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1.0	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1.0	±100	µA
I_{HOLD}	Bus Hold current Data inputs	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		-75	–130		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00040

FAMILY DESCRIPTION

ALVT is the world's fastest low-voltage BiCMOS standard logic family. Fabricated using the advanced QUBiC-LP process, ALVT is specified to operate with the 3.3V power supply range and the new JEDEC standard 2.5V range. Both ranges of operation offer input and output compatibility with 5V logic products, and pin for pin compatibility with existing ABT and LVT families.

The speed of ALVT extends TTL well into the 100MHz operating range while providing the power savings of low voltage. ALVT provides a 20% speed enhancement over LVT operating at 3.3V and equals LVT speeds when used at 2.5V

HANDLING BICMOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		24		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND			0.1	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs	V_{CC} = 3.0V; V_I = 0.8V		75	120		µA
		V_{CC} = 3.0V; V_I = 2.0V		–75	–130		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.3	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

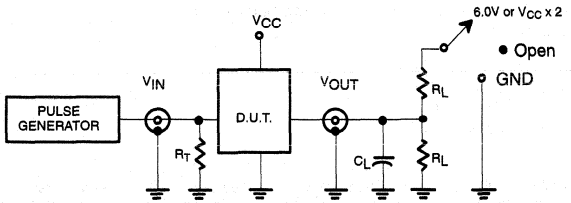
NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

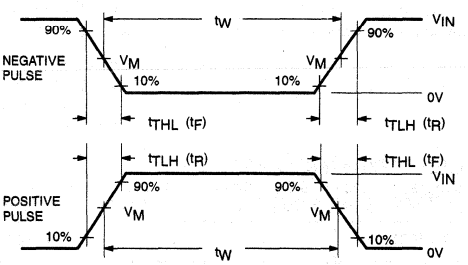
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		V
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = GND or V_{CC}	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.0	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire FBL family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The FBL Advanced BiCMOS family combines the low power dissipation and low noise of BiCMOS with the high speed and high output drive of bipolar products.

The basic family of devices designated as FBL will operate at TTL logic input levels or CMOS logic input levels. The devices operate from a power supply of 3.0 to 3.6V.

HANDLING BICMOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +4.6	V
V_{IN}	Input voltage	AI0 – AI6, OEB0, $\overline{OEBn}$, OEAn	-0.5 to +7.0	V
		$\overline{B0} – \overline{B6}$	-0.5 to +3.5	
I_{IN}	Input current	$V_{IN} < 0$	-50	
V_{OUT}	Voltage applied to output in High output state		-0.5 to +7.0	V
I_{OUT}	Current applied to output in	AO0 – AO6	64, –64	mA
	Low output state/High output state	$\overline{B0} – \overline{B6}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		COMMERCIAL LIMITS V_{CC} = 3.3V±10%; T_{amb} = 0 to +70°C			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage	Except $\overline{B0}$–$\overline{B6}$	2.0			V
		$\overline{B0} – \overline{B6}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}$–$\overline{B6}$			0.8	V
		$\overline{B0} – \overline{B6}$			1.47	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	AO0 – AO6			-32	mA
I_{OL}	Low-level output current	AO0 – AO6			+32	mA
		$\overline{B0} – \overline{B6}$			100	
C_{OB}	Output capacitance on B port			6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

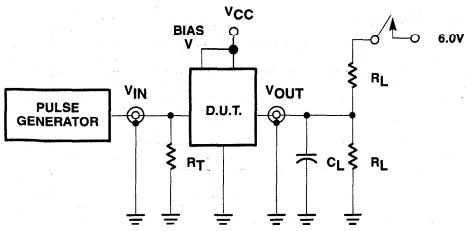
Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0} - \overline{B6}$	V_{CC} = MAX, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0} - \overline{B6}$	V_{CC} = 0V, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	AO0 – AO6[3]	V_{CC} = MIN to MAX; I_{OH} = -100µA	V_{CC} –0.2			V
			V_{CC} = MIN; I_{OH} = -8mA	2.4			V
			V_{CC} = MIN; I_{OH} = -32mA	2.0			V
V_{OL}	Low-level output voltage	AO0 – AO6[3]	V_{CC} = MIN; I_{OL} = 16mA			0.4	V
			V_{CC} = MIN; I_{OL} = 32mA			0.5	V
		$\overline{B0} - \overline{B6}$	V_{CC} = MIN, I_{OL} = 4mA	0.5			V
			V_{CC} = MIN, I_{OL} = 100mA	0.75	1.0	1.20	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK} = –18mA		–0.85	-1.2	V
I_I	Input leakage current	Control pins	V_{CC} = 3.6V; V_I = V_{CC} or GND			±1.0	µA
		Control/ AI0 – AI6	V_{CC} = 0V or 3.6V; V_I = 5.5V			10	
		AI0 – AI6	V_{CC} = 3.6V; V_I = V_{CC}			1	
		Note 4	V_{CC} = 3.6V; V_I = 0V			–5	
I_{IH}	High-level input current	$\overline{B0} - \overline{B6}$	V_{CC} = MAX, V_I = 1.9V			100	µA
I_{IH}	High-level input current	$\overline{B0} - \overline{B6}$	V_{CC} = MAX, V_I = 3.5V, note 5	100			mA
I_{IL}	Low-level input current	$\overline{B0} - \overline{B6}$	V_{CC} = MAX, V_I = 0.75V			-100	µA
I_{OZH}	Off-state output current	AO0 – AO6	V_{CC} = MAX, V_O =3V			5	µA
I_{OZL}	Off-state output current	AO0 – AO6	V_{CC} = MAX, V_O = 0.5V			-5	µA
I_{CC}	Supply current (total)	I_{CCZ}	V_{CC} = MAX		5.2	13.5	mA
		I_{CCB}	V_{CC} = MAX, outputs Low or High		3.2	9.0	
		I_{CCL} A3	V_{CC} = MAX, outputs Low		13.5	19.5	
		I_{CCH} A5	V_{CC} = MAX, outputs High		10.7	16.0	

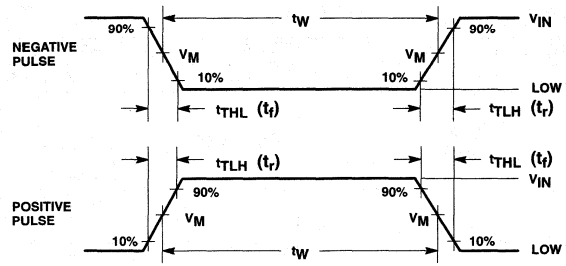
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
4. Unused pins are at V_{CC} or GND.
5. For B port input voltage between 3 and 5 volt; I_{IH} will be greater than 100mA but the part will continue to function normally (clamping circuit is active).

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port



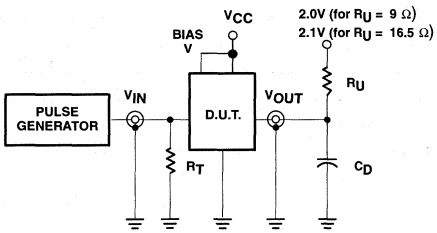
V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

SWITCH POSITION FOR ALL A-PORTS

TEST	SWITCH
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	CLOSED
t_{PHZ}, t_{PZH}	GND

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns



Test Circuit for Outputs on B Port

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

SG00090

SPICE / IBIS behavorial models

SPICE Models

SPICE models are available for the ABT, LVT, and ALVT families. These models play an important role in optimizing applications and improving understanding of practical details so that designers can take better measures to improve their designs. Design changes and optimization can be done prior to circuit board layout, saving time and effort.

SPICE may be used to test behavior in exceptional circumstances or situations that are not covered in the data sheets of the parts. For instance it is possible to see the effect of higher capacitive loading of the outputs. Also, testing of waveforms inside a package is virtually impossible, but with SPICE one may actually check waveforms and currents inside the IC. This may be very helpful in estimating noise voltage developed across bonding wires (ground bounce) and EMC aspects. Last but not least, SPICE models are very helpful in testing an application with worst case devices. The worst case models are actually worse than the worst case parts delivered to customers. This allows for the design of very safe applications in a variety of environmental conditions.

You can request the SPICE libraries with a modeling manual through your Philips Semiconductors representative.

Model updates can be downloaded from the World Wide Web at: www.philipslogic.com.

Behavioral Models

Behavioral models are another signal integrity tool that designers can use to predict circuit behavior. Third party models are offered through Zeelan Technology for various Philips logic product families. Zeelan generates model libraries based on measurements from actual parts. Models are formatted for specific simulator platforms including Mentor Graphics, Viewlogic, and Cadence as well as others. With the growing interest in IBIS models, that format is also supported. For information, please contact:

Zeelan Technology
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070
U.S.A.

Phone: (503) 685–1000
FAX: (503) 685–1001
Website (url): www.zeelan.com
Email: info@zeelan.com

IBIS models generated within Philips are planned for logic product types, so contact your Philips representative for updates.

Interfacing 3V and 5V applications AN240

Authors: Tinus van de Wouw (Nijmegen) / Todd Andersen (Albuquerque)

1.0 THE NEED FOR INTERFACING BETWEEN 3V AND 5V SYSTEMS

Many reasons exist to introduce 3V[1] systems, notably the lower power consumption for mobile applications and the introduction of parts that use technologies with such fine geometries that 5V is simply not allowed any more.

The introduction of the 3V standard as supply voltage has resulted in many design activities for digital systems. Very often, however, there is a gradual transition from 5V to 3V, since not always are all required components available, or the system is rather complex so that 3V is introduced in part of a system. As an example, customers wish to use an existing and proven CPU, while a new, more complex ASIC with added features can only be made with 3V. Or vice versa!

With the introduction of new standards such as 2.2-2.7V or even 1.7V we expect that interfacing between systems that use different supply voltages will be an actual issue for many years to come. This application note specifically addresses the interfacing between 3V and 5V systems, but the results can be applied for interfacing between other voltage levels as well.

We will discuss how one can ensure reliable information exchange and how to prevent current flow between both supply voltages when interfacing logic with memories, ASICs, PLDs and microprocessors at different supply voltages.

2.0 LEVEL SHIFTING - INPUT AND OUTPUT LEVELS

We obviously want a reliable signal transfer from the 5V system to the 3V system and vice versa. This implies that the output voltages should be such that the input levels are exceeded.

2.1 TTL and CMOS Switching Levels

As a reminder, digital circuits have input levels defined: one voltage (V_{IL}) below which the circuit certainly sees it as a logical "0" and another voltage (V_{IH}) above which the input is guaranteed "1".

Digital circuits normally come in two versions:

- TTL levels: V_{IL} = 0.8V, V_{IH} = 2.0V
- CMOS levels: V_{IL} = 0.3 V_{CC}, V_{IH} = 0.7 V_{CC}.
  For systems with V_{CC} = 5.0 ± 0.5V this practically means:
  V_{IL} = 1.35V, V_{IH} = 3.85V.

2.2 Level Shifting from 5V to 3V

All 5V families have an output voltage swing that is large enough to drive 3V reliably. As described in Section 4.0, outputs may be as high as 3.5V for many "TTL" output stages, to the full 5V for many CMOS outputs. Therefore, as far as switching levels are concerned, there are no problems in interfacing from 5V to a 3V system.

2.3 Level Shifting from 3V to 5V

All 3V logic families deliver practically the full output voltage swing of 3V, so they can drive TTL switching levels without problems (see Fig. 1).

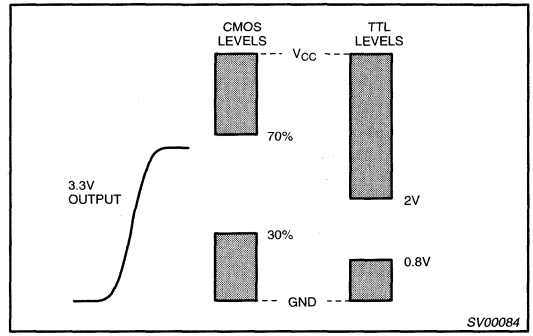


Figure 1. Switching Levels

One issue remains: a 3V system driving a 5V one that has CMOS input levels. This cannot be reliably done by standard 3V logic families, even when using pull-up resistors, simply because under worst case conditions, the output voltage is not high enough to guarantee that the signal will be seen as a logical "1". Philips Semiconductors developed special dual V_{CC} levelshifters to address that situation (see Section 6.0).

3.0 INPUT STRUCTURES OF DIGITAL CIRCUITS

Before discussing further issues on 3-5V interfacing we should start by investigating the inputs of digital circuits in order to understand what care one should take to prevent problems.

3.1 ESD Input Protection Circuits

Virtually all inputs of a digital circuit contain an ESD protection circuit that prevents damage against electrostatic discharge. This circuit is present between the physical input pin and the active circuit. Two popular schemes are given in Fig. 2.

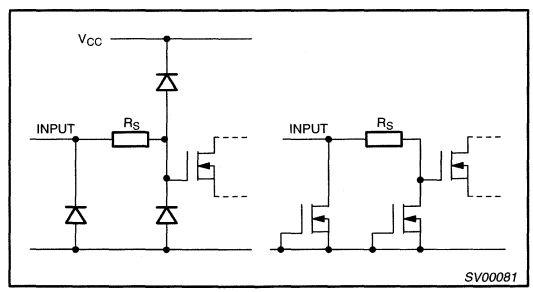


Figure 2. ESD Protection Circuits

The classic CMOS scheme as shown left provides protection against negative zaps by the diodes to ground. Positive zaps are clamped by the diode to V_{CC}. The real disadvantage is that the maximum input voltage of such a circuit is limited to V_{CC} + 0.5V. For a V_{CC} of 3V the allowed input voltage is too low for direct interfacing to most 5V systems.

1. We use the expression "3V" when a supply voltage is used between 2.7 and 3.6V.

Modern low voltage circuits use a double transistor circuit as shown right that was pioneered in our ABT families. Two transistors (Bipolar or MOS) act as fast Zener diodes protecting against positive zaps. Now, there is no diode to V_{CC} and the maximum input voltage is not limited by V_{CC}.

Typically, such circuits have a breakdown voltage between 7 and 10V, easily allowing input voltages from any 5V system.

LV is the only family that employs a classic protection circuit, all other Philips Semiconductors low voltage logic families have the dual transistor protection circuit.

3.2 Bus Hold Circuits

ALVC, LVC16 and LVT families use bus hold circuits as shown in Fig. 3. A bus hold circuit holds the input at the most recent value when the input is left floating by using a small MOS transistor as pull-up or pull-down device.

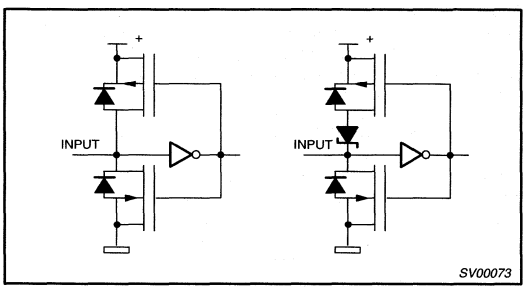


Figure 3. Bus hold circuits

A bus hold circuit for CMOS as shown left has also a diode between the input and V_{CC} which is formed by the intrinsic diode between the source and drain of the upper PMOS. This means that for ALVC and LVC16 the input voltage is limited to V_{CC} + 0.5V.

A different bus hold circuit is used in LVT parts as shown right due to the versatility of the QUBiC process which allows the use of a series Schottky diode so that there is no current path to V_{CC} in the bus hold circuit used for LVT.

4.0 OUTPUT STAGES OF DIGITAL CIRCUITS

Output structures of digital circuits (see Figs. 4 and 8) determine the output voltage swing. Circuits may swing between GND and V_{CC} or the swing may be limited by voltages developed internally.

Also, output structures determine the behavior when the output pin is taken above V_{CC}, which may be the case when two outputs are tied together on a common bus.

4.1 Bipolar Output Stage

A typical bipolar output structure does not have the full output voltage swing. When a 5V output is active HIGH, the output voltage is limited to $V_{CC} - 2 \quad V_{BE}$ (= approx. 3.6V). Therefore, quite often, interfacing with 3V systems works without currents flowing from the 5V supply into the 3V supply, or the current is so low that there is no real problem.

4.2 CMOS output stage

The output for a typical CMOS part swings fully between GND and V_{CC}.

One important point to note is that there is an intrinsic diode between the source and the drain of the upper PMOS as shown in Fig. 4. This may cause a current to flow from the output to V_{CC} when the voltage on the output pin is lifted higher than one diode voltage above V_{CC}.

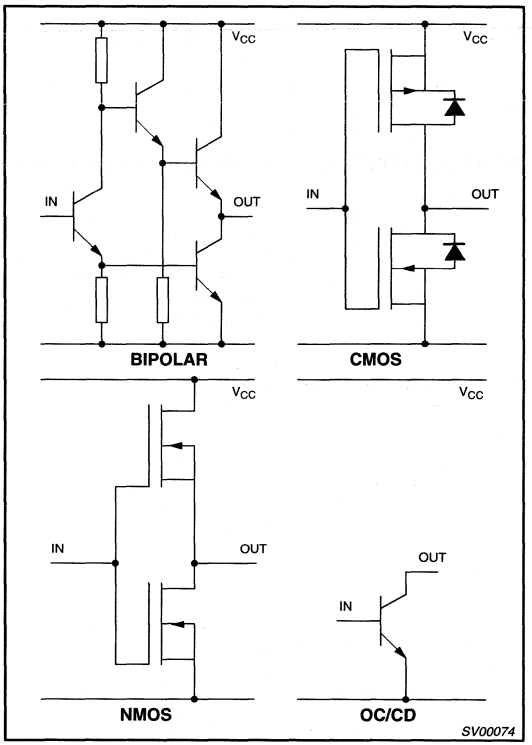


Figure 4. Typical digital output structures

4.3 Other MOS Output Structures

Some other MOS output stages such as many SRAM and DRAM circuits may have a circuit that shows a behavior similar to a bipolar output stage. An example is given Fig. 4: the upper NMOS limits the output voltage to $V_{CC} - V_{TH}$ (= approx. 3.5V). Such a circuit often works fine when driving 3V systems.

4.4 Open Collector/Open Drain

Some parts have an "Open Collector" or "Open Drain" output stage and there is no internal circuit to pull the output high. Normally a pull-up resistor connects the output to a voltage that can be higher than V_{CC}. Obviously such parts allow easy interfacing, but for speed reasons the pull-up resistor often needs to be relatively small, so the use of pull-up resistors increases power losses.

4.5 The BiCMOS Output

A BiCMOS output combines the advantages of bipolar (i.e. high output drive, low noise) and CMOS (full output voltage swing, low standby current). The output stage of Philips Semiconductors BiCMOS parts has some specific features that will be discussed in Section 6.1.

5.0 CURRENT FLOW FROM +5V TO +3V OR TO GROUND

A particular issue to address is the flow of current from the 5V power supply to the 3V supply. Then, the 3V supply may be charged up to a higher voltage which is potentially hazardous, affecting all connected 3V ICs. In addition the current provides extra power losses and may damage parts, although normally the driver capability is such that no damage occurs.

One other issue to study is the behavior of parts when either the 5V or 3V supply line is made 0V (suspend or power-down mode). In such a case high currents may flow from V_{CC} to ground.

5.1 Current Flow from the 5V Supply into a 3V Input

In mixed mode systems there is always data transmission from 5V to 3V. In such a case a 5V output drives a 3V input circuit. A potentially damaging current can only flow when two conditions are met: first, the 5V driver should be able to deliver current when the output voltage exceeds approximately 3.5V; second, the input circuit of the 3V part driven should have a current path from its input pin to V_{CC}. One has to carefully consider both aspects and check especially for a current path from the inputs of 3V parts to V_{CC}. Even with 5V parts that have limited output voltage swings, considerable currents may flow under worst case conditions.

5.2 Transceivers

The 3V part driven is often a transceiver, so the 'input' is effectively an input paralleled by an output. This means that the behavior of an output when its voltage exceeds V_{CC} is also important. More specifically, a CMOS transceiver has its output's intrinsic diode tied to V_{CC} that still provides a current path even when the part is in 3-State.

A similar situation may occur in the case of bus contention, when both outputs try to drive the bus HIGH. Fig. 5 shows the current paths via the active part and via the intrinsic diode of a CMOS output stage.

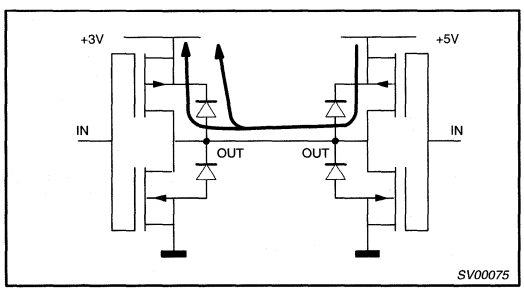


Figure 5. Currents from +5 to +3V

5.3 Suspend Mode or Power-down Mode

For energy savings parts of systems may be powered down, i.e., the supply voltage is made zero (called suspend mode or power-down mode) and the same observations can be made as above. In general, when a part allows 5V on its output under normal operating conditions, it also can withstand 5V on its output when V_{CC} is made zero. This is not always the case, however, especially for some competitive dual V_{CC} level shifters (see Section 6.1).

5.4 Summarizing Current Flow

When looking at unwanted currents from the 5V supply to the 3V supply, or in the case of suspend or power-down mode, we should study the following:

- The output capability of the driver (with V_{CC} = 5V)
- The input circuit of the driven part

When the driven part is a transceiver, we also have to look at:

- The behavior when the part is in 3-State: is there a diode to V_{CC}?
- Its output characteristics when the part is active HIGH in the case of bus contention.

6.0 PHILIPS SEMICONDUCTORS LOW VOLTAGE LOGIC FAMILIES

Philips Semiconductors has a wide range of logic families optimized for operation at 3V. Below we only discuss the properties for level shifting between 3 and 5V systems; other data can be found in the databook or brochures. In addition SPICE simulation models are available (see Section 7.0).

6.1 Main Interfacing Properties per Family

LV, which is derived from HCMOS, has a classical ESD protection circuit with a diode to V_{CC}; therefore its input interfacing capabilities are limited. The input voltage should not exceed V_{CC} + 0.5V (see Fig. 2 and Fig. 6) or the input current should be limited. As a result, one may use 5V outputs with a low drive capability as input for LV, or TTL outputs with a limited output voltage such as DRAM outputs described in Section 4.0. Obviously this is strongly dependent on the circuit layout of the driving 5V device.

LV has a standard CMOS output with a diode between the output and V_{CC}, so its output voltage is limited to V_{CC} + 0.5V.

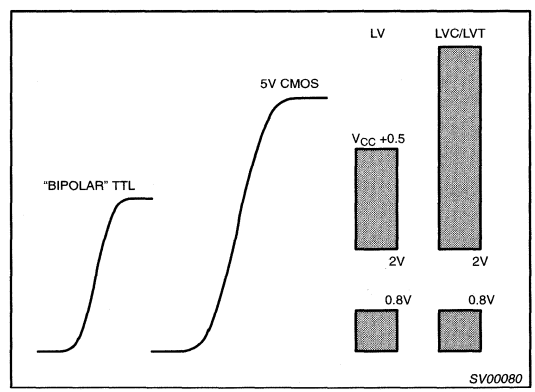


Figure 6. 5V Driving 3V

LVC has an input circuit without a diode to V_{CC}. Unidirectional devices, i.e., all parts that are not transceivers, can perfectly interface between 3V and 5V without any difficulty (see Fig. 6). Transceiver circuits, as described in Section 4.0, have a diode to V_{CC} in the output stage and have therefore limitations similar to LV.

The output voltage of LVC is limited to V_{CC} + 0.5V since it has a standard CMOS output with a diode between the output and V_{CC}.

Currently being introduced[2] is an enhancement to the LVC parts that have 3-State capability: 5V I/O tolerant (see Fig. 7). It works by dynamically tying the back gate to the highest possible voltage, either V_{CC} or V_{OUT}, such that the diode is never forward biased. This patented feature allows 5V on its output when the part is in 3-State. When the part is active HIGH, obviously there is still a current path from the output to V_{CC} via the active PMOS.

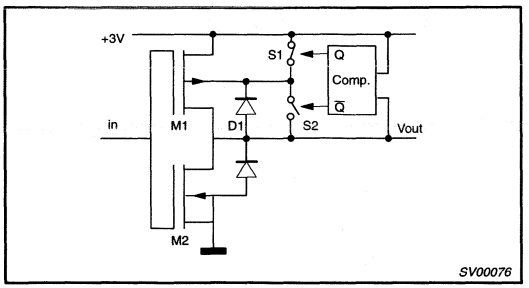


Figure 7. New LVC Output Structure

LVC16 parts have a bus hold circuit as described below under ALVC, limiting the 5V input tolerance to control pins only.

HLL behaves identical to LVC. Due to its high speed and high drive, the output is not 5V tolerant.

ALVC has an ESD protection circuit similar to LVC, but also employs bus hold circuits on its data inputs (i.e. not on its control inputs) as described in Section 3.2. Therefore, both unidirectional and bidirectional devices have the same limitations as LV. Its control inputs, such as OE and DIR, may be driven from both 3V and 5V. For speed reasons we do not plan a 5V tolerant version.

LVT uses QUBiC with its versatility in internal component options. LVT's bus hold has a built-in Schottky diode that prevents any currents from the input to V_{CC}, as is the case for the bus hold used in ALVC.

In its output stage (see a simplified circuit in Fig. 8) the output diode to V_{CC} is eliminated using a Schottky diode, making LVT fully 5V compatible when the part is in 3-State.

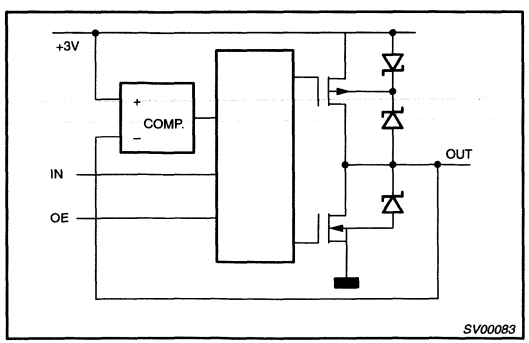


Figure 8. LVT's Output Circuit

Moreover, a special circuit has been incorporated that switches off the current path to V_{CC} when the output is pulled more than approximately 0.5V above V_{CC}. A comparator simply switches off the output stage, disregarding the state of the inputs and the control pins. This feature, called 'overvoltage protection', makes LVT fully 5V compatible and makes LVT the ideal choice for all sorts of mixed mode systems. There are no basic limitations in using LVT in mixed mode systems.

When the output voltage of LVT is lifted above V_{CC}, a current will flow, shown in Fig. 9. As one can see, where competitive devices have a current that can be considerable, a current of approximately 30mA is sufficient to toggle the overvoltage protection. The value of 30mA appears to be a good optimum to prevent noise signals from triggering the protection circuit. This implies that a simple pull-up resistor is not sufficient to pull the output into protection mode.

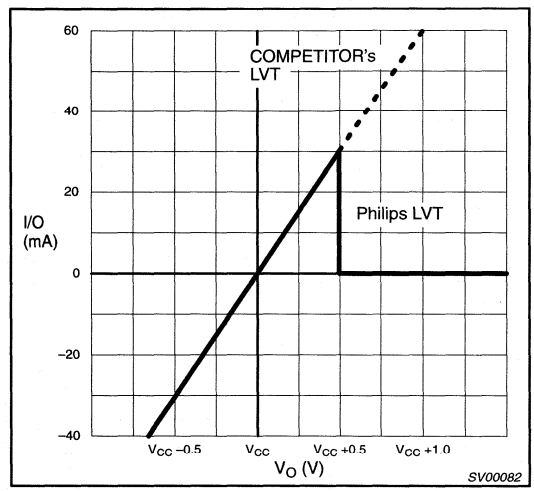


Figure 9. LVT I/O Current

It should be noted that this figure is valid when the output is active HIGH. When the output is in 3-State, no currents will flow.

Dual V_{CC} level shifters (74LVC4245 and 74ALVC164245, 8 and 16 bits resp.) are CMOS transceivers fed from both 3V and 5V supplies. The level shifting is done internally and the parts have full output voltage swings at both sides (see Fig. 10), making them ideal for level shifting purposes, especially when driving 5V CMOS levels.

2. First part available early 1996.

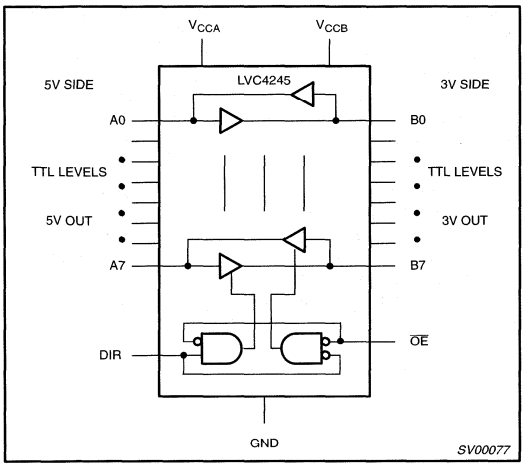


Figure 10. 74LVC4245

Dual V_{CC} level shifters are superior alternatives to the sometimes used input pull-up resistors, blocking diodes and other circuits that normally degrade speed and/or noise margins.

6.2 Summarizing Low Voltage Logic Interfacing Capabilities

Table 1 below sums up the input and output capabilities of our logic families and their behavior at suspend/power-down mode.

Table 1.

FEATURE		LV	LVC	LVC16 ALVC	LVT LVT16	DUAL V_{CC} LEVEL SHIFTERS
Drive 5V TTL levels		✓	✓	✓	✓	✓
Drive 5V CMOS levels		–	–	–	–	✓
5V on Input		–	✓	–	✓	✓[2]
5V on Control pins		–	✓	✓	✓	✓
5V on Output	when in 3-State	–	–/✓[1]	–	✓	✓[2]
	when active HIGH	–	–	–	✓	✓[2]
Suspend/power down mode		–	–/✓[1]	–	✓	–

NOTES:
1. Feature to be introduced early 1996 for 3-State LVC parts.
2. Valid for side working from the +5V supply side when V_{CC} = 5V

6.3 Unidirectional Dataflow from 5V to 3V

Fig. 11 gives the situation for unidirectional data flow from 5V to 3V. Any 5V TTL part can basically drive the 5V tolerant inputs of LVC, HLL and LVT. The other families need a dual V_{CC} level shifter to prevent current flow from the 5V supply into the inputs of the 3V logic.

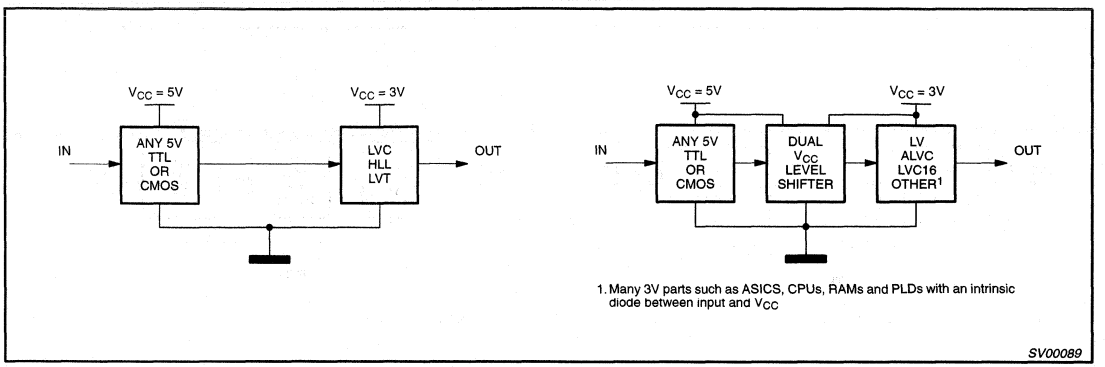


Figure 11. 5V Drivers to 3V Receivers

6.4 Unidirectional Dataflow from 3V to 5V

Fig. 12 Shows that driving 5V TTL can be done from any 3V logic family. When driving 5V CMOS levels, a dual V_{CC} level shifter is required to increase the output voltage swing.

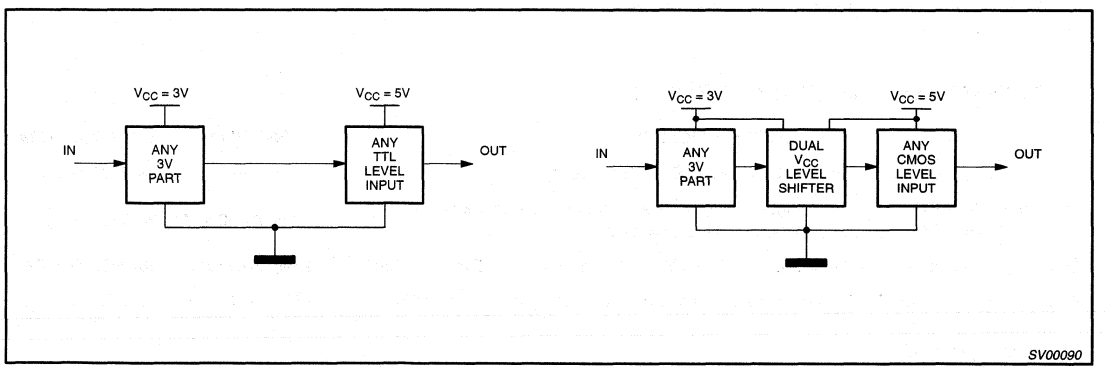


Figure 12. 3V Drivers to 5V Receivers

6.5 Bidirectional Data Communication Between 5V and 3V Systems

In many cases the data communication is bidirectional, both from 3V to 5V and from 5V to 3V. Parts that operate in both directions may be transceivers, but also other parts with a combined input/output (I/O), as shown in Fig. 13.

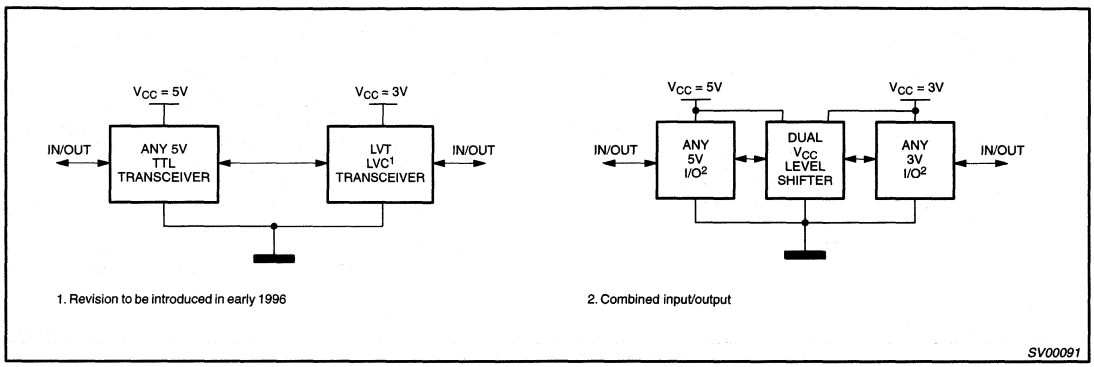


Figure 13. 5V Transceivers on Common Bus with 3V Transceivers

When either LVT or LVC with 5V tolerant outputs is used, a direct communication can be established between these and any 5V TTL level transceiver. When other low voltage families or parts with I/O are used, the dual V_{CC} levelshifters provide the transceiver function with built-in level shifting and preventing current flows between power supplies.

7.0 REFERENCES AND FURTHER READING

AUTHOR AND TITLE	ORDER NO.	ORDER NO. USA
Brian Martin, *Tips for straddling the 3V to 5V Fence* (EDN, Apr 4, 1994)	—	98 2902 010
Tinus van de Wouw, Rob Croes and Yong-in Shin, *Considerations for interfacing with Philips 3V HLL/LV with 5V ICs in mixed mode systems*, 1993	9398 706 29011	98 2902 003
Philips Semiconductors, Data Handbook IC24, *Low Voltage CMOS and BiCMOS families*, 1995	9398 652 71011	98 2902 002 02
Philips Semiconductors, *SPICE I/O models for 5V and 3.3V Standard Logic Families*, 1995	9397 750 00119	9397 750 00119

8.0 CONCLUSION

This report gives many details on how to properly communicate between 3V and 5V systems. Special characteristics of Philips Semiconductors low voltage logic families often allow easy and worry-free translation of data from one system to the other.

LVT (Low Voltage Technology) and ALVT (Advanced LVT) AN243

Author: Tinus van de Wouw, Philips Semiconductors, Nijmegen

1 INTRODUCTION

Philips Semiconductors has introduced two low voltage families optimized for backplane driving applications: LVT (Low Voltage Technology) and ALVT (Advanced LVT). The purpose of this note is to provide better insight into both families for optimal use by designers in their applications.

New circuit techniques have been pioneered that give LVT and ALVT their unique properties, some of which will be discussed in detail.

Both families are fabricated using QUBiC, an advanced BiCMOS process, where the best properties of bipolar transistors (f_T=17GHz) are combined with optimized CMOS (0.65 – 0.8 µ). In addition, special components can be built in such as Schottky diodes and zener diodes for specific requirements. QUBiC processing enables extremely short propagation delay times combined with low power dissipation, low noise and high output drive. The process also allows very low temperature dependency of AC and DC characteristics.

The excellent properties available in the world's first Advanced BiCMOS family, Philips Semiconductors' 5V ABT family, are now taken to even greater heights in LVT and ALVT.

Table 2. Basic Properties of LVT and ALVT

PARAMETER	LVT	ALVT		UNIT
		3.3V range	2.5V range	
Supply voltage	2.7–3.6	2.7–3.6	2.3–2.7	V
Input voltage	5.5			V
Output current	–32/64		–8/24	mA
Drive capability	35		75	Ω
Quiescent current	70		40	µA
Propagation delay	2.5 4.2	1.5 2.4	1.8 3.5	ns
Product portfolio Gates/Flip-flop 8-bit bus driver 16-bit bus driver	✓ ✓ ✓	✓		

2 APPLICATION REQUIREMENTS FOR LVT AND ALVT

Both LVT and ALVT families are intended primarily for fast low voltage bus driver applications, especially driving low bus impedances such as backplanes. For this range of applications a number of parameters are important such as operating voltage range, propagation delay, drive capability and power dissipation (see Table 2). Other important factors, discussed below, are power-up/down characteristics, 5Volt input and output capability, bus hold and ground bounce.

ALVT is different from LVT in two ways. First ALVT is fully specified at V_{CC} = 2.5V, and second, it is about 40% faster than LVT. It is the fastest TTL family available: shorter propagation delays do not exist in other 5V or 3V TTL families.

Due to the trade-off between speed and ground bounce, ALVT has only Multibyte™ products with multiple GND and V_{CC} pins (flow-through architecture). Having the same speed in a standard pinning 8 bit device would require the speed to be tuned down to a level comparable to LVT. As a result, LVT has a much wider product portfolio with a variety of 8 to 10-bit bus functions and also some very fast, lower drive gates and flip-flops. Both families have versions with built-in damping resistors (for example, '2244 or '162244) to minimize undershoot, especially for driving memories.

3 DETAILS OF THE INTERNAL CIRCUIT

Figure 1 gives a simplified version of the internal buffer circuit, with the output enable function ($\overline{OE}$) and other details (some of which will be discussed later) omitted. Its purpose is to show the basic aspects of the internal circuit so that applying LVT circuits is made easier and certain aspects of the datasheet are clarified.

The input uses a small CMOS inverter stage with a low input capacitance, so no drive energy is needed. The output LOW is bipolar (Q4) with a small (M7) in parallel, and the output HIGH is a combination of a bipolar transistor (Q2) and PMOS (M4) to pull the output to the full Vcc.

Bipolar transistors introduce less bounce than pure CMOS. The NMOS M7 is very small and therefore does not affect ground bounce. The PMOS transistor M4 is delayed via the inverters INV1/INV2 so that it becomes active somewhat later than Q2 with only a minimal effect on V_{CC} bounce. This smart construction enables the best possible trade-off between speed and bounce.

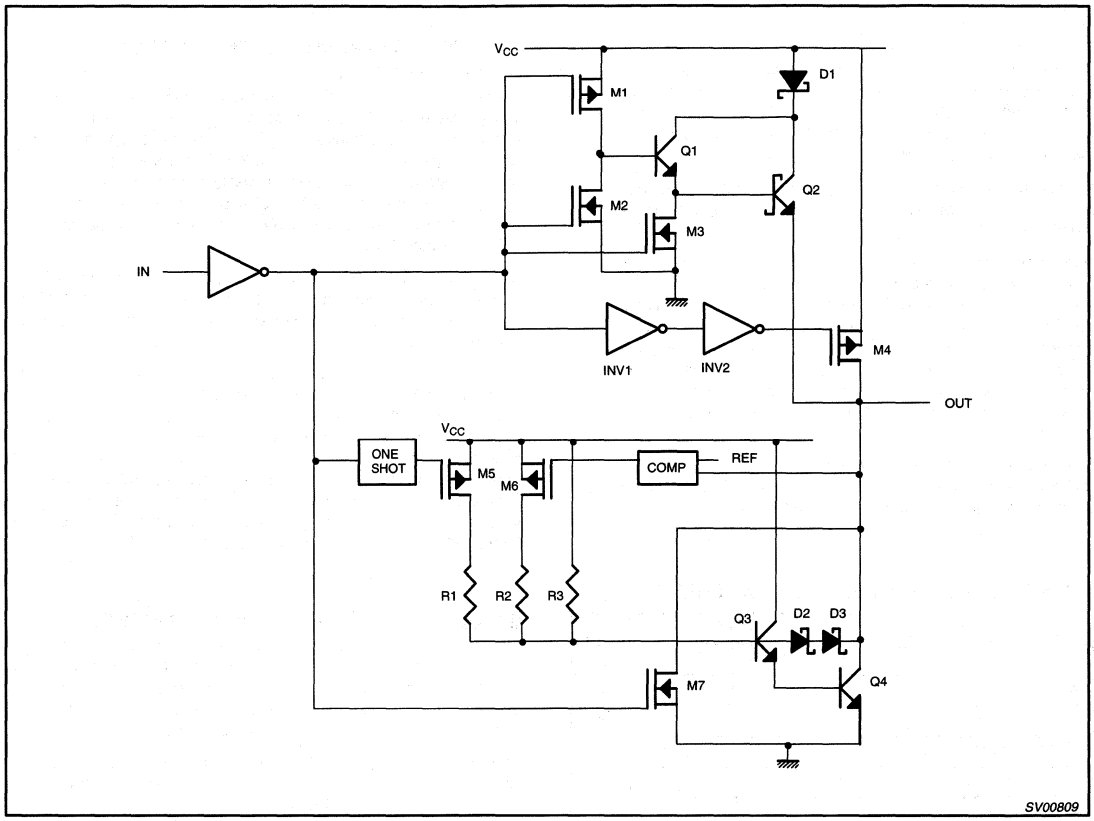


Figure 1. Simplified LVT/ALVT circuit

The drive of Q2 in the active HIGH state, taken care of by M1, M2 and Q1, is standard for advanced BiCMOS and makes optimum use of MOS and bipolar transistors to get the fastest, lowest internal capacitance inverter.

M3 ensures a fast turn-off of Q2 when the output goes LOW or into 3-state. When the output is forced LOW, a 'power-on-demand' circuit is activated. A one shot delivers Q4 with a high base current (via M5, R1 and Q3), which will quickly pull the output low. Additional base current is provided via M6/R2 and R3. The path M6/R2 is connected to the output voltage via a very fast comparator. When the output drops lower than approximately 1V, the current path via M6/R2 is blocked. The diodes D2/D3 prevent deep saturation of Q4 to enable quick turn-off.

This, at first sight, rather complex circuit ensures a very fast transition to around 1V, and below that value the output voltage smooths out somewhat so that the amount of ringing generated is kept to a minimum. Also, when the output is active LOW, a very low current is drained from the supply voltage. When a glitch appears on the output trying to pull the output HIGH, the diodes D2/D3 stop conducting, providing base current into Q3/Q4 so that the bus is pulled LOW again. This structure provides an excellent dynamic behavior, little ringing and good glitch suppression combined with low power dissipation.

When the output is in 3-state or active HIGH, only a small bias current flows (for the power-up/down circuit discussed in Section 3.1) while in the active LOW state some current flows via R3, which may vary somewhat among part types. Therefore I_{CCH} and I_{CCZ} are low, while I_{CCL} is somewhat higher.

3.1 Powering-up/Powering-down

LVT and ALVT have a feature that is useful for live insertion and removal. A circuit is built into these families that monitors the supply voltage and ensures that the output is forced to a 3-state mode when V_{CC} is lower than 1.2V. Then, the transistor does not conduct and the external $\overline{OE}$ signal is overruled and the output goes into 3-state mode. Normally, when removing a board in a live system, the power supply is removed first and high currents into the output circuit are prevented.

Above 1.2V the transistor will start to conduct and the part may again become active (i.e., the external $\overline{OE}$ enables the output). It's the task of the system designer to ensure that an external circuit forces the correct $\overline{OE}$ signal when V_{CC} is higher than 1.2V.

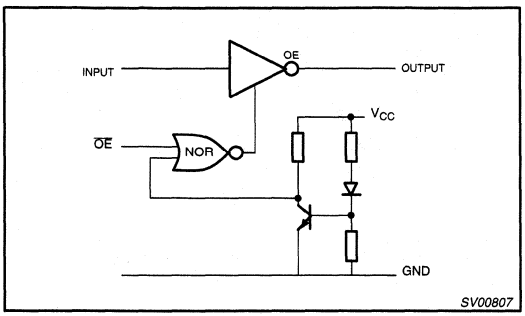


Figure 2. Power-up state

3.2 Bus Hold

All LVT and ALVT products have integrated bus hold inputs. A bus hold circuit allows CMOS input pins to be left open: the input is always defined to be LOW or HIGH via the small MOS transistors that serve as dynamic pull-up or pull-down resistors.

To allow 5V on the inputs, a Schottky diode is inserted between input and the PMOS transistor, blocking any current V_{CC}, even when the part is powered down.

For more information about bus hold circuits, see Reference #1.

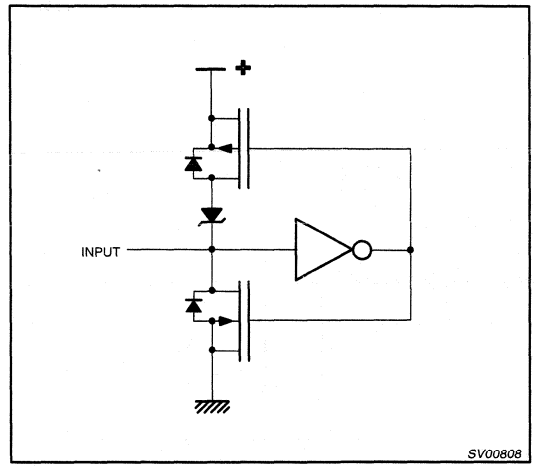


Figure 3. Bus Hold circuit

3.3 Interfacing with 5V systems

Special measures have been taken to allow easy interfacing with existing 5V systems. First, the input circuits are designed without a diode to V_{CC} so that all inputs are 5V tolerant.

For outputs on shared busses there may be a problem with the diode normally existing between drain and backgate/source of the pull-up PMOS (M4 in Figure 1). This diode current path has been blocked by replacing the normal short circuit between source and backgate with a Schottky diode (see Figure 4).

Also, special output overvoltage protection has been implemented. The output voltage is compared to V_{CC}, and when the output is approximately 0.4 to 0.5V higher than V_{CC} the output is automatically put into 3-state. In this way an overvoltage on the output will not lead to high currents from output to V_{CC}, and the device is fully protected.

The current flowing into the output for our parts and competitors' products is given in Figure 5. Above V_{CC} + 0.5V, LVT and ALVT interrupt the current from the output to V_{CC}. It should be noted that typically 20 to 30 mA must be delivered into the output before the overvoltage protection is activated.

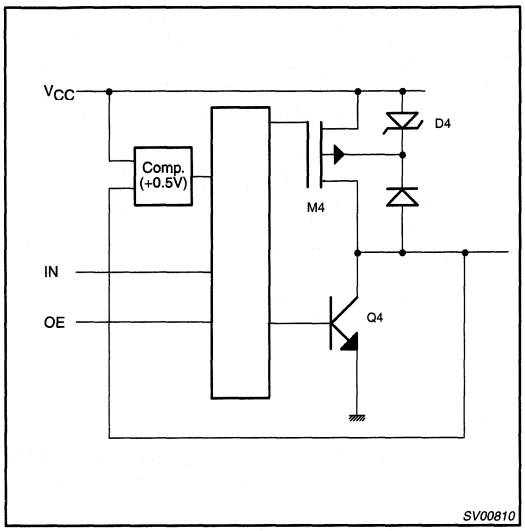


Figure 4. 5V tolerant output

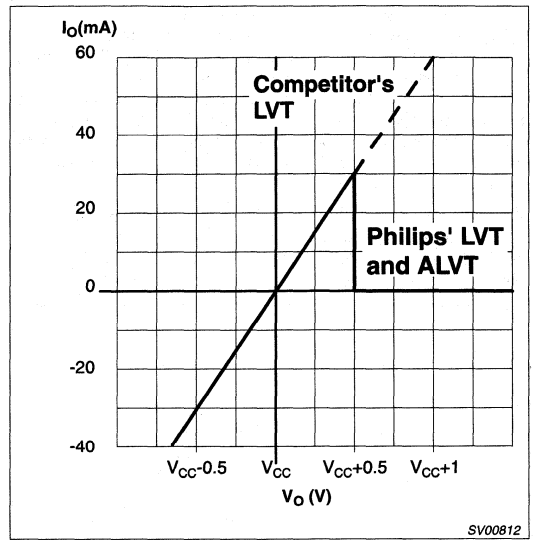


Figure 5. Output current with $V_O > V_{CC}$

More information about interfacing between 3V and 5V systems is available in an Application Note AN240 (Reference #2).

It should be noted that the 5V tolerant features built into LVT and ALVT also play a role during powering-up or-down, since they prevent any current to flow into the output pins when powered-down.

4 SPECIAL INFORMATION

The LVT and ALVT datasheets give characteristics of certain special properties that are unique for both families.

Table 3. Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	T_{amb} (°C) −40 to +85			UNIT
			MIN	TYP	MAX	
V_{RST}	Power-up output LOW voltage	V_{CC} = 3.6V; I_O = 1 mA; V_I = GND or V_{CC}	–	–	0.55	V
I_{OFF}	Output OFF current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V	–	–	±100	μA
I_{HOLD}	Bus hold current A or B outputs	V_{CC} =3.0V; V_I = 0.8V	75	–	–	μA
		V_{CC} =3.0V; V_I = 2.0V	–75	–	–	
I_{EX}	Current into an output in the HIGH state when $V_O > V_{CC}$	V_{CC} =3.0V; V_O = 5.5V	–	–	125	μA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V, outputs HIGH. V_I = V_{CC} or GND; I_O = 0	–	–	0.12	mA
I_{CCL}		V_{CC} = 3.6V, outputs LOW. V_I = V_{CC} or GND; I_O = 0	–	–	6	
I_{CCZ}		V_{CC} = 3.6V, outputs disabled. V_I = V_{CC} or GND; I_O = 0	–	–	0.12	
$I_{PU/PD}$	Power-up/down 3-State output current	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = don't care	–	–	±100	μA

V_{RST} Applies to parts with storage cells. When all outputs are LOW and V_{CC} is made zero, after power-up the outputs are still LOW.

I_{OFF} Specifies the current flowing into the output when the supply voltage is zero (power-down mode). The output may even be pulled to higher voltages than the nominal V_{CC}.

I_{HOLD} Bus hold current at the TTL input levels.

I_{EX} Gives the current into the output when the output is pulled to a voltage higher than V_{CC}. Useful for mixed mode 2.5/3.3/5V applications.

I_{CCH} When the output is high, a current is still drawn from the supply for the automatic 3-state circuit (see Section 3).

I_{CCL} I_{CCL} is higher than I_{CCH}, since a base current flows when the output is forced active LOW (see Section 3); its value is rather low owing to the Power-On-Demand circuitry.

I_{CCZ} See comment above for I_{CCH}.

$I_{PU/PD}$ Maximum current into the output when powering up or down. This parameter is valued for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC} = 1.2V to V_{CC} = 3.3V ±0.3V a transition time of 100 µs is permitted.

The ALVT datasheet contains additional data specifying AC and DC characteristics for a supply voltage of 2.5V (2.3–2.7V). Other relatively new characteristics are skew and data referring to the effects of dynamic thresholds (see section 5.1).

5 TREND CURVES FOR ALVT16245

The ALVT16245 datasheet is of great help in gaining more insight into the part's behavior due to a number of extra curves. These curves include the following:

5.1 Dynamic Thresholds

Due to some internal effects, depending on drive and loading conditions, the normally static values of V_{IL} and V_{IH} change under dynamic conditions. For parts with low output drive, such effects were usually ignored, but for high output drive parts, such as ALVT, it is useful to know how these values may change. For instance, better noise margin targets may be set due to high capacitive loading that negatively affects the input thresholds. Figures 6 and 7 give the dependency of the dynamic threshold voltages on V_{CC} and switching frequency.

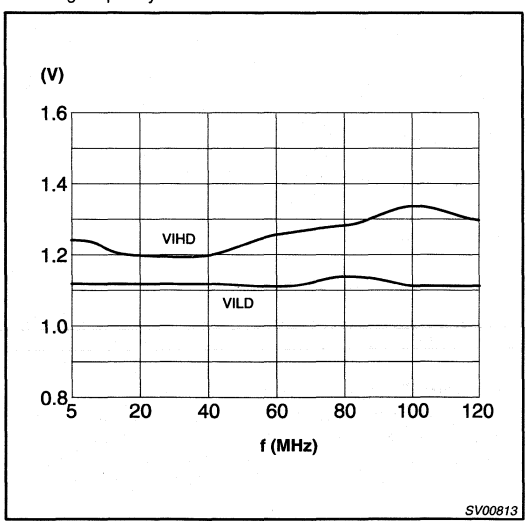


Figure 6. VILD/VIHD f (MHz)

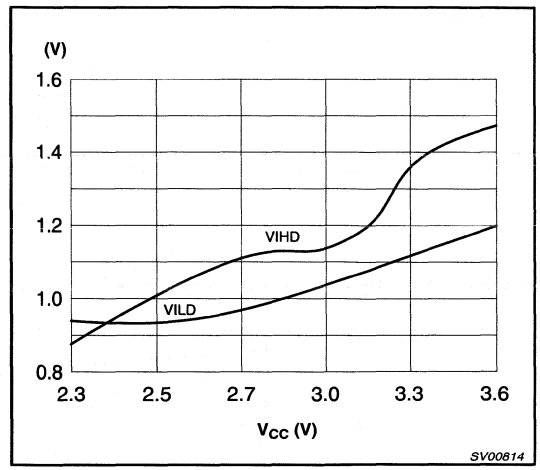


Figure 7. VILD/VIHD V_{CC} (V)

5.2 Ground Bounce

LVT and ALVT are designed so that an optimum is reached between both propagation delay and ground bounce. As we know, this represents a trade-off: higher speed parts will exhibit more ground noise. Figures 8 and 9 show that at higher capacitive loads a lower ground bounce is observed due to the optimized bipolar output stage and the delayed PMOS (see Section 3). Also, the dependency of ground bounce on the number of outputs switching has been minimized.

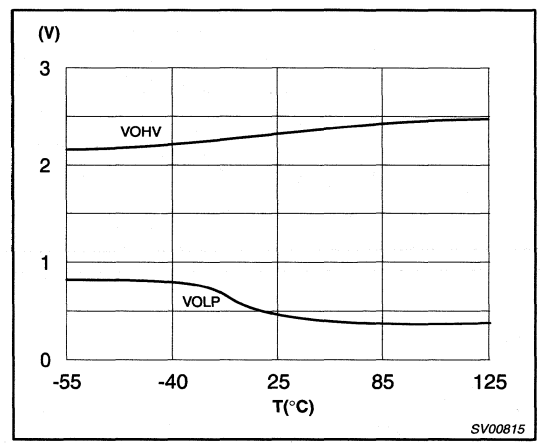


Figure 8. Bounce Temperature (°C)

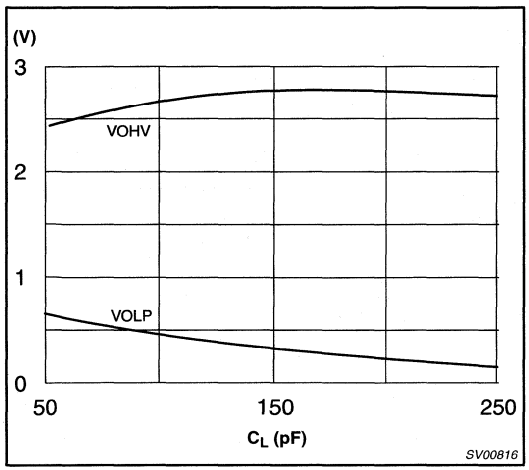


Figure 9. Bounce C_{LOAD} (pF)

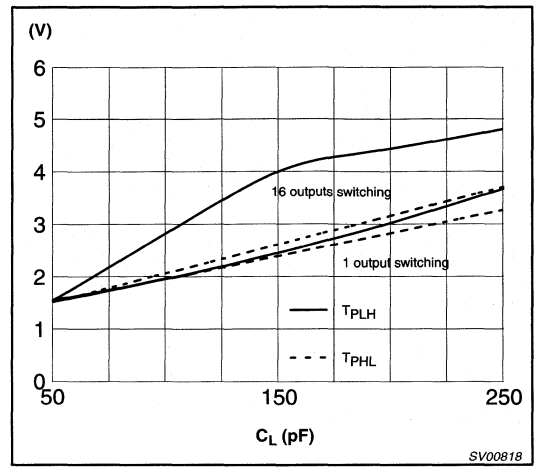


Figure 11. T_{PLH}/T_{PHL} (CL and O/P's switching) C_{LOAD} (pF)

5.3 Propagation Delays

The temperature dependency of the propagation delay times (Figure 10) is excellent due to optimum use of components available in QUBiC. Due to ground bounce, the delay time depends on the number of outputs switching simultaneously. For LVT and ALVT this is kept to a minimum by using a good balance between ground bounce and delay times as shown in Figures 11 and 12.

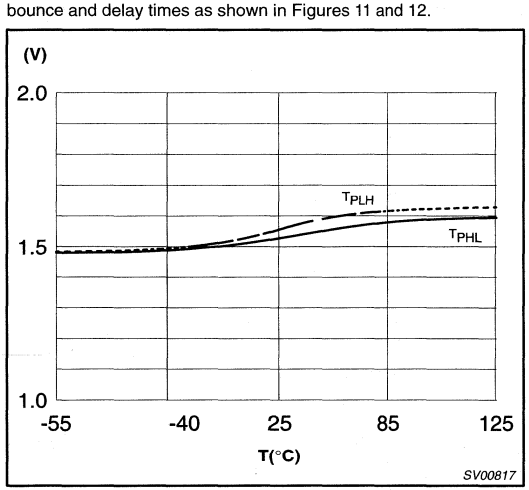


Figure 10. T_{PLH}/T_{PHL} Temperature (°C)

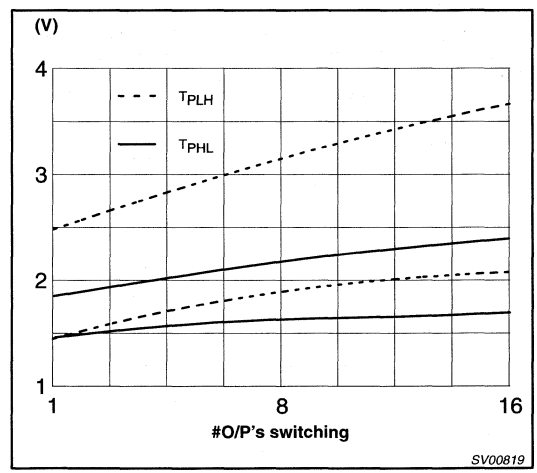


Figure 12. T_{PLH}/T_{PHL} (# O/P's switching)

5.4 Skew Characteristics

The propagation delay times are very short, so we decided to add skew characteristics for a variety of conditions, for example, the spread of propagation delays within one part and over various parts of the same type number. A further explanation can be found in Databook IC23 (Reference #3).

6 DESIGNING WITH LVT/ALVT

The drive capability has been assessed in a backplane application. Figure 13 shows how a 74LVT244 behaves when driving a backplane with an impedance of around 30Ω. Notice the relatively sharp edges due to the fact that the transmission line has a low capacitance and behaves much like a real load.

SPICE models for optimizing your design with LVT and ALVT are available for some platforms such as Berkeley SPICE, PSPICE and HSPICE. The latest models can always be found on the WWW (see cover). SPICE is an essential tool for studying signal integrity and for analysis of the behavior of a system with extreme devices.

To minimize board space, all parts are available in a variety of packages including TSSOP (Thin Shrink Small Outline Package) while for the future also TVSOP (Thin Very Small Outline Package) with a 0.4mm pitch is in the planning stages for 1998.

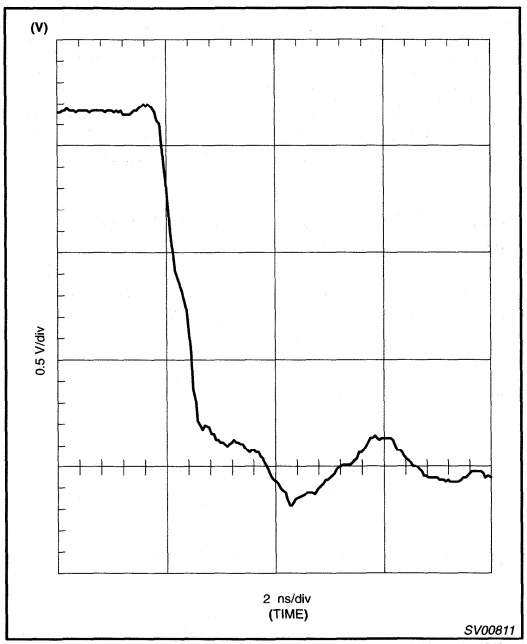


Figure 13. LVT driving 30Ω transmission line, H to L transition

7 SUMMARY

Both LVT and ALVT logic families are state-of-the-art logic families, optimized for use as backplane drivers. These parts combine very fast switching with low power dissipation. The clever design makes them an ideal choice for use in backplanes in high-end EDP and telecom applications. In other areas also where very short propagation delays are a must, both families excel. Added features such as automatic 3-state when the part's output is tied to a higher voltage make them an ideal choice in many mixed mode 3V – 5V systems.

8 ACKNOWLEDGEMENTS

We would like to acknowledge Tom Parkinson, Alan Glaus and Mike Magdaluyo for their help on this Application Note.

9 REFERENCES

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Transmission lines and terminations with Philips Logic families

AN246

Author: Mike Magdaluyo, Logic Products Group

INTRODUCTION

With increasing systems speeds and faster logic families, interconnect characteristics have become significant. The signal transition times of faster families can increase transmission line effects on printed circuit board traces and cables. If not taken into consideration, signal degradation can cause data errors in a system.

Previous logic families with slower rise and fall times such as LS and HCMOS were not as severely affected by this issue if line lengths were not too long. For example, an HCMOS buffer with a 5 ns edge will start exhibiting transmission line effects when a circuit board trace is longer than a foot. However, with newer families, even relatively short trace lengths become very important. This application note will briefly review transmission line concepts and evaluate transmission line effects with Philips 5 volt and 3 volt BiCMOS and CMOS logic families such as ABT, AC(T), ALVC, LVC, LVT, and ALVT.

For more detailed information on transmission lines, there are many other resources to refer to. The terms line or transmission line will refer to a cable or printed circuit trace medium and will be regarded as equivalent for electrical purposes, though their construction varies in real applications.

CRITICAL LINE LENGTH

An interconnect is considered electrically long when the round trip propagation delay of the interconnect from the driver to the load is equal to or greater than the transition time of the driver's rise or fall time. At this point, transmission line effects become significant. Using 160ps per inch as a nominal propagation delay for 50 Ω stripline medium and a nominal 0.9 ns rise time for a lightly loaded ABT driver with 15 pF loading, the critical line length is

Eq. 1

$$\text{Critical line length} = 2 \times \frac{t_{pd}}{t_r}$$

$$= 2 \times \frac{160 \text{ ps / in.}}{0.9 \text{ ns}}$$

$$= 2.8 \text{ in.}$$

For this example, traces shorter than this can be treated as lumped elements. Traces equal to or longer than this length should be modeled as distributed elements. Table 1 shows critical line lengths at various line impedances for different Philips' logic families. Assumptions are light loading of 15 pF and a nominal 8 nH per inch characteristic inductance for a PC board trace. Formulas to determine line impedance are shown in the following section.

Table 1. Maximum trace length in inches with 15pF loading

Family	tr ns	tf ns	100 Ω	70 Ω	50 Ω	35 Ω	25 Ω
HC	2.9	2.9	18.1	12.7	9.1	6.3	4.5
AHC	2.1	1.6	10.0	7.0	5.0	3.5	2.5
AC	1.2	1.7	7.5	5.3	3.8	2.6	1.9
ALS	2.7	1.7	10.6	7.4	5.3	3.7	2.7
FAST	4.0	1.4	8.8	6.1	4.4	3.1	2.2
ABT	0.9	1.2	5.6	3.9	2.8	2.0	1.4
LVT	0.8	0.6	3.8	2.6	1.9	1.3	0.9
ALVT	0.8	0.7	4.4	3.1	2.2	1.5	1.1
LVC	1.8	1.8	11.3	7.9	5.6	3.9	2.8
LV	2.9	2.9	18.1	12.7	9.1	6.3	4.5
ALVC	1.2	1.1	6.9	4.8	3.4	2.4	1.7

As you can see, using faster edge families even with relatively short traces still requires consideration of transmission line effects.

CHARACTERISTIC LINE IMPEDANCE AND CAPACITIVE LOADING

A transmission line has distributed series inductance and distributed capacitance throughout its length, and can be modeled as shown in Figure 1. The line has characteristic inductance and capacitance per unit length, l, where L_O is in Henries per inch, and C_O is in farads per inch.

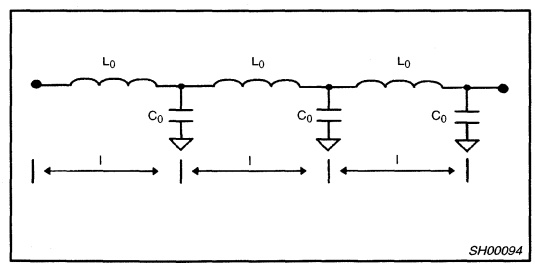

Figure 1. Circuit equivalent for a transmission line

Typical characteristic impedances on PC boards can be from 50 Ω to 100 Ω. The impedance can be determined by

Eq. 2

$$Z_O = \sqrt{\frac{L_O}{C_O}}$$

where L_0 and C_0 are the characteristic inductance and capacitance per unit length of the trace.

The line propagation delay can be determined by

Eq. 3

$$T_O = \sqrt{L_O C_O}$$

Distributed capacitive loads lower the effective impedance of a transmission line and increase the line propagation delay. Consider a bus structure with equally spaced loads of the same value as in Figure 2. The capacitors represent the input capacitance of each receiver.

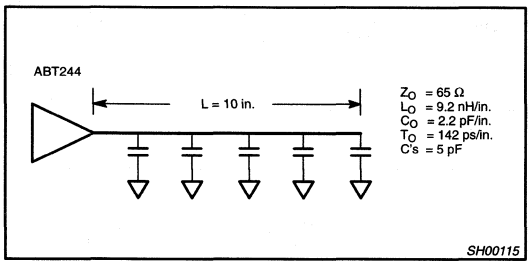

Figure 2. Equally spaced capacitive loads

If the driver's rise or fall time is longer than the electrical length of the spacing between the loads, the effects of individual capacitors distribute evenly across the waveform edge. This adds capacitance to the line's characteristic capacitance. The board interconnect at the receiver pin has capacitance also: via, connector, etc., and the values are added to the receiver's capacitance to form a lumped value. Suppose the interconnect capacitance is 5 pF, then the lumped distributed capacitance is 10 pF per every 2 inches or 5 pF per inch. The new line impedance, Z_O', can be calculated and will be

Eq. 4

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_{LU}}{C_O}}}$$

$$= \frac{65\ \Omega}{\sqrt{1 + \frac{5\ \text{pF/ in.}}{2.2\ \text{pF/ in.}}}}$$

$$= 36\ \Omega$$

where C_{LU} = load capacitance per unit length, pF/in.

Likewise, the new line propagation delay will be

Eq. 5

$$T_O' = T_O \times \sqrt{1 + \frac{C_{LU}}{C_O}}$$

$$= 142\ \text{ps/in.} \times \sqrt{1 + \frac{5\ \text{pF/ in.}}{2.2\ \text{pF/ in.}}}$$

$$= 257\ \text{ps/in.}$$

Since the effective line impedance can be reduced with more loading, a driver with sufficient source and sink capability should be chosen to drive that particular impedance. This is discussed in the next section.

INCIDENT WAVE SWITCHING AND DRIVER I-V CHARACTERISTICS

When launching a pulse down the line, the driver needs sufficient current to change the voltage on the line. For TTL level input receivers, the guaranteed V_{IH} and V_{IL} levels are 2.0 V and 0.8 V. This means that the leading edge incident wave launched down the line should meet those levels to switch all receivers on the line and switch them only once. The drive current required is

Eq. 6

$$I_{AV} \text{ at } V_{OH} = \frac{V_{IH}\ \text{min} - V_{OL}\ \text{typ}}{Z_O'}$$

Eq. 7

$$I_{AV} \text{ at } V_{OL} = \frac{V_{OH}\ \text{typ} - V_{IL}\ \text{max}}{Z_O'}$$

As an example of incident wave switching capability, refer back to the bus structure in Figure 2. The effective line impedance is 34 Ω. Using Equations 6 and 7, the drive current required to switch the line is determined as follows:

$$I_{AV} \text{ at } V_{OH} = \frac{V_{IH}\ \text{min} - V_{OL}\ \text{typ}}{Z_O'}$$

$$= \frac{2\ \text{V} - 0.2\ \text{V}}{36\ \Omega}$$

$$= 50\ \text{mA}$$

and

$$I_{AV} \text{ at } V_{OL} = \frac{V_{OH}\ \text{typ} - V_{IL}\ \text{max}}{Z_O'}$$

$$= \frac{3.4\ \text{V} - 0.8\ \text{V}}{36\ \Omega}$$

$$= 72\ \text{mA}$$

ABT products are rated for +32 mA source current at 2 V and –64 mA sink current at 0.55 V. By referring to I-V curves you can determine if the dynamic drive current is enough to switch the line on the incident wave. From the following curves in Figures 3 and 4, note that the –76 mA at 2 V and +167 mA at 0.8 V satisfies the requirements in the above formulas. To compare the drive strength of other product families, Figures 5 through 9 show IOL and IOH currents for a typical '244 driver for the ABT16, ALVC, ALVT, LVC, LVT, and LVT16 families.

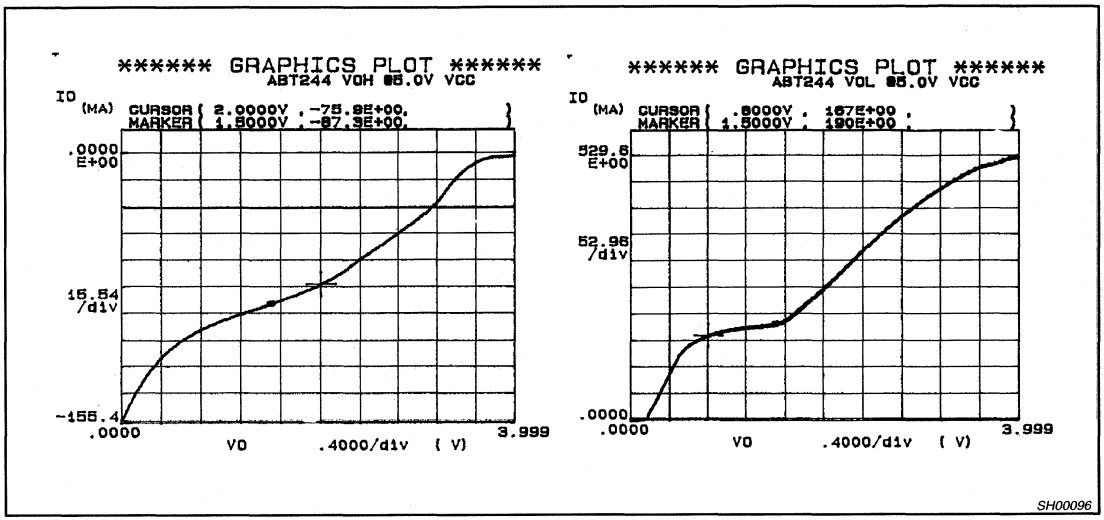

Figure 3. ABT244 I-V curves

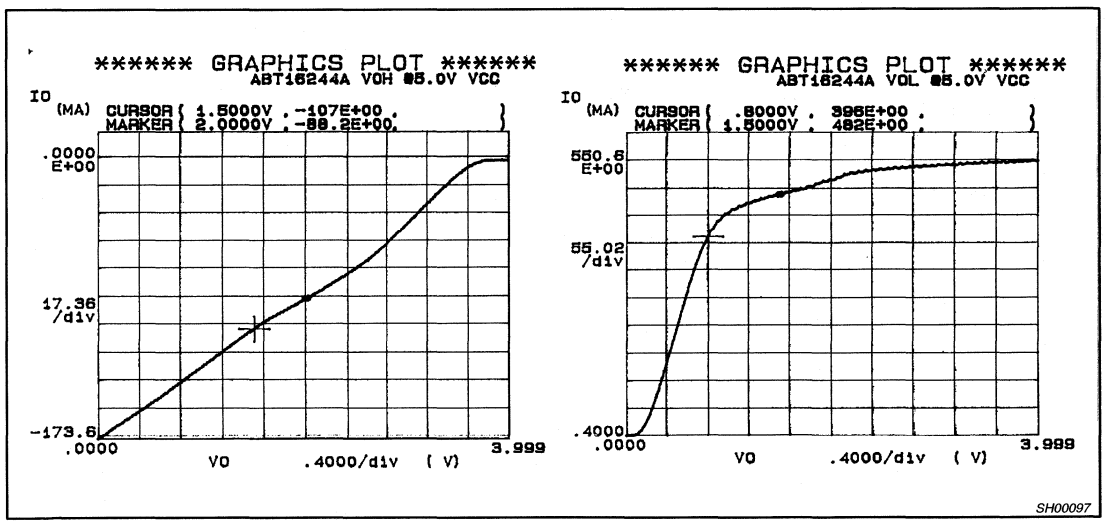

Figure 4. ABT16244 I-V curves

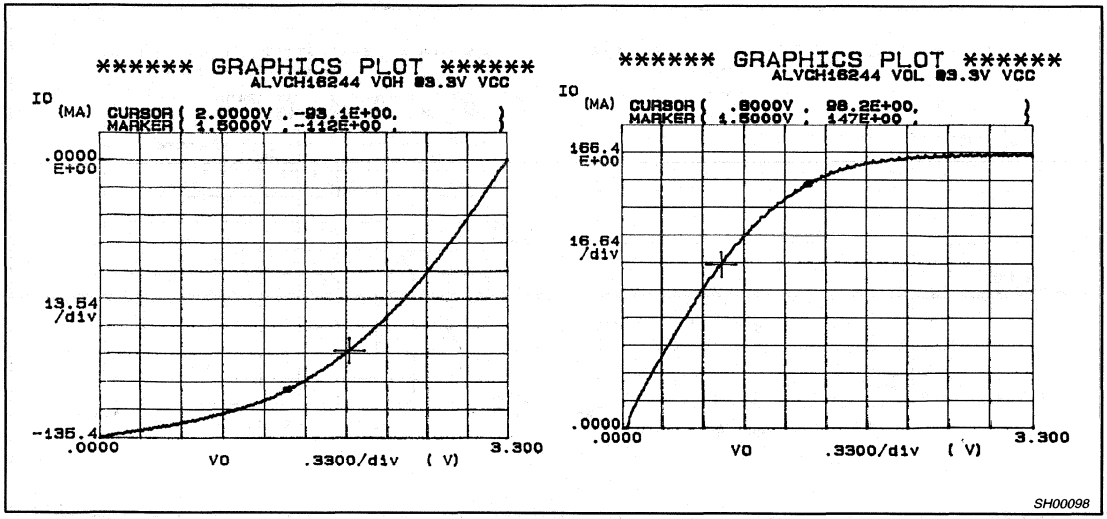

Figure 5. ALVC16244 I-V curves

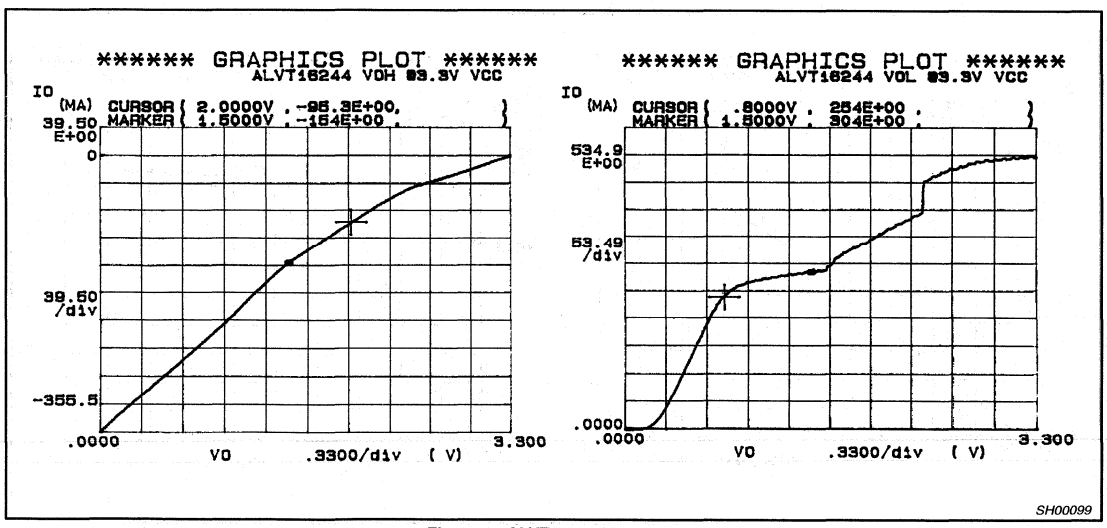

Figure 6. ALVT16244 I-V curves

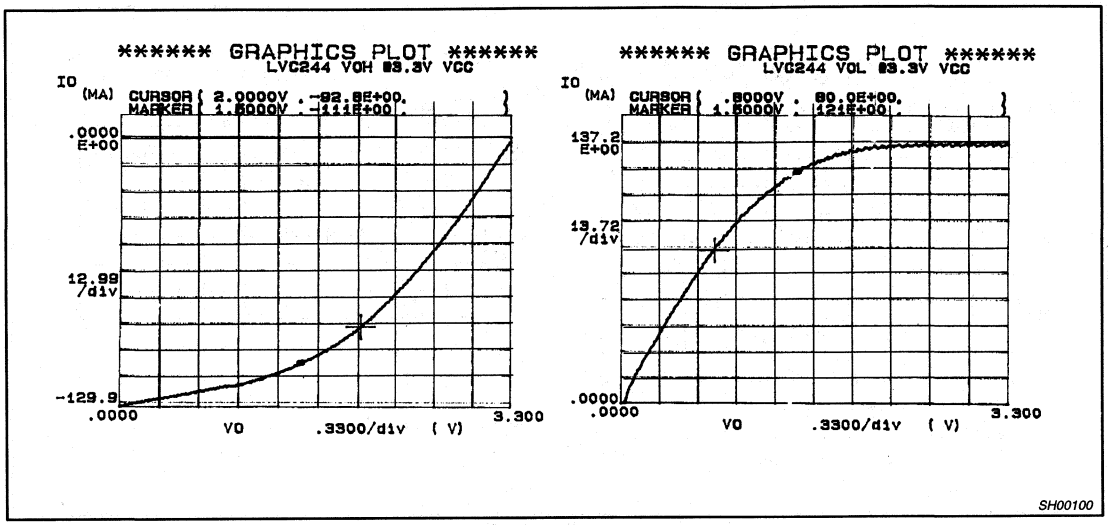

Figure 7. LVC244 I-V curves

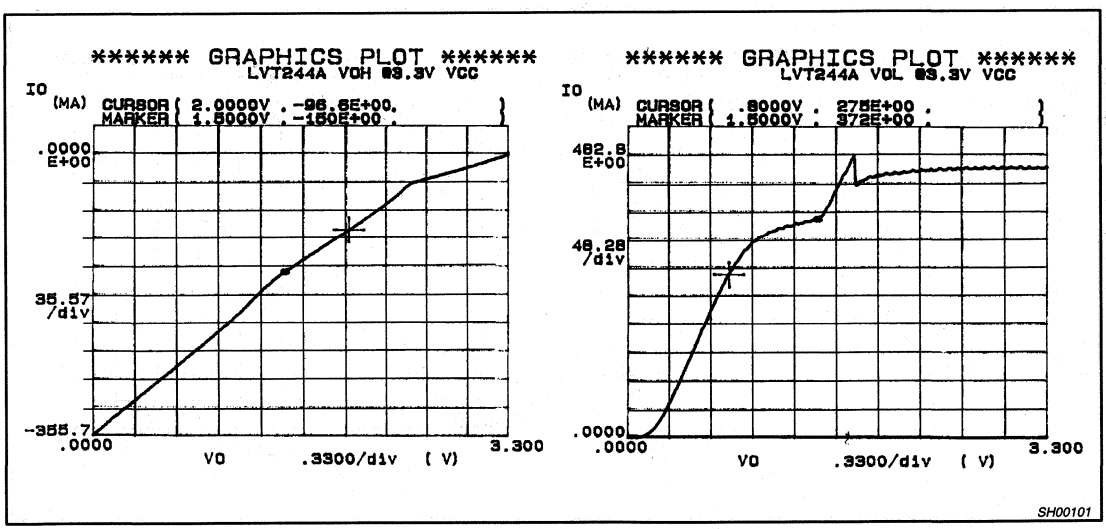

Figure 8. LVT244 I-V curves

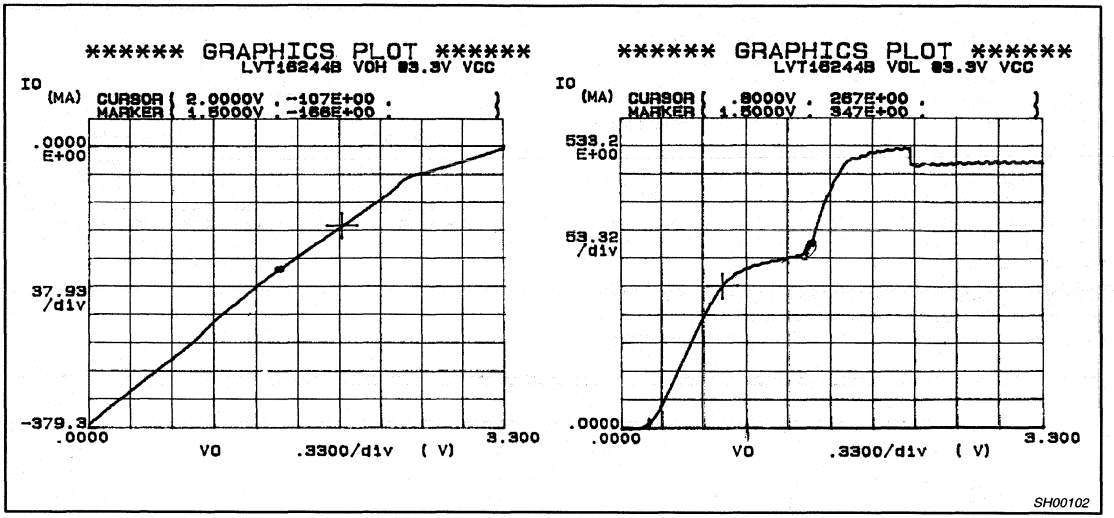

Figure 9. LVT16244 I-V curves

Based on the I-V curves, all families have good drive current in the logic high state, and ABT(16), ALVT, and LVT(16) BiCMOS families have considerably stronger drive than the other families in the logic low state. The BiCMOS families have been optimized to drive backplanes. The other CMOS families are suitable for local buses and driving point-to-point loads. The following table shows recommended minimum line impedances that can be driven by the buffer/drivers of various Philips logic families:

Table 2. Minimum line impedance for logic families

Logic Family	Minimum Z_O
ABT(16)	35 Ω
AC/ACT	50 Ω
ALS(–1)	65 Ω
FAST	50 Ω
LVT(16)	35 Ω
ALVT	35 Ω
LVC(16)	50 Ω
ALVC	50 Ω

REFLECTIONS FROM IMPEDANCE MISMATCHES

Since a driver has non-zero output impedance, its impedance along with the line impedance form a voltage divider. The incident wave launched down the line is a portion of the driver's voltage. When the wave encounters an impedance change from either the line or a receiver input, a portion of the wave is reflected back towards the driver ($V_{reflected}$) which is determined by the reflection coefficient r. The reflected portion is also added to the incident wave which continues propagating down the line ($V_{transmitted}$). The relationship of these voltages are shown in the following equations:

Eq. 8

$$\rho = \frac{(Z_{load} - Z_O)}{(Z_{load} + Z_O)}$$

Eq. 9

$$V_{reflected} = V_{incident} \times \rho$$

Eq. 10

$$V_{transmitted} = V_{incident} + V_{reflected}$$

Since driver and line impedances are usually mismatched, a reflection occurs at the driver and travels back towards the load. The reflection coefficient at the driver is determined by Equation 11:

Eq. 11

$$\rho = \frac{(Z_{driver} - Z_O)}{(Z_{driver} + Z_O)}$$

This volley of wave reflections continues, with reflections getting smaller as the signal waveform settles.

During the reflection period, the waveform may have a stairstep response—in the case of a driver's impedance higher than the line's—or it may have a "ringy" response—in the case of a driver's impedance lower than the line's. To predict the signal integrity of a waveform you can use reflection charts or Bergeron plots, but they can be cumbersome.

Another tool that is useful for evaluating these effects is SPICE models. Philips Semiconductors offers free models for our FAST, ALS, HCMOS, ABT, ABT16, ALVC, ALVT, LV, LVC, LVT, and LVT16 product families to aid in signal integrity evaluation. The models help reduce design time by eliminating time consuming efforts of reflection and Bergeron diagrams, and they also help predict signal integrity prior to board layout.

As an example, the circuit in Figure 10 was modeled and the results are shown in Figure 11. A pulse was fed into the ALVC16244 and the input and output waveforms were observed. This example illustrates the effect of reflections due to the mismatch of the driver impedance (around 10 Ω) and the transmission line.

Note that the overshoot and undershoot in Figure 11 may not be acceptable to drive other 3V device inputs or DRAM's. To reduce the overshoot and undershoot, line termination will be necessary.

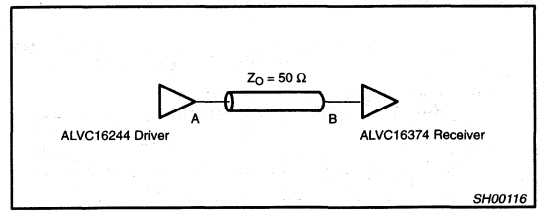

Figure 10. ALVC16244 driving ALVC16374 receiver

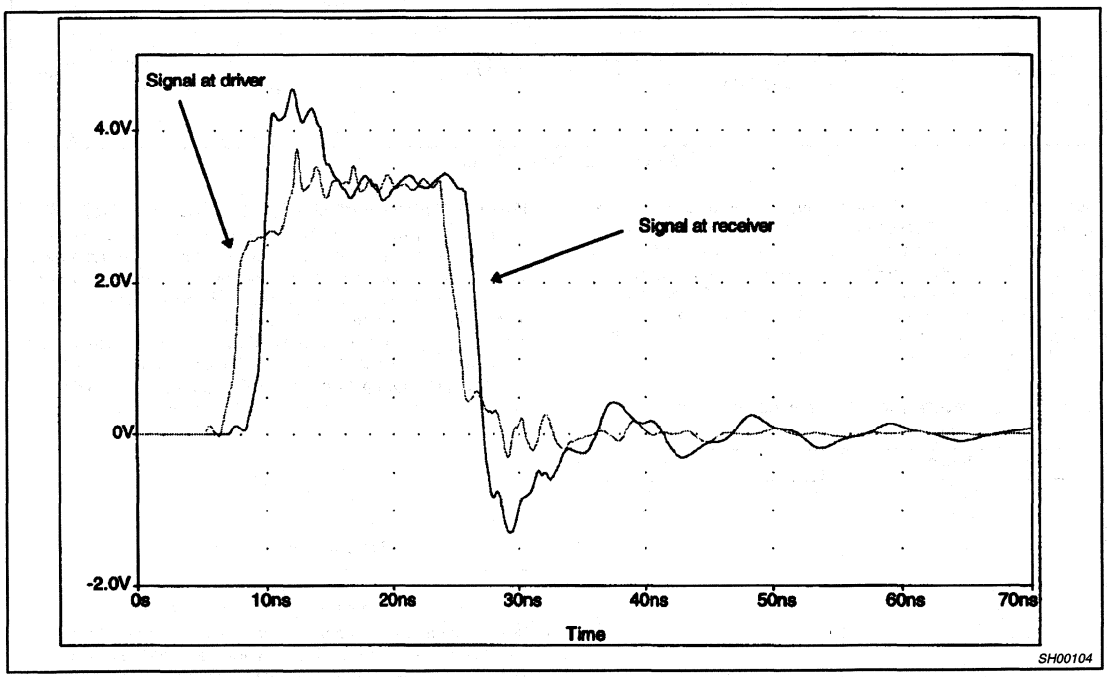

Figure 11. SPICE simulation for the circuit in Figure 10.

TERMINATION CONSIDERATIONS AND TECHNIQUES

As shown earlier, impedance mismatches between the source, line and load can cause reflections. These reflection can cause signal delays, such as the case of a stairstep type of response which requires additional line delays to reach sufficient switching threshold levels, mis-clocking from non-monotonic edges, or excess voltage/current on inputs. A signal should be terminated if it won't settle on time, if it produces overshoot or undershoot that violates the receivers input voltage or current ratings, or if it drives edge-sensitive asynchronous inputs and has non-monotonic edges. Several termination schemes can be used depending on drive current capability, power dissipation requirements, and incident wave switching requirements.

There are two basic approaches to line termination: source termination and end termination. Both schemes will result in a stable signal at the far end of the line after one line delay. Source termination, however, results in a stable signal up to two line delays for loads at intermediate points on the line and at the source. More details of each scheme follows.

Source Terminations Methods

Figure 12 shows the configuration of a source terminated daisy chain line.

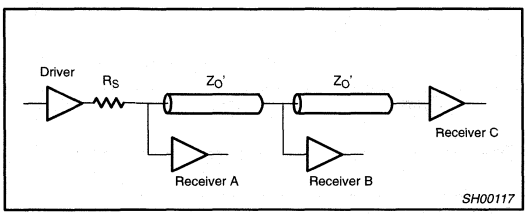

Figure 12. Source termination configuration

The concept of this termination method is to try and match the loaded line impedance with the sum of the driver output and series resistor impedances. The series resistor value is equal to Z_O' minus the driver impedance. The resistor should be located as close to the driver as possible.

Since the sum of the driver impedance and series resistor equals the line impedance, a half-height wave travels down the line from the voltage divider effect. Assuming a reflection coefficient approaching +1 at the end of the line, the reflection adds to the half-height wave, and the voltage at the last receiver is at near full amplitude. The wave amplitude at the first and intermediate receivers, however, are half-height and require up to one additional line delay for the reflected wave to reach the series terminator and add to the initial wave. Figure 13 shows a SPICE simulation of the reflections for this circuit and termination method.

Note that the last receiver is first to switch to the full signal amplitude, while the first receiver is the last to reach full amplitude. This means that any edge-sensitive asynchronous signals should be located at the end of the line. Non-monotonic edges at the beginning and intermediate points along the line could cause false clocking of devices. Also, drivers at the beginning and at intermediate points need to be able to tolerate roughly twice the settling time.

As you can see, this termination method is not very good for lines with daisy chain topologies. Source terminators work well, though, for single receiver, point-to-point loads and star type of topologies. They work well to dampen overshoot and undershoot.

Source terminators dissipate no quiescent power. The AC power dissipation can be estimated by:

Eq. 12

$$P \approx f_{2T}\left(\frac{\Delta V}{2R}\right)^2$$

where f = pulse frequency
where T = one-way line delay
ΔV = V_{OH}–V_{OL}
R = termination resistance

This approximation works if the pulse interval is greater than twice the line delay. For shorter pulse intervals, you can assume a worst case of DV/2 across the termination resistor at all times. With its low power dissipation, series termination is recommended for low voltage logic.

As mentioned previously, the sum of source impedance and the series terminator should match the loaded line impedance. Since output impedances are different in the logic low and high states, there needs to be a compromise when choosing the termination resistance. It's probably better to slightly overdrive the line by choosing a smaller resistor to ensure fast enough edge transitions to a valid logic level. Typical values in applications range from 22 Ω to 33 Ω. Philips offers ABT, ALVC, ALVT, LVC, and LVT parts with built-in series terminators that have equivalent output impedances of 30 Ω. These parts save board space by eliminating the need for a terminating resistor. Part types are designated by a "2" prefix before the part type number, e.g., 74ABT2245.

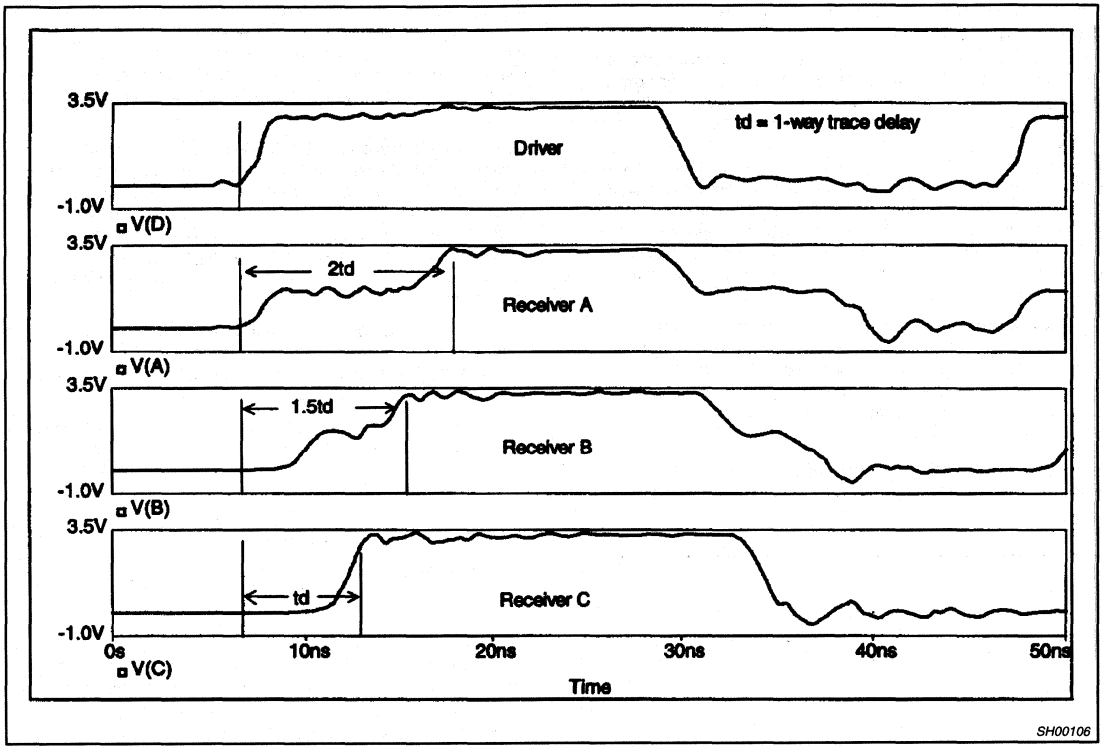

Figure 13. Reflections from source termination

Other Series Termination Schemes

Figure 14 shows a series termination used with a star stub topology.

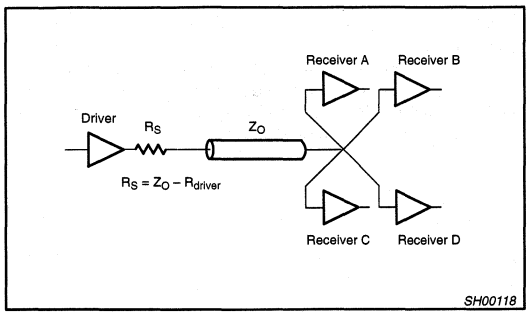

Figure 14. Series termination with star stub routing

Stub electrical lengths should be very short, about 10% of the signal edge, to prevent reflections. This method is useful for terminating clocks and other asynchronous signals if stubs are of equal length/delay. Terminating methods for some alternative star routing is shown in Figure 15.

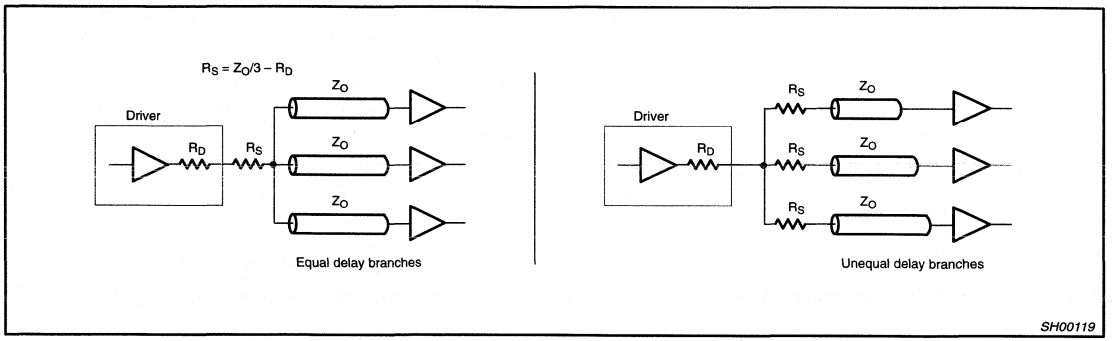

Figure 15. Series termination for alternate star routing

Figure 16 shows another method of series termination.

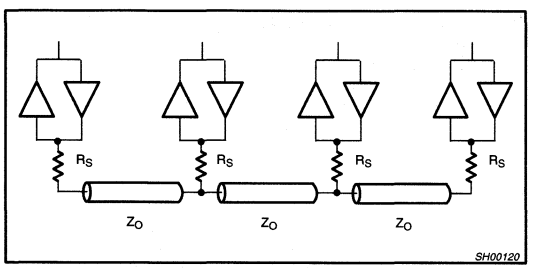

Figure 16. Series stub termination

Note that the drivers at the end will be driving RS + Z_O. Drivers in the middle should be strong enough to drive RS + Z_O/2. Again, keep stub lengths short.

End Terminations

End terminated line are recommended for distributed loads, and several methods can be used such as parallel, AC, and diode clamp methods. Figure 17 shows two parallel termination schemes.

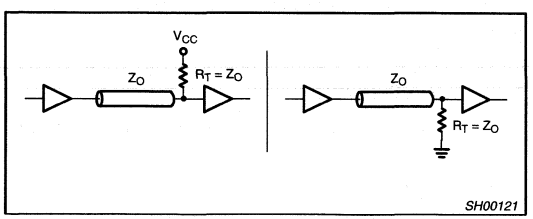

Figure 17. Parallel terminations

With this method, the termination resistance is matched to the effective line impedance. The advantage is that this method allows for incident wave switching. The disadvantages are that you need an extremely strong driver and it consumes high static power.

To reduce the drive requirements and power dissipation for this configuration, a more practical parallel Thevenin termination is shown in Figure 18 can be used.

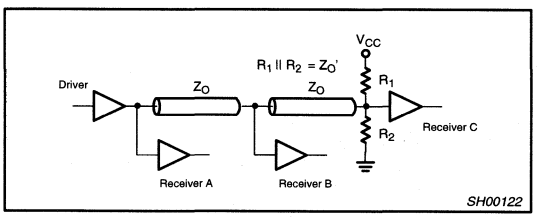

Figure 18. Daisy chain topology with split resistor Thevenin termination

This method is suitable for ABT, LVT, and ALVT families but not recommended for low voltage CMOS logic if power dissipation is a concern. The termination is placed at the end of the line as close to the receiver as possible.

If this termination technique is used on LVC and ALVC drivers, take precaution not to connect the pull-up resistor to a 5 volt supply in a mixed 3 volt/5 volt system. This can cause 5 volt supply current to flow to the 3 volt supply through the upper PMOS transistor's parasitic diode of the driver output during the active high state.

If used on a 3-State bus, avoid biasing the receiver input at its threshold switching voltage which is about 1.5 V for BiCMOS and CMOS TTL level inputs. Inputs left floating around the threshold region can consume excessive current or cause oscillations. You can use the following formula to determine values for R1 and R2 if they are not equal:

Eq. 13

$$R_1 = Z_O \frac{V_{CC}}{V_T} \text{ and } R_2 = Z_O \frac{V_{CC}}{V_{CC} - V_T}$$

where V_T = termination voltage.

A good termination voltage to choose is 2.5 V for TTL thresholds.

Assuming a 50% duty cycle, the average power dissipation of the resistors will be:

Eq. 14

$$P = 0.5 \times \left(\frac{V_{OH}^2 + V_{OL}^2}{2R_2} + \frac{(V_{CC} - V_{OH})^2 + (V_{CC} - V_{OL})^2}{2R_1} \right)$$

Another method to reduce quiescent power dissipation is AC termination shown in Figure 19. This method is recommended for distributed loads or when static power consumption is a concern.

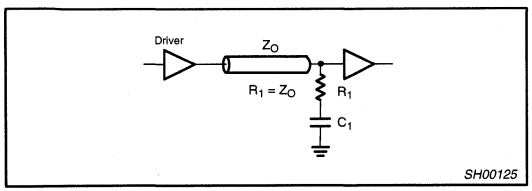

Figure 19. AC termination

No DC current flows during quiescent high or low logic levels, but an AC current path is available through C1 to terminate the line. Choose XC to be a small percentage of Z_O at the operating frequency of:

Eq. 15

$$f = \frac{1}{2T_r}$$

where T_r is the faster of the rise or fall time

Also, for DC balanced signals with 50% duty cycle, choose C such that $Z_O C$ is much greater than the pulse period. For DC imbalanced signals, choose C such that $Z_O C$ is much greater than the rise time but much smaller than half the pulse period.

Provided that the duty cycle is 50%, the average voltage across C1 is midway between the driver high and low output levels. R1 will also have half the voltage swing always across it. The power dissipation across R1 will be:

Eq. 16

$$P = \frac{\left(V_{OH} - \frac{V_{OL}}{2}\right)^2}{Z_O}$$

$$= \frac{(V_{OH} - V_{OL})^2}{4Z_O}$$

Another method of end termination is shown in Figure 20.

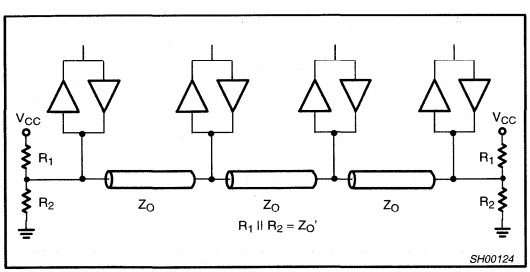

Figure 20. Party bus dual termination

The same principles should be applied to this method as in the Thevenin termination. Note that drivers will need to be strong, such as the BiCMOS devices, since they will have to drive half the value of Z_O.

The last method of end termination discussed in this paper is diode clamp termination shown in Figure 21:

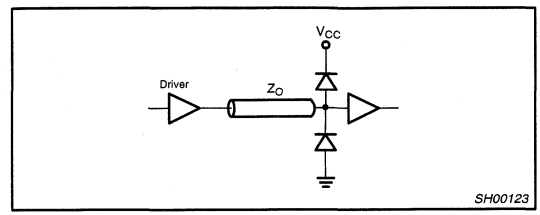

Figure 21. Diode clamp termination

The advantages are that it dissipates no power and it adds no delay to the net. The method is good to clamp overshoot and undershoot provided that it is fast enough to react to the rising or falling edge. The disadvantage is that it won't limit overshoot on 5 volt TTL drivers such as ABT. Also, it can't guarantee monotonicity on weak drivers.

CONCLUSION

Philips Semiconductors offers various advanced CMOS and BiCMOS families for high speed bus applications. This paper discussed aspects of transmission line effects with these families. Critical line length, line impedance, loading, and drive capability of different product families was examined. Impedance mismatches and reflections were discussed along with various termination solutions. Considerations of these various factors will help solve signal integrity issues in a design, and these factors need to be considered with their tradeoffs to satisfy the system design needs.

To help make design efforts easier, Philips Semiconductors offers free SPICE models for our 3V and 5V product families to aid in signal integrity evaluation. The models help reduce design time by eliminating time consuming efforts of reflection and Bergeron diagrams, and they also help predict signal integrity prior to board layout.

ACKNOWLEDGEMENTS

Thanks to Tinus van de Wouw and Jeff West for their help and data.

REFERENCES

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2. James Buchanan, *Signal and Power Integrity in Digital Systems: TTL, CMOS, and BiCMOS.* New York: McGraw-Hill, 1996.
3. Steve Kaufer, *Termination Improves Board Signal Quality.* Electronic Engineering Times: September 2, 1996, p. 44, p. 74.
4. *High Performance ECL Data Book: Design Guide Section,* System Interconnect. Motorola, Inc.: 1993.

The behaviour of integrated bus hold circuits AN2022

Author: Tinus van de Wouw, Philips Semiconductors, Nimegen

INTRODUCTION

The problem with floating or unused CMOS inputs as a general rule is that they must not be left floating otherwise due to gradual charging of the gate input capacitance, they may cause the following:

- There may be a static current flowing through the input stage, causing unnecessary excessive power dissipation.
- When the input voltage reaches the threshold level, the device may start high frequency oscillations causing heat generation that may eventually damage the part.

Therefore, as a standard solution, all unused (open or floating) inputs are simply connected to GND or V_{CC} to prevent these adverse effects.

In certain testing conditions, inputs may be left open, but certainly in bus applications, it may happen that inputs are effectively floating when all devices driving the bus are in 3-state. One should ensure that all inputs are defined "0" or "1" to prevent excessive heat dissipation or unwanted high frequency oscillations.

THE SOLUTIONS

The following are several solutions including their added costs, components counts, and effectiveness:

Static Pull-up/Pull-down Resistors

Static pull-up/pull-down resistors are a solution used very often to define the state of unused CMOS inputs when the bus is not driven by any device. Although these resistors cause additional power dissipation and increase component count, they are very effective. However, when using today's narrow pitch packages such as TSSOP48-56, there may not even be enough space to add these pull-up/pull-down resistors on the PCB.

External Bus Hold Circuit

An external bus hold circuit (see Figure 1) is another solution which uses an inverter and resistor between its input and output. This circuit connects the input to GND or V_{CC} depending on the state of the input and holds the bus in this state, hence its name "bus hold". Although this circuit reduces excessive power dissipation caused by static pull-up/pull-down resistors described earlier, it significantly adds to the component count and costs.

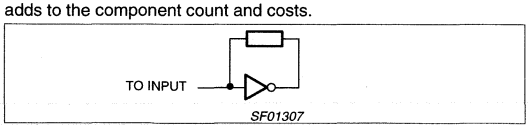


Figure 1. External Bus Hold Circuit

Integrated Bus Hold Circuit

Philips Semiconductors has applied integrated bus hold circuits (see Figure 2) for a number of logic families. Integrated bus hold circuits minimize additional power dissipation and provide additional component count internally at no extra cost for the device.

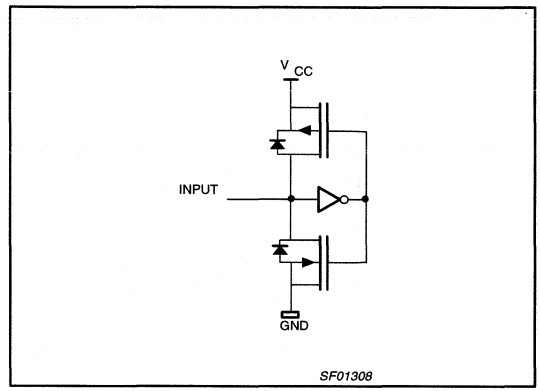


Figure 2. Integrated Bus Hold Circuit

The integrated Bus Hold circuit acts like dynamic pull-up/pull-down resistors as follows:

- When the input is at "0", the output of the inverter is at "1" so that the lower FET is ON and acts like a pull-down resistor.
- Similarly, when the input is at "1", the upper FET is activated and acts like a pull-up resistor.

When the input voltage varies, an input current will flow into or out of the input circuit (see Figure 3), so that when the input voltage rises, the input current will slowly increase, since the lower FET is conducting. Around the threshold level, the upper FET will then start conducting and the lower FET will stop conducting. Then the input current will reverse direction (input current flows out of the integrated bus hold circuit) slowly decreasing until the input voltage is at V_{CC}.

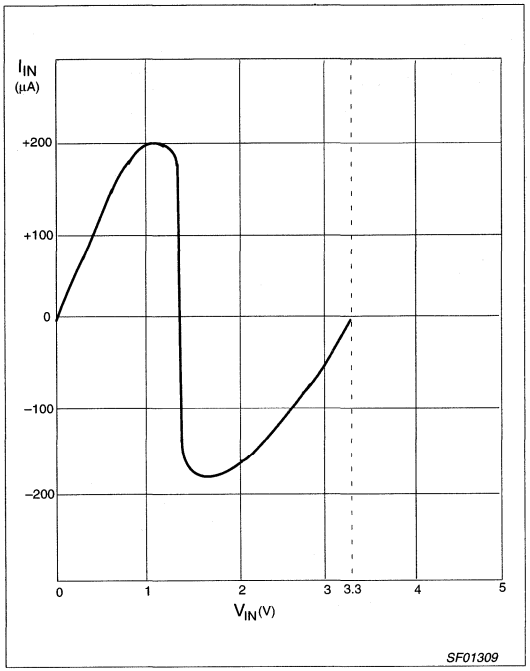


Figure 3. Input Voltage (V_{IN}) vs. Input Current (I_{IN})

Description

The following parameters describe the behaviour of the integrated bus hold circuit:

- IBHL (for LVT called I_{HOLD}) is the bus hold LOW sustaining current, that specifies an input current below which the bus hold circuit is keeping the input voltage lower than the 0.8V TTL switching level.
- Similarly, input current (IBHH), the bus hold HIGH sustaining current will yield an input voltage higher that 2.0V when the input is at "1".
- IBHLO is the bus hold LOW overdrive current. When the input is driven with this current, the input will change from a "0" to a "1".
- Similarly, IBHHO specifies the input current that will change the input from a "1" to a "0".

INTEGRATED BUS HOLD CIRCUITS FOR 5V TOLERANT DEVICES

The circuit discussed in Figure 2 is the integrated bus hold circuit in its basic form as it is used in logic devices such as the ALVC.

However, logic transceiver functions that have 5V tolerant outputs also require the integrated bus hold circuits to be 5V tolerant. For such cases, the bus hold circuits have been provided with additional components to enable bus hold circuits to handle 5V operation.

Philips Semiconductors has provided two such solutions, the bus hold with Schottky diode and with dynamic backgate switching (see Figure 4) as follows:

Bus Hold with Schottky Diode

The standard solution for LVT devices uses a series Schottky diode (see Figure 4), which effectively blocks the current path from the input to V_{CC}.

Bus Hold with Dynamic Backgate Switching

The standard solution for LVCHXXXA devices is called dynamic backgate switching (see Figure 4), where the MOSFET is switched OFF when the input voltage exceeds V_{CC} and the current path through the diode is blocked by some switches.

Both bus hold circuits behave quite differently as shown in the V_{IN}/I_{IN} characteristics (see Figure 5) as follows:

- The input current for LVT (with Schottky diode) becomes zero when the input exceeds ($V_{CC} - V_{Fdiode}$).
- Whereas for LVCHXXXA devices with dynamic backgate switching have a hysteresis effect. When the input voltage exceeds (V_{CC} + 0.6V), the input FET is turned off, so the input current becomes zero. The upper FET is turned on again when the voltage becomes lower than (V_{CC} – 0.6V).

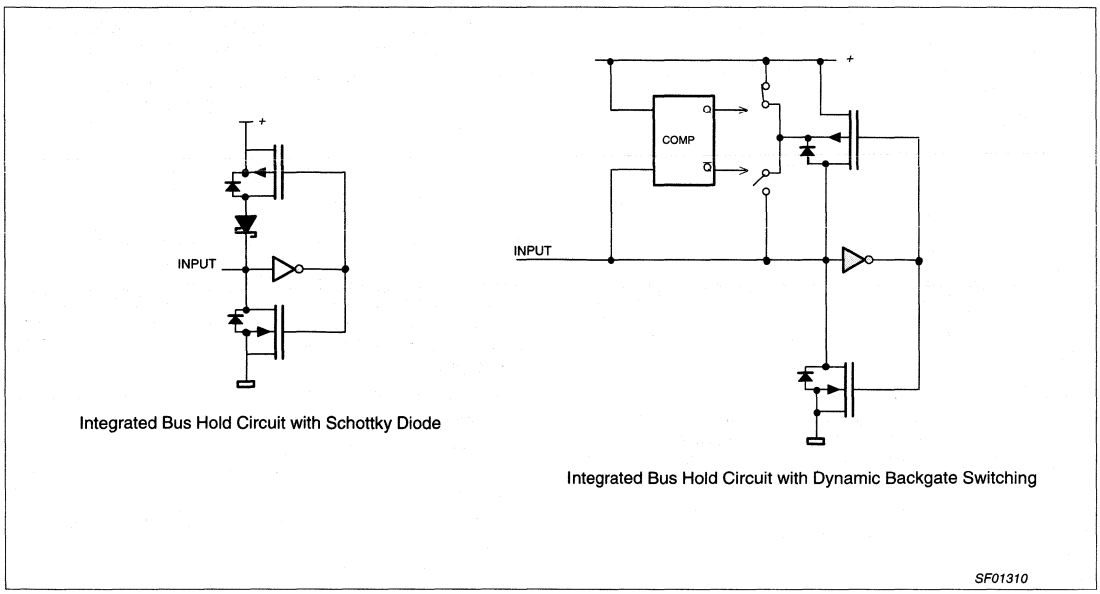


Figure 4. Integrated Bus Hold Circuits with Schottky Diode and Dynamic Backgate Switching

DRIVING A BUS HOLD CIRCUIT

The input current is so low that virtually any part is capable of delivering enough current to toggle quite a number of paralleled inputs. At Philips Semiconductors we have performed tests with one (1) 74LV244 device (with 8mA output drive) driving from 0 to 10 74LVC244As (without integrated bus hold circuits) and compared them with 0 to 10 74LVCH244As (with integrated bus hold circuits). These tests showed that the effects of integrated bus hold circuits on the total propagation delay are negligible.

As a rule of thumb, adding one (1) integrated bus hold circuit gives an extra propagation delay of about 40 ps, so that one (1) LV device driving 10 integrated bus hold circuits will give an extra delay of 0.4ns. Families with a higher output drive will have a propagation delay that is proportionally shorter. For instance, one 74LVC244 (24mA driver) will have an extra propagation delay of about 15ps per integrated bus hold circuit load.

When applying parts with integrated bus hold circuits in backplane buses, where the total current flowing in the bus are so high, the desired effects of integrated bus hold circuits may be negligible. The current that an integrated bus hold circuit can handle is by far insufficient to pull an active bus high ("1") or low ("0"). Only after all reflections are at a minimum can the integrated bus hold circuit become effective. Additionally, for crosstalk situations, the bus hold may be incapable of holding the bus to the required "1" or "0" state.

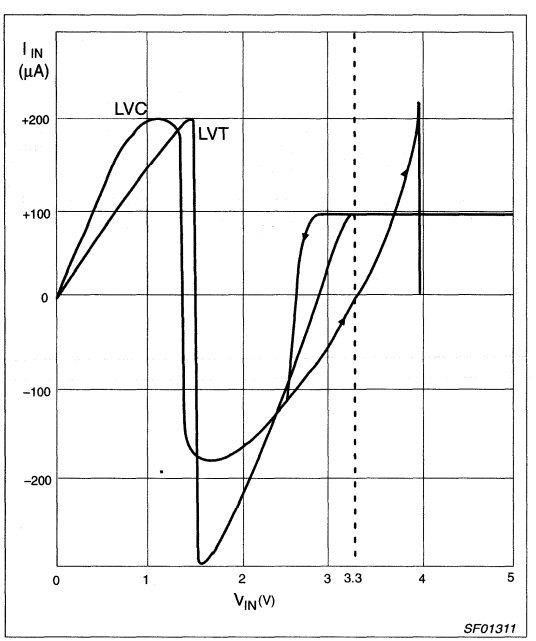


Figure 5. V_{IN} vs I_{IN} for 5V tolerant Integrated Bus Hold Circuits

In some applications, the bus should become HIGH when all outputs driving the bus are in 3-state. In such cases, you should use a termination resistor, (R_T pulled-up to V_{CC}) which is low enough to overrule all the bus holds connected to that circuit. R_T is calculated as follows from equation 1:

EQUATION 1

$$R_T \quad \frac{V_{CC} \quad V_{TH}}{IBHHO}$$

where V_{TH} is the switching level HIGH
IBHHO is the maximum overdrive current; the typical value is about a factor of two lower

Example

With a V_{CC} of 5V, IBHHO = 500μA and TTL switching levels (i.e. V_{TH} = 2V), the termination resistor value should be less than 6kΩ. Therefore, when more inputs are connected to the bus, this value is proportionally lower.

Power Dissipation Effects

Since a bus hold effectively forms a pull-up or pull-down resistor, it will dissipate extra power when the input changes state. Additionally, the driver must deliver extra current which creates more dissipation in the driver.

Using conservative assumptions, you can calculate the following parameters from equation 2 for low voltage families when 2.7V V_{CC} 3.6V :

EQUATION 2

$$P_{BH} \quad f \pm T_T \pm \frac{I_{HOLD} \pm V_{CC}}{2}$$

where P_{BH} is the dissipation in the bus hold circuit itself
T_T is the average of the rise and fall times of the input signal
f is the frequency of the input signal

One important consequence of the above equation is that the dissipation of bus hold is dependent on the input rise and fall times which are primarily determined by the output drive capability of the driving component and the capacitive load.

The frequency, f in the equation is normally NOT equal to the clock frequency, it is an effective input frequency. For example, if the input is HIGH for a long time, the dissipation during that time is essentially zero. Therefore, you should estimate the number of transitions based on a practical occurrence of "0's" and "1's".

From equation 2, if IBHHO = 500μA and V_{CC} = 3.3V, the following worst case dissipation value in μW can be determined from equation 3 as follows:

EQUATION 3

$$P_{BH} \quad f \pm T_T$$

where f is in MHz and
T_T is in ns

Typically, the power dissipation is about half the value of P_{BH}.

Family Survey and Nomenclature

Philips Semiconductors has integrated bus hold circuits in some advanced BiCMOS and CMOS families which are identified by the letter "H" in its the part number (the exceptions are LVT and LVT16 families) as follows:

- A standard bus hold circuit with current path to V_{CC} is built in the following:
  - **LVCH** and **ALVCH**
- An enhanced bus hold circuit without current path to V_{CC} is built in the following:
  - **LVT**, **LVT16**, **ABTH**, and **ABTH16** using a Schottky diode arrangement
  - The 5 Volt tolerant **LVCXXXA** devices that use dynamic backgate switching.
- Families such as **LV**, **LVC**, **HLL**, **ABT**, **ABT16**, and all **5V CMOS** have no bus hold circuits.

Conclusion

This application note discusses the effects of bus hold circuits as applied by Philips Semiconductors in their advanced CMOS and BiCMOS logic families. Logic devices with bus hold circuits can have floating (open) inputs without any negative effects. They have a low power dissipation compared with using static pull-up or pull-down resistors and most importantly because they are integrated, they do not increase component count, keep costs low, and optimize the available space on the PCB.

Section 2
5V Devices
ABT, ABT16, MULTIBYTE™

BiCMOS Bus Interface Logic

CONTENTS

Section 2 – 5V Devices – ABT, ABT16, MULTIBYTE™(Continued)

ABT16, 16-Bit Devices

Section 2 – 5V Devices – ABT, ABT16, MULTIBYTE™ (Continued)

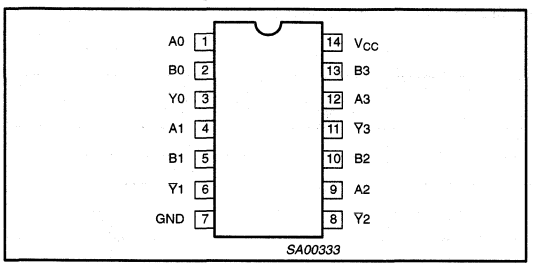
MULTIBYTE™ Devices

Quad 2-input NAND gate — 74ABT00

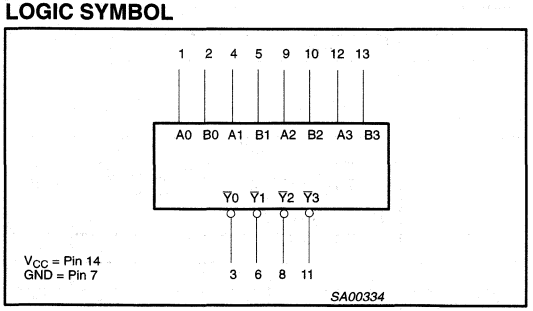
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 5V	2.5 2.0	ns
t_{OSLH} t_{OSHL}	Output to Output skew		0.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

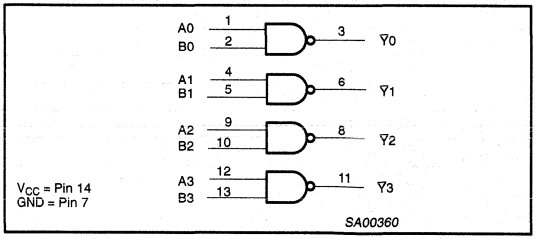
PIN CONFIGURATION



LOGIC SYMBOL



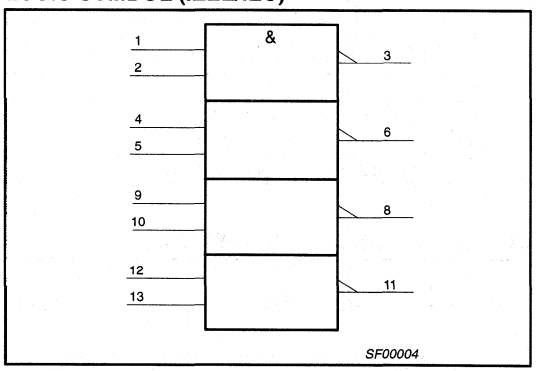
LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An-Bn	Data inputs
3, 6, 8, 11	$\overline{Y}n$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT00 N	74ABT00 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT00 D	74ABT00 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT00 DB	74ABT00 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT00 PW	74ABT00PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	40	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−75	−180	−50	−180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

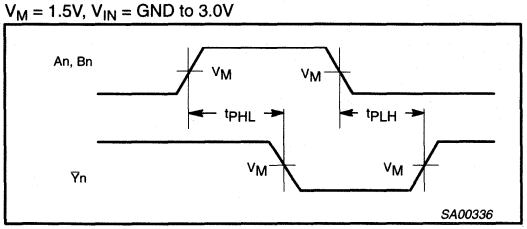
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}$n	1	1.0 1.0	2.5 2.0	3.6 2.8	1.0 1.0	4.1 3.4	ns
t_{OSHL} t_{OSLH}[1]	Output to Output skew An or Bn to $\overline{Y}$n	2		0.4 0.4	0.5 0.5		0.5 0.5	ns

NOTE:

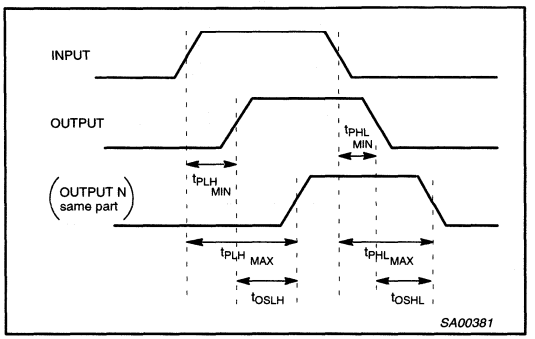
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

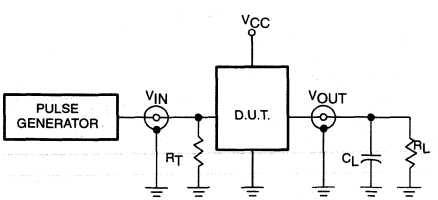


Waveform 1. Propagation delay for inverting outputs

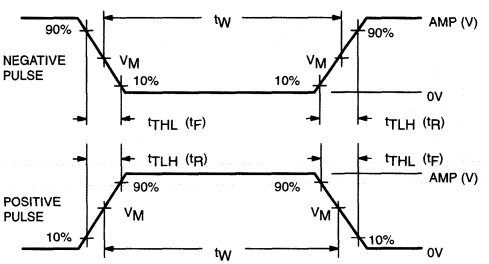


Waveform 2. Common edge skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

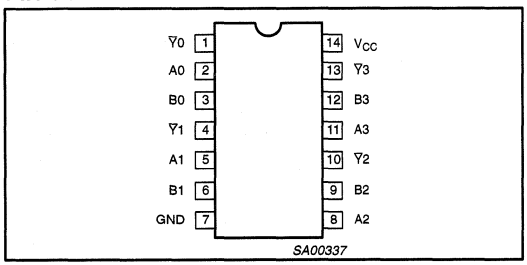
SH00067

Quad 2-input NOR gate | 74ABT02

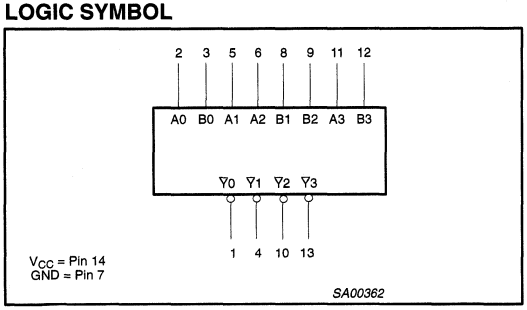
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 5V	2.4 1.8	ns
t_{OSLH} t_{OSHL}	Output to Output skew		0.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	μA

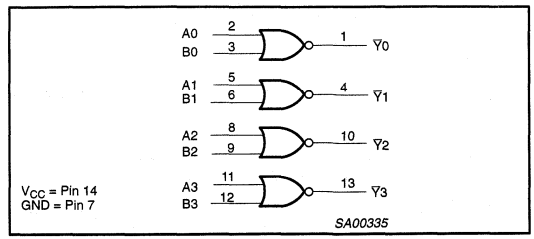
PIN CONFIGURATION



LOGIC SYMBOL



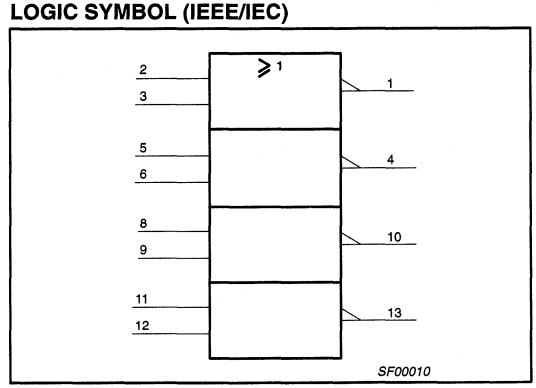
LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 5, 6, 8, 9, 11, 12	An-Bn	Data inputs
1, 4, 10, 13	$\overline{Y}n$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
An	Bn	$\overline{Y}n$
L	L	H
L	H	L
H	L	L
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT02 N	74ABT02 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT02 D	74ABT02 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT02 DB	74ABT02 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT02 PW	74ABT02PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	40	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–75	–180	–50	–180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

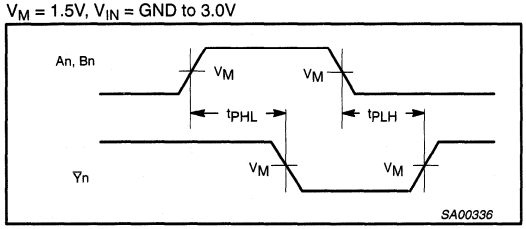
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}$n	1	1.0 1.0	2.4 1.8	3.7 2.8	1.0 1.0	4.4 3.4	ns
t_{OSHL} t_{OSLH}[1]	Output to Output skew An or Bn to $\overline{Y}$n	2		0.4 0.4	0.5 0.5		0.5 0.5	ns

NOTE:

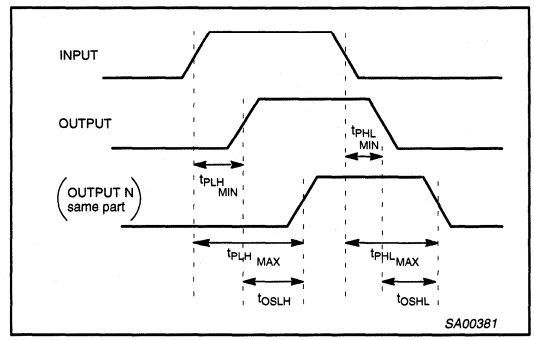
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

AC WAVEFORMS

$V_M = 1.5V$, V_{IN} = GND to 3.0V

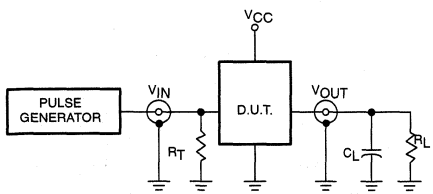


Waveform 1. Propagation delay for inverting outputs

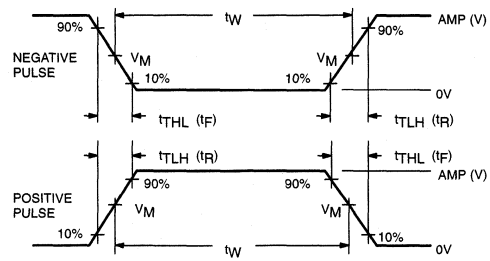


Waveform 2. Common edge skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

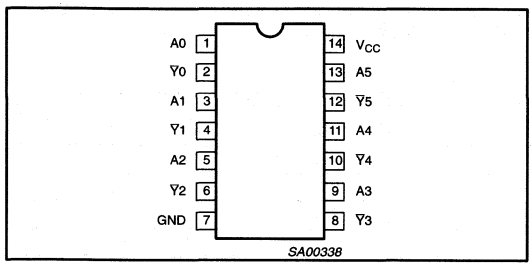
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00067

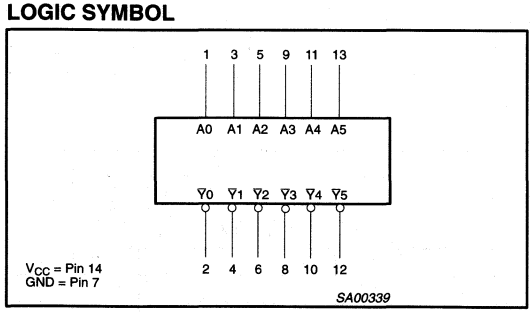
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}n$	C_L = 50pF; V_{CC} = 5V	2.2 1.6	ns
t_{OSLH} t_{OSHL}	Output to Output skew		0.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

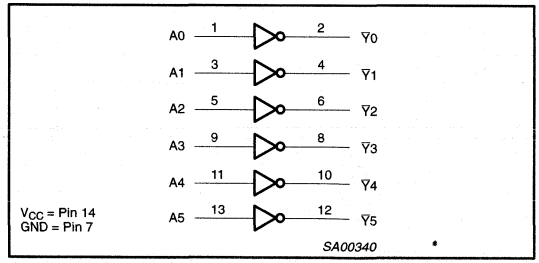
PIN CONFIGURATION



LOGIC SYMBOL



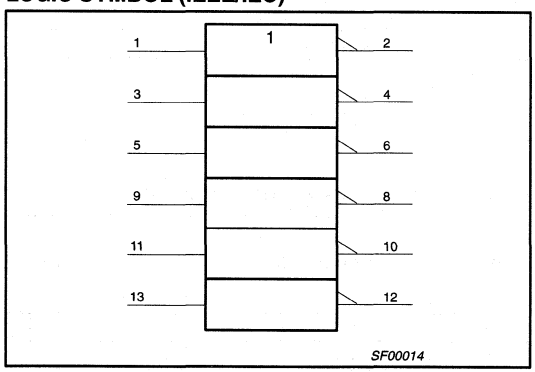
LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	An	Data inputs
2, 4, 6, 8, 10, 12	$\overline{Y}$n	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS	OUTPUT
An	$\overline{Y}$n
L	H
H	L

NOTES:
H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT04 N	74ABT04 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT04 D	74ABT04 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT04 DB	74ABT04 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT04 PW	74ABT04PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	40	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–75	–180	–50	–180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

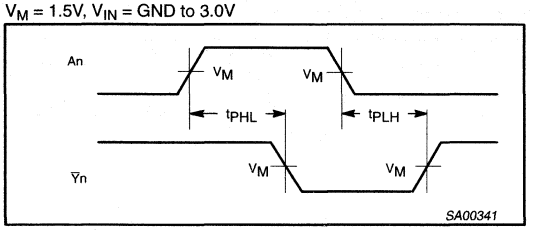
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	1	1.0 1.0	2.2 1.6	3.4 2.5	1.0 1.0	4.1 3.0	ns
t_{OSHL} t_{OSLH}[1]	Output to Output skew An or Bn to $\overline{Y}$n	2		0.4	0.5		0.5	ns

NOTE:

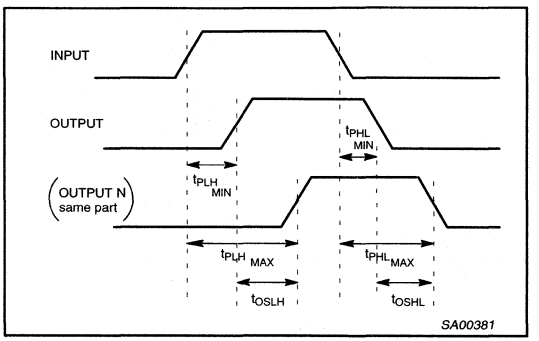
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

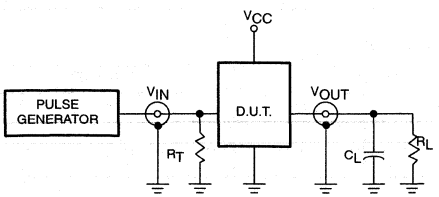


Waveform 1. Propagation delay for inverting outputs

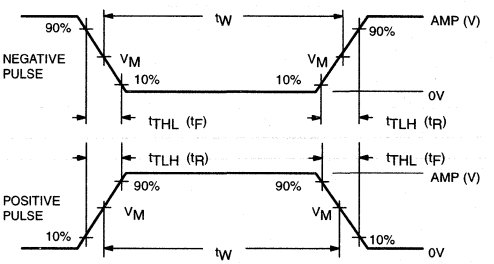


Waveform 2. Common edge skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

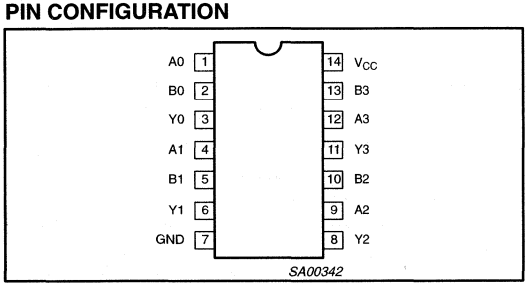
SH00067

Quad 2-input AND gate — 74ABT08

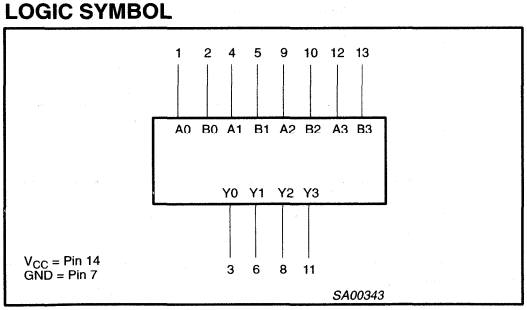
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An or Bn to Yn	C_L = 50pF; V_{CC} = 5V	2.4 1.9	ns
t_{OSLH} t_{OSHL}	Output to Output skew		0.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

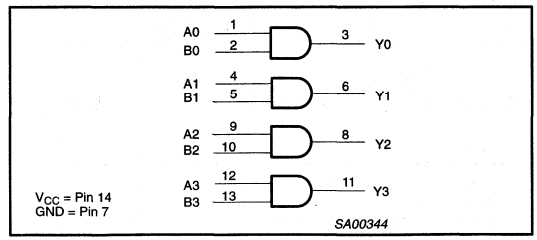
PIN CONFIGURATION



LOGIC SYMBOL



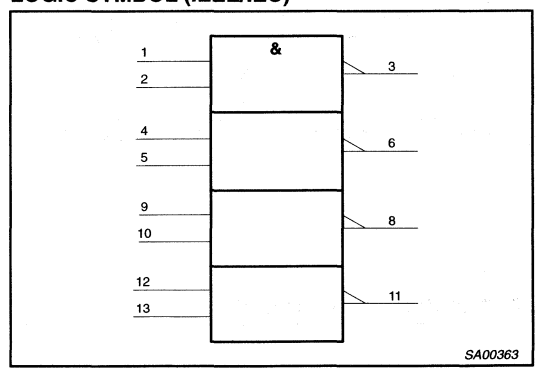
LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An-Bn	Data inputs
3, 6, 8, 11	Yn	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
An	Bn	Yn
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:
H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT08 N	74ABT08 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT08 D	74ABT08 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT08 DB	74ABT08 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT08 PW	74ABT08PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	40	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–75	–180	–50	–180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

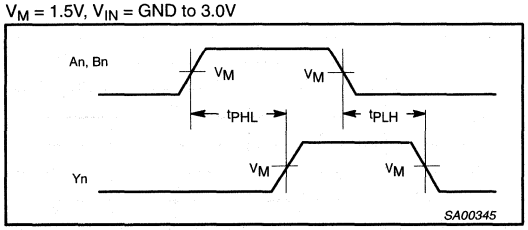
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An or Bn to Yn	1	1.0 1.0	2.4 1.9	3.4 2.8	1.0 1.0	4.0 3.0	ns
t_{OSHL} t_{OSLH}[1]	Output to Output skew An or Bn to $\overline{Y}$n	2		0.4 0.4	0.5 0.5		0.5 0.5	ns

NOTE:

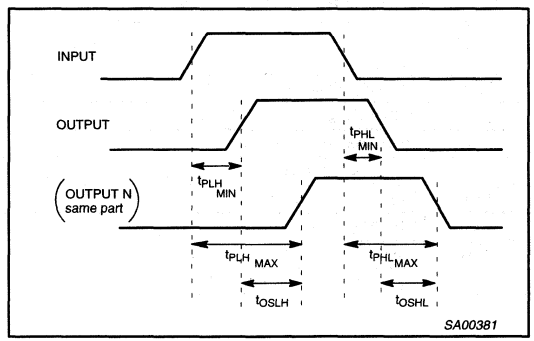
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

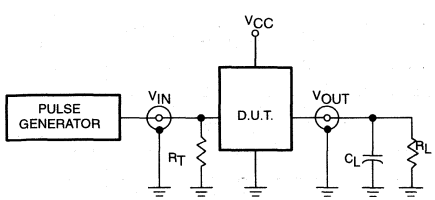


Waveform 1. Propagation Delay for Non-Inverting Outputs

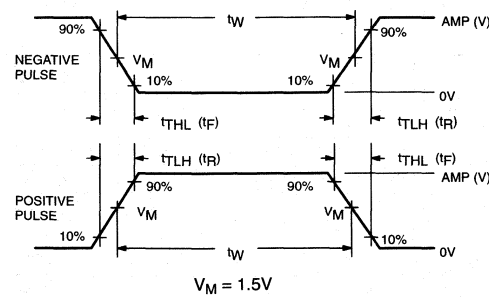


Waveform 2. Common edge skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

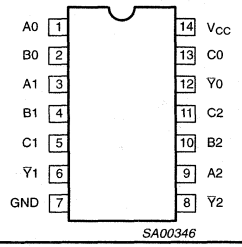
SH00067

Triple 3-input NAND gate | 74ABT10

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 5V	3.3 2.2	ns
t_{OSLH} t_{OSHL}	Output to Output skew		0.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

PIN CONFIGURATION

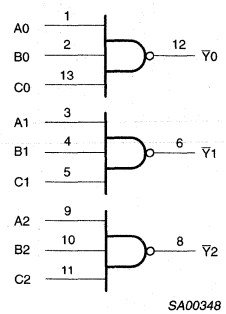


SA00346

PIN DESCRIPTION

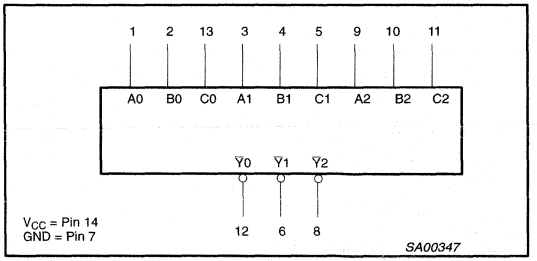
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 9, 10, 11, 13	An, Bn, Cn	Data inputs
6, 8, 12	$\overline{Y}n$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



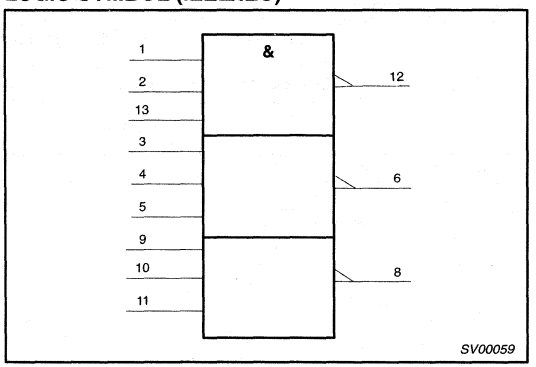
SA00348

LOGIC SYMBOL



SA00347

LOGIC SYMBOL (IEEE/IEC)



SV00059

FUNCTION TABLE

INPUTS			OUTPUTS
An	Bn	Cn	$\overline{Y}n$
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT10 N	74ABT10 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT10 D	74ABT10 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT10 DB	74ABT10 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT10 PW	74ABT10PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	40	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–75	–180	–50	–180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flop or latch after applying the power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

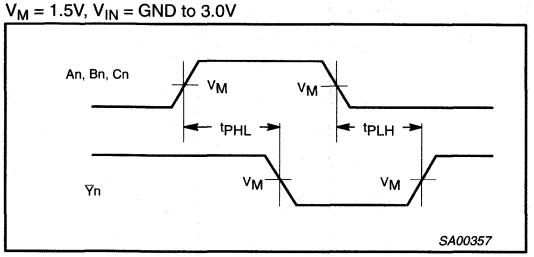
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn to $\overline{Y}n$	1	1.0 1.0	3.3 2.2	4.7 3.3	1.0 1.0	5.3 3.7	ns
t_{OSHL} t_{OSLH}[1]	Output to Output skew An or Bn to $\overline{Y}n$	2		0.4	0.5		0.5	ns

NOTE:

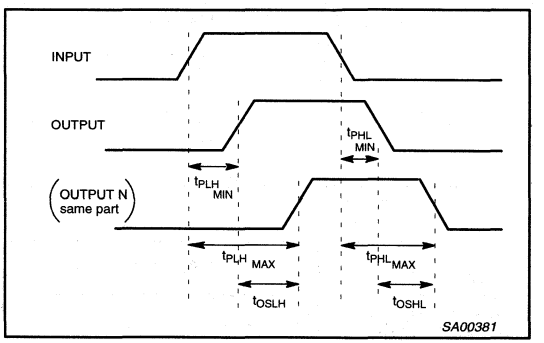
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH–to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

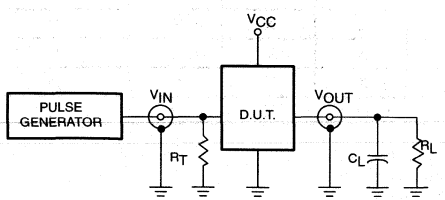


Waveform 1. Propagation Delay for Inverting Outputs

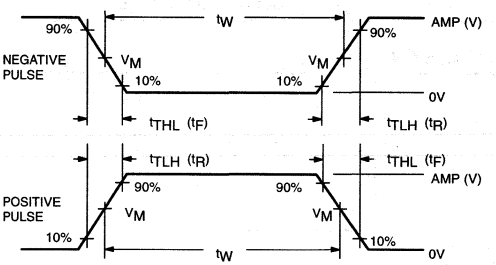


Waveform 2. Common edge skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

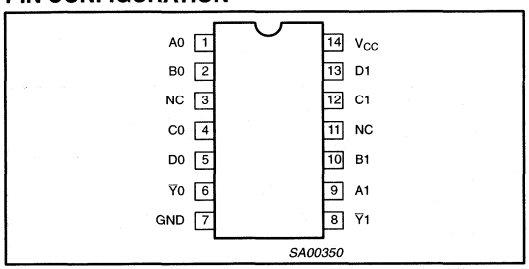
SH00067

Dual 4-input NAND gate — 74ABT20

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn, Dn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 5V	2.7 2.2	ns
t_{OSLH} t_{OSHL}	Output to Output skew		0.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

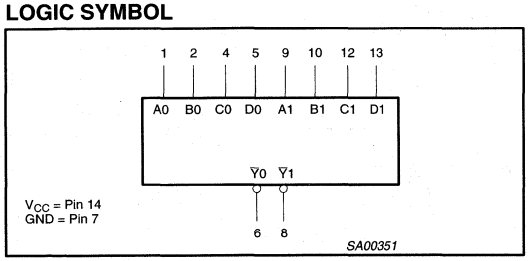
PIN CONFIGURATION



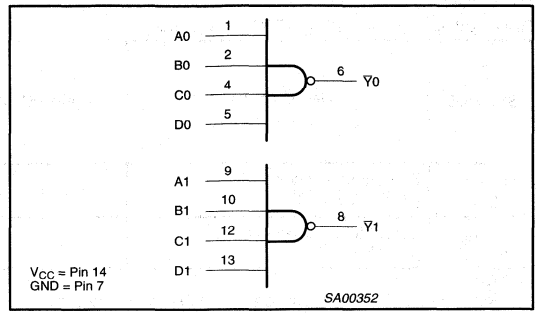
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An, Bn, Cn, Dn	Data inputs
6, 8	$\overline{Y}$n	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

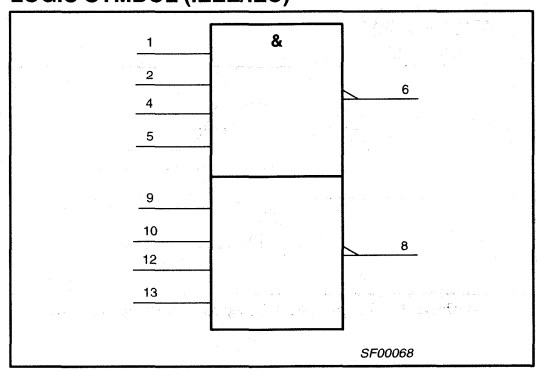
LOGIC SYMBOL



LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUT
An	Bn	Cn	Dn	$\overline{Y}$n
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT20 N	74ABT20 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT20 D	74ABT20 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT20 DB	74ABT20 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT20 PW	74ABT20PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	40	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−75	−180	−50	−180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flop or latch after applying the power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

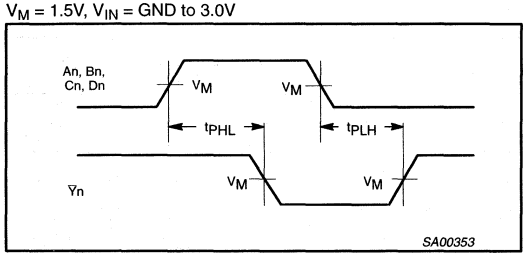
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn, Dn to $\overline{Y}$n	1	1.0 1.0	2.7 2.2	3.9 3.4	1.0 1.0	4.6 3.8	ns
t_{OSHL} t_{OSLH}[1]	Output to Output skew An or Bn to $\overline{Y}$n	2		0.3	0.5		0.5	ns

NOTE:

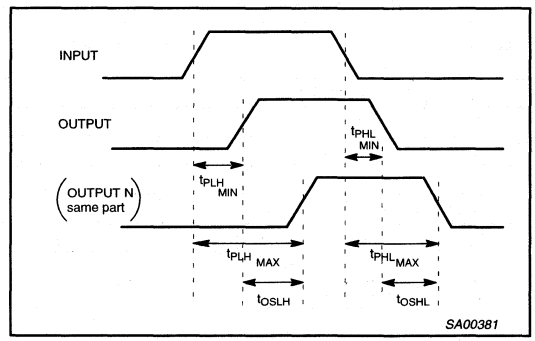
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH–to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

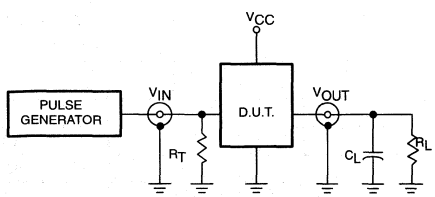


Waveform 1. Propagation Delay for Inverting Outputs

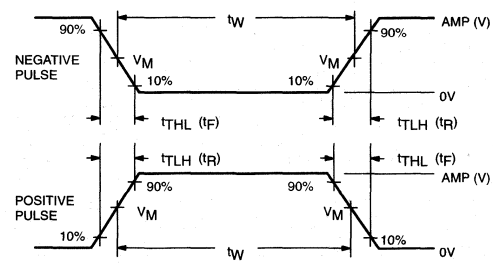


Waveform 2. Common edge skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

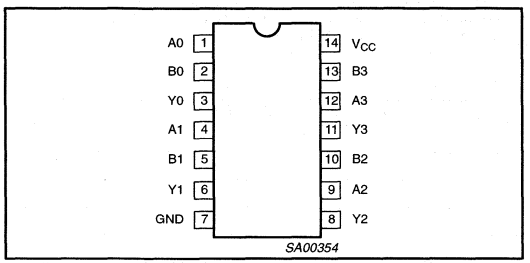
SH00067

Quad 2-input OR gate — 74ABT32

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An, Bn to Yn	C_L = 50pF; V_{CC} = 5V	2.3 1.9	ns
t_{OSLH} t_{OSHL}	Output to Output skew		0.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	μA

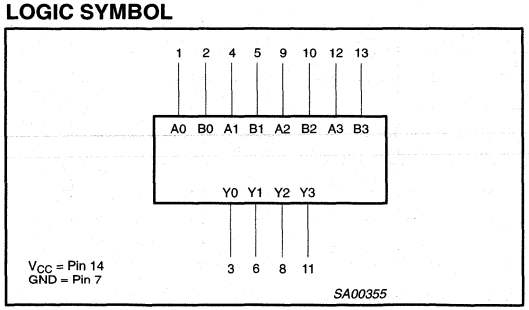
PIN CONFIGURATION



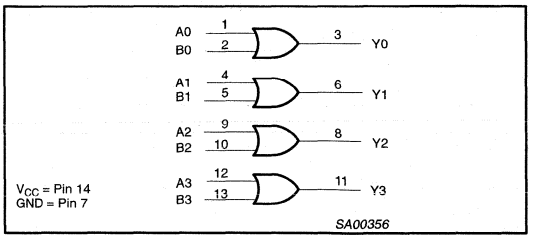
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An, Bn	Data inputs
3, 6, 8, 11	Yn	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

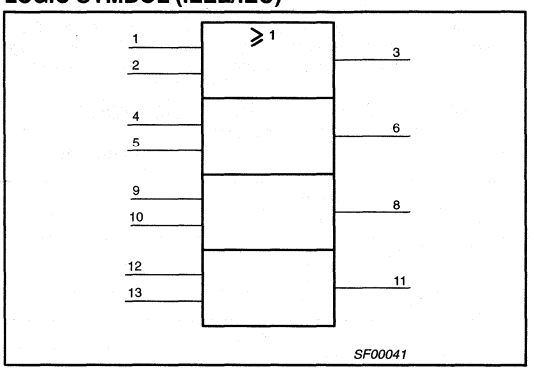
LOGIC SYMBOL



LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
An	Bn	Yn
L	L	L
L	H	H
H	L	H
H	H	H

NOTES:
H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT32 N	74ABT32 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT32 D	74ABT32 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT32 DB	74ABT32 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT32 PW	74ABT32PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	40	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–75	–180	–50	–180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flop or latch after applying the power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

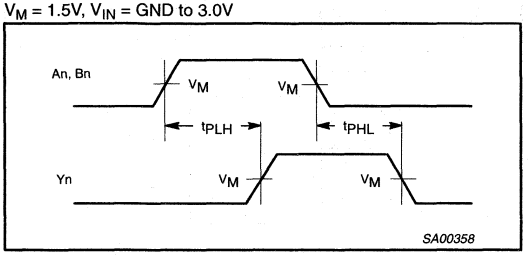
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An, Bn to Yn	1	1.0 1.0	2.3 1.9	3.4 2.9	1.0 1.0	3.8 3.2	ns
t_{OSHL} t_{OSLH}[1]	Output to Output skew An or Bn to $\overline{Y}$n			0.4	0.5		0.5	ns

NOTE:

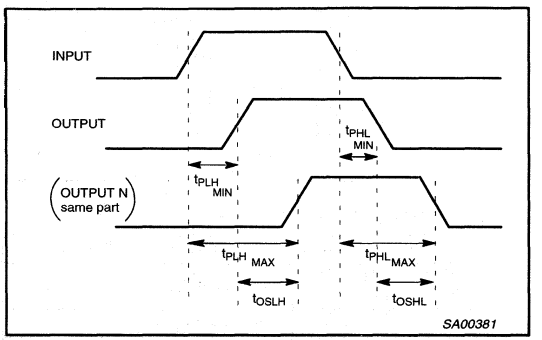
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH–to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

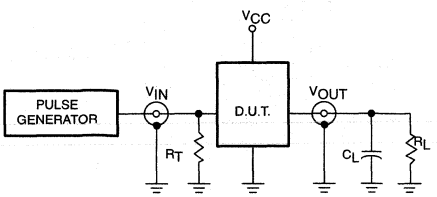


Waveform 1. Propagation delay for inverting outputs

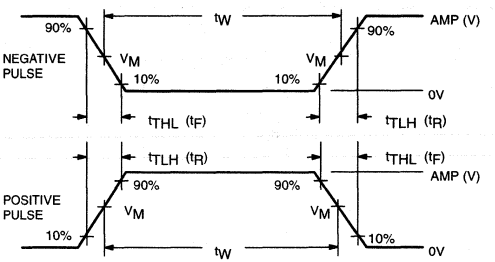


Waveform 2. Common edge skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

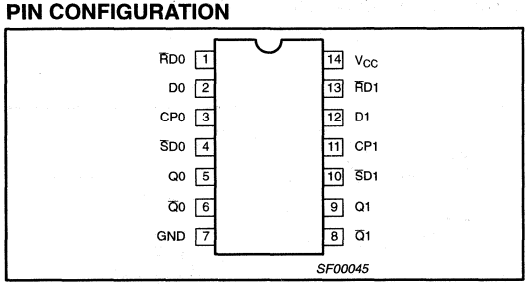
SH00067

Dual D-type flip-flop | 74ABT74

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPn to Qn, $\overline{Q}$n	C_L = 50pF; V_{CC} = 5V	3.0 2.5	ns
t_{OSLH} t_{OSHL}	Output to Output skew		0.5	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	μA

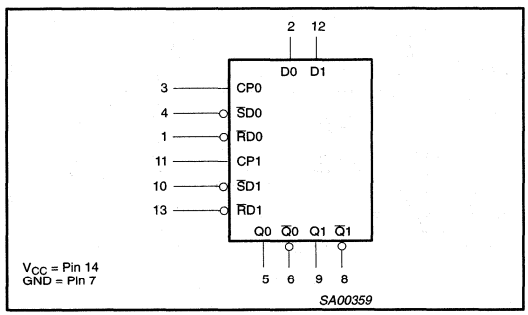
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 10, 11, 12, 13	$\overline{R}$Dn, Dn, CPn, $\overline{S}$Dn	Data inputs
5, 6, 8, 9	Qn, $\overline{Q}$n	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

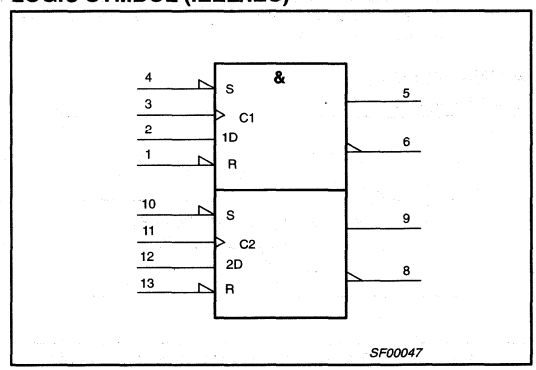
LOGIC SYMBOL



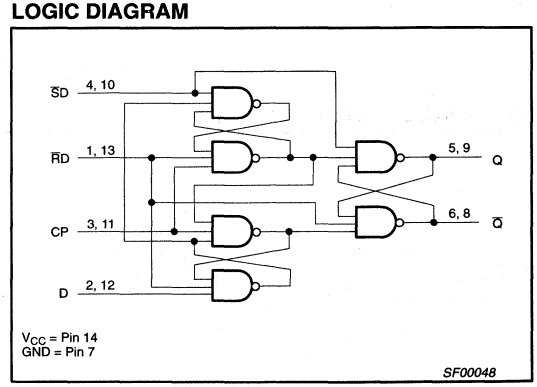
DESCRIPTION

The 74ABT74 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{S}$D) and reset ($\overline{R}$D) are asynchronous active low inputs and operate independently of the clock input. When set and reset are inactive (high), data at the D input is transferred to the Q and $\overline{Q}$ outputs on the low-to-high transition of the clock. Data must be stable just one setup time prior to the low-to-high transition of the clock for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT74 N	74ABT74 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT74 D	74ABT74 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT74 DB	74ABT74 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT74 PW	74ABT74PW DH	SOT402-1

FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↥	X	NC	NC	Hold

NOTES:
H = High voltage level
h = High voltage level one setup time prior to low-to-high clock transition
L = Low voltage level
l = Low voltage level one setup time prior to low-to-high clock transition
NC = No change from the previous setup
X = Don't care
↑ = Low-to-high clock transition
↥ = Not low-to-high clock transition
* = This setup is unstable and will change when either set or reset return to the high level.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	40	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−75	−180	−50	−180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flop or latch after applying the power.

AC ELECTRICAL CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	180	250		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPn to Qn, $\overline{Q}$n	1	1.0 1.0	3.0 2.5	4.2 3.5	1.0 1.0	4.7 4.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$n, $\overline{R}$n to Qn, $\overline{Q}$n	3	1.0 1.0	3.4 2.9	4.9 4.5	1.0 1.0	6.2 5.2	ns
t_{OSHL} t_{OSLH}[1]	Output to Output skew An or Bn to Yn	4		0.5	0.6		0.6	ns

NOTE:
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH–to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

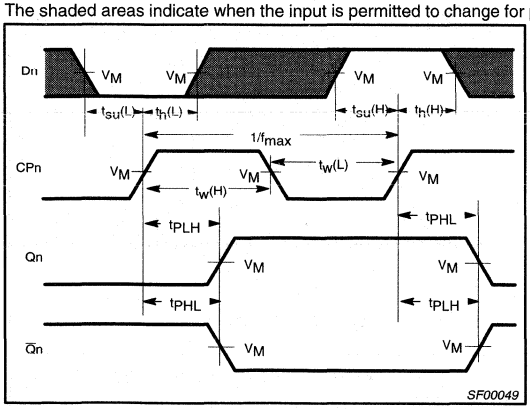
AC SETUP REQUIREMENTS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

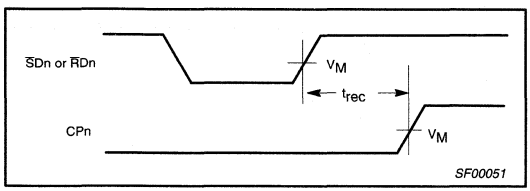
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C V_{CC} = +5.0V		T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CPn	1	2.6 2.4	1.4 1.4	2.6 2.4	ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	1	0 0	−1.4 −1.4	0 0	ns
t_w (H) t_w (L)	CPn pulse width, high or low	1	1.7 1.7	1.0 1.0	2.1 2.1	ns
t_w (L)	$\overline{S}$Dn, $\overline{R}$Dn pulse width, low	3	2.0	1.3	2.2	ns
t_{rec}	Recovery time $\overline{S}$Dn, $\overline{R}$Dn to CPn	2	2.1	1.4	2.4	ns

AC WAVEFORMS

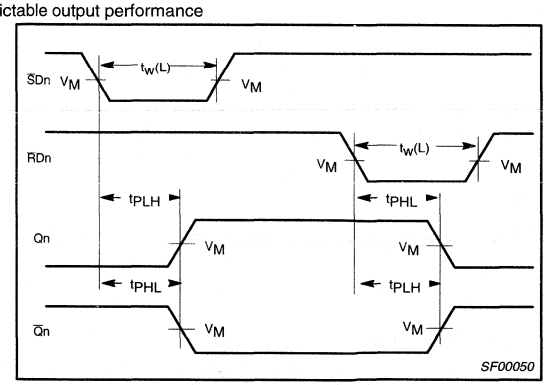
V_M = 1.5V, V_{IN} = GND to 3.0V
The shaded areas indicate when the input is permitted to change for predictable output performance



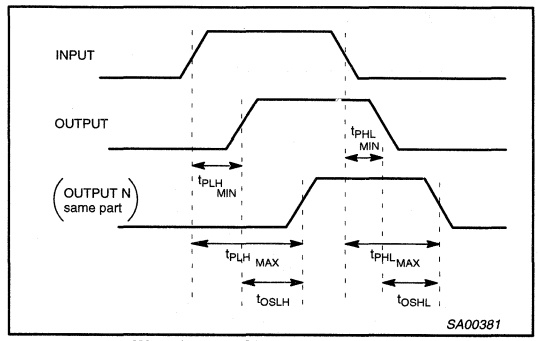
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Recovery time for set or reset to clock

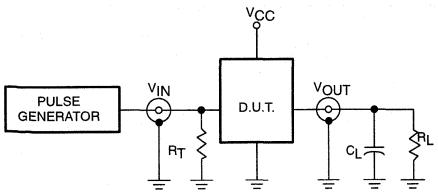


Waveform 3. Propagation delay for set and reset to output, set and reset pulse width

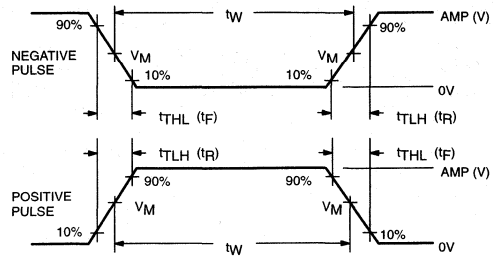


Waveform 4. Common edge skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00067

Quad buffer (3-State) 74ABT125

FEATURES

- Quad bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT125 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT125 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$, $\overline{OE}3$), each controlling one of the 3-State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	65	µA

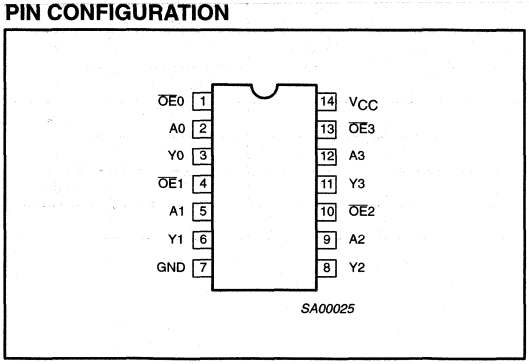
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT125 N	74ABT125 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT125 D	74ABT125 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT125 DB	74ABT125 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT125 PW	74ABT125PW DH	SOT402-1

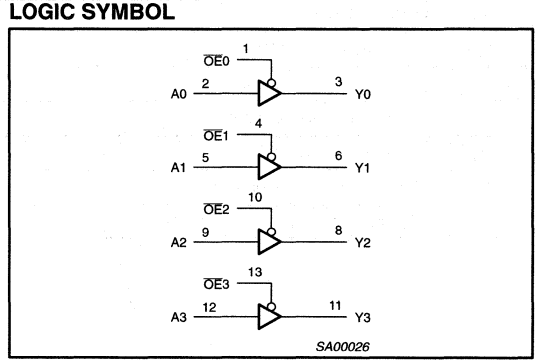
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 9, 12	A0 – A3	Data inputs
3, 6, 8, 11	Y0 – Y3	Data outputs
1, 4, 10, 13	$\overline{OE}0$ – $\overline{OE}3$	Output enable inputs (active-Low)
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

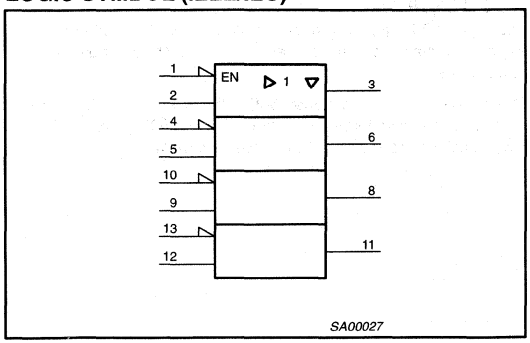
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}n$	An	Yn
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.35	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		1.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–1.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		65	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		12	15		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		65	250		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

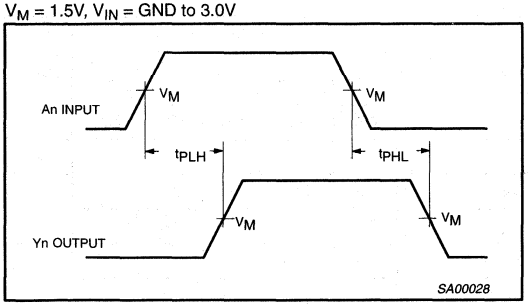
AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

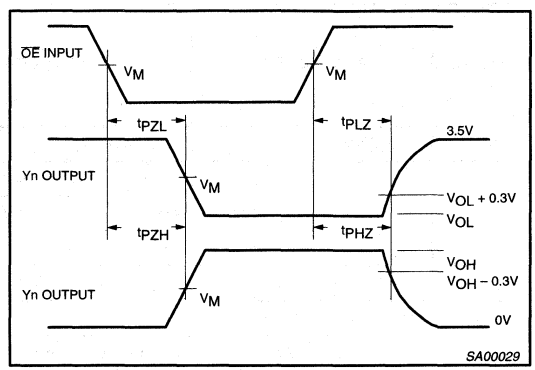
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.8 3.1	4.1 4.6	1.0 1.0	4.6 4.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.2 4.2	5.0 6.2	1.0 1.0	5.9 6.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.0 1.5	4.1 2.8	5.4 5.0	1.0 1.5	6.2 5.5	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

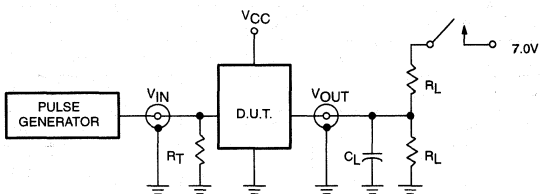


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

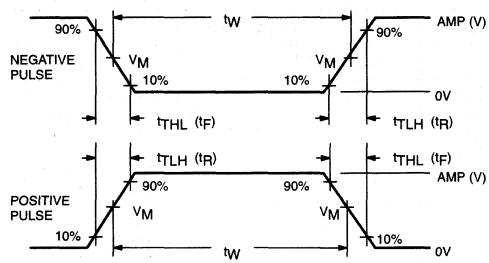


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Quad buffer (3-State) 74ABT126

FEATURES

- Quad bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT126 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT126 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables (OE0, OE1, OE2, OE3), each controlling one of the 3-State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	65	μA

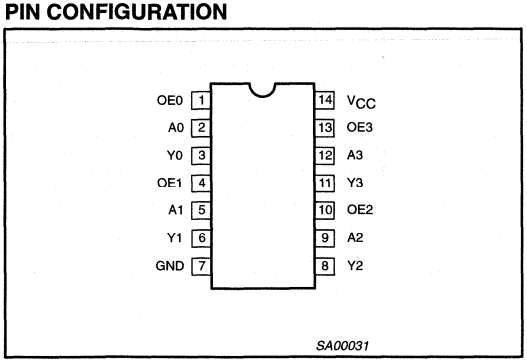
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT126 N	74ABT126 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT126 D	74ABT126 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT126 DB	74ABT126 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT126 PW	74ABT126PW DH	SOT402-1

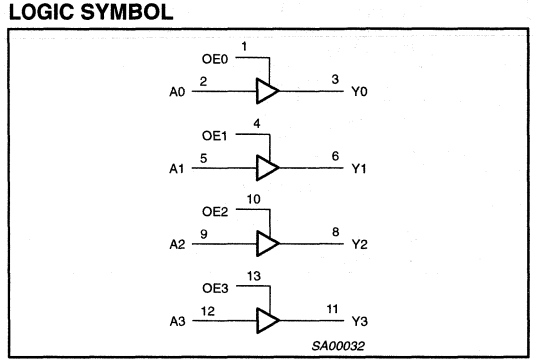
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 9, 12	A0 – A3	Data inputs
3, 6, 8, 11	Y0 – Y3	Data outputs
1, 4, 10, 13	OE0 – OE3	Output enable inputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

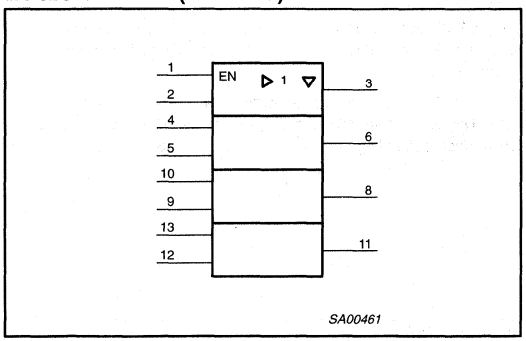
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS
OEn	An	Yn
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.35	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I GND or V_{CC}; $V_{\overline{OE}}$ = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		1.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–1.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		65	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		12	15		15	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		65	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

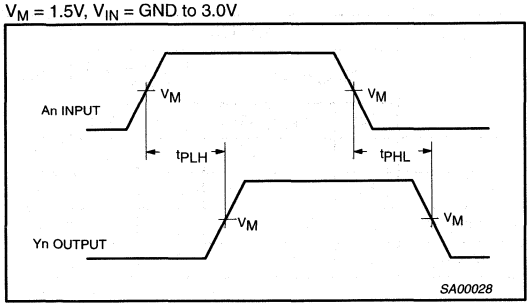
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

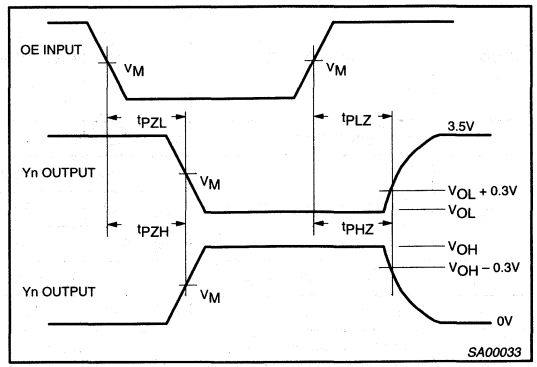
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.9 3.0	4.2 4.3	1.0 1.0	4.4 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.9 1.9	3.2 4.4	5.8 5.9	1.9 1.9	6.5 6.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.0 1.0	4.2 2.9	5.2 4.9	1.0 1.0	5.8 5.5	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

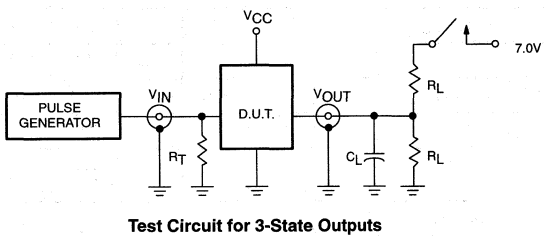


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

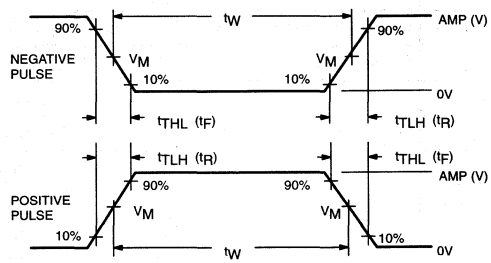


Waveform 2. Waveforms Showing the 3–State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal inverting buffer (3-State) 74ABT240

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT240 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT240 device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	μA

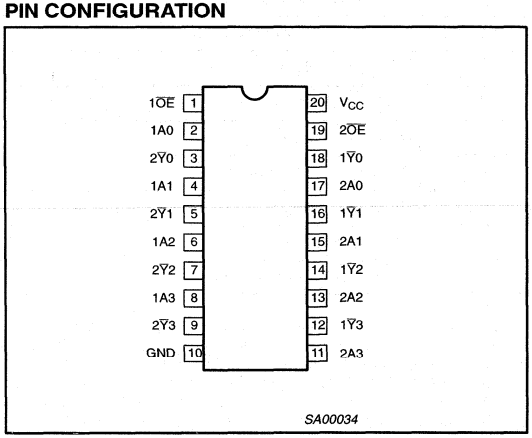
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT240 N	74ABT240 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT240 D	74ABT240 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT240 DB	74ABT240 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT240 PW	74ABT240PW DH	SOT360-1

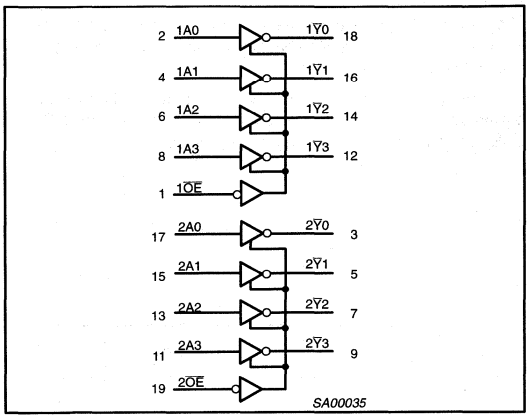
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1$\overline{Y}$0 – 1$\overline{Y}$3	Data outputs
9, 7, 5, 3	2$\overline{Y}$0 – 2$\overline{Y}$3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

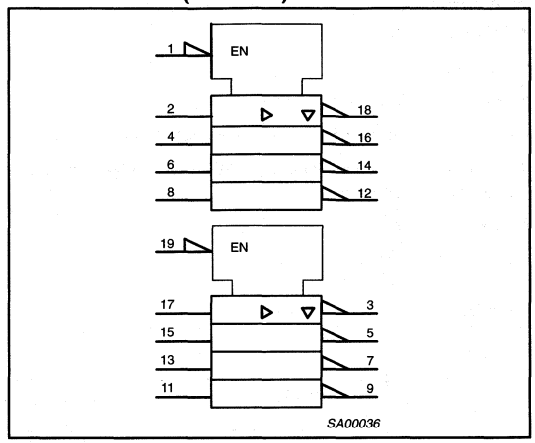
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	$1\overline{Y}n$	$2\overline{Y}n$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V;		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-state output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs 3-State, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} 5V ± 10% a transition time of up to 100µsec is permitted.

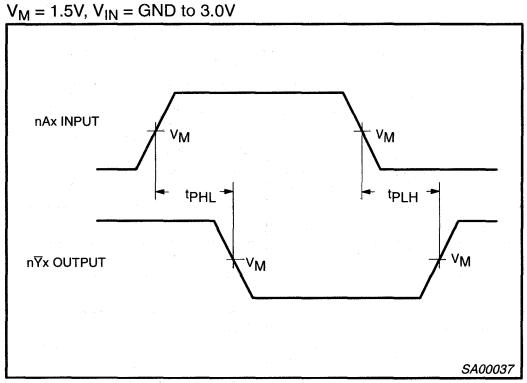
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

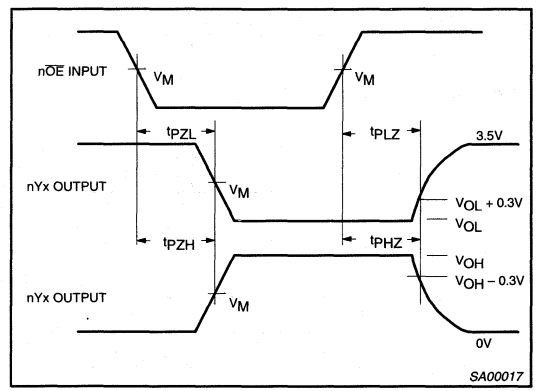
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1.0 1.6	2.7 3.5	4.1 4.3	1.0 1.6	4.8 4.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.1	3.1 4.2	4.7 5.8	1.1 1.1	5.2 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.8 1.6	3.7 3.0	5.7 5.4	1.8 1.6	6.4 5.8	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

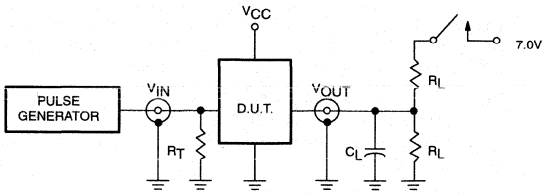


Waveform 1. Waveforms Showing the Input (nAx) to Output (n$\overline{Y}$x) Propagation Delays

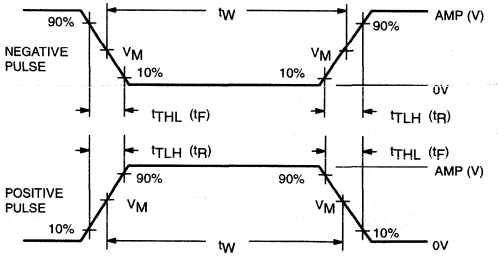


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal inverting buffer with 30Ω series termination resistors (3-State)

74ABT2240

FEATURES

- Octal bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω, making external termination resistors unnecessary
- Output capability: +12mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Same part as 74ABT240-1

DESCRIPTION

The 74ABT2240 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT2240 device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

The 74ABT2240 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

The 74ABT2240 is the same as the 74ABT240-1. The part number has been changed to reflect industry standards.

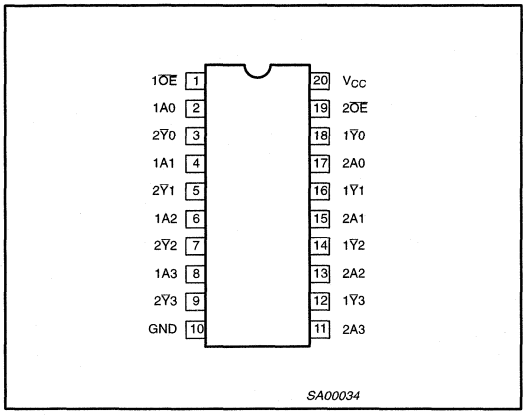
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}n$	C_L = 50pF; V_{CC} = 5V	2.8 4.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT2240 N	74ABT2240 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT2240 D	74ABT2240 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT2240 DB	74ABT2240 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT2240 PW	7ABT2240PW DH	SOT360-1

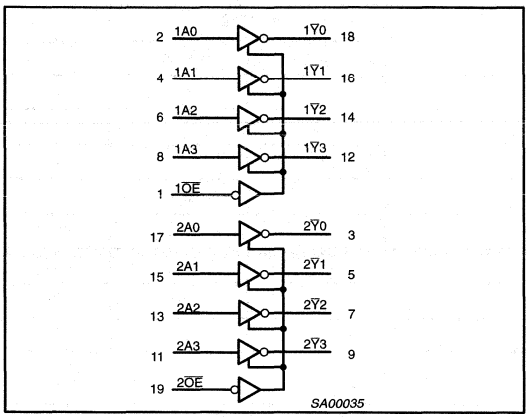
PIN CONFIGURATION



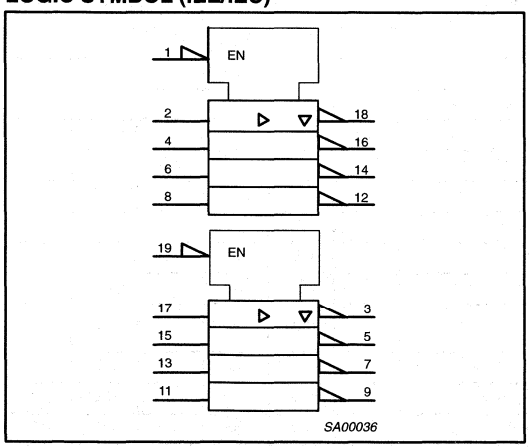
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	$1\overline{Y}0$ – $1\overline{Y}3$	Data outputs
9, 7, 5, 3	$2\overline{Y}0$ – $2\overline{Y}3$	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEE/IEC)

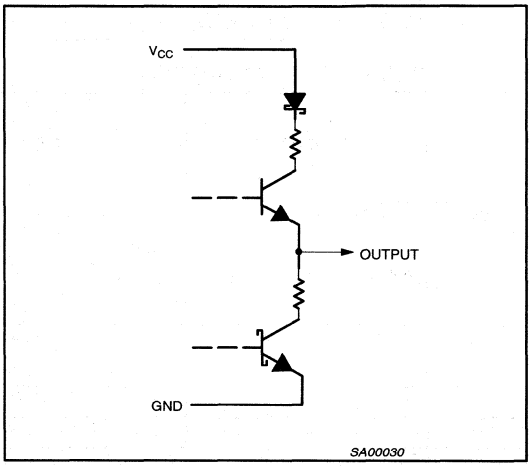


FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	$1\overline{Y}n$	$2\overline{Y}n$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

SCHEMATIC OF EACH OUTPUT



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 5mA; V_I = V_{IL} or V_{IH};		0.32	0.55		0.55	V
		V_{CC} = 4.5V; I_{OL} = 12mA; V_I = V_{IL} or V_{IH}			0.8		0.8	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power–up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		0.01	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–0.01	–50		–50	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

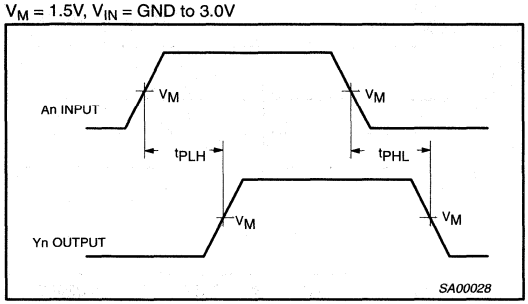
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

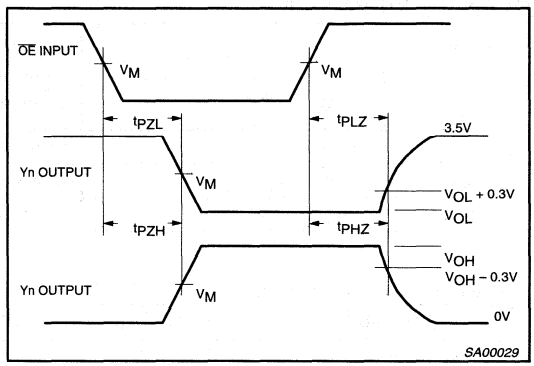
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	1	1.0 3.0	2.8 4.3	4.0 5.8	1.0 3.0	4.9 6.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 4.2	3.4 5.5	4.7 7.6	1.5 4.2	5.8 8.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.9 2.5	4.1 3.4	5.0 5.8	1.9 2.5	5.6 6.4	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

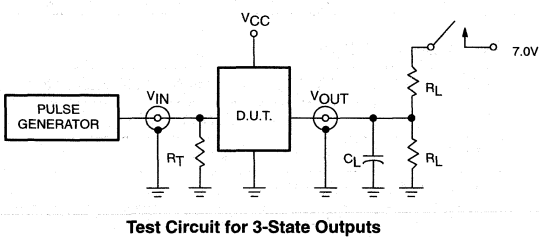


Waveform 1. Waveforms Showing the Input (An) to Output ($\overline{Y}$n) Propagation Delays

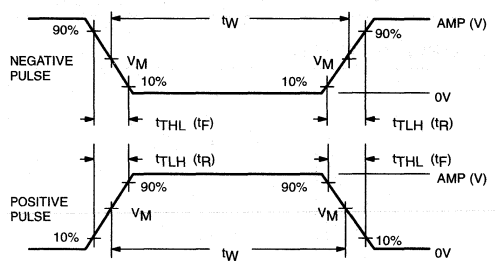


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal buffer/line driver (3-State) 74ABT241

FEATURES

- Octal bus interface
- 3-State buffers
- Power-up 3-State
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT241 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, 2OE), each controlling four of the 3-State outputs.

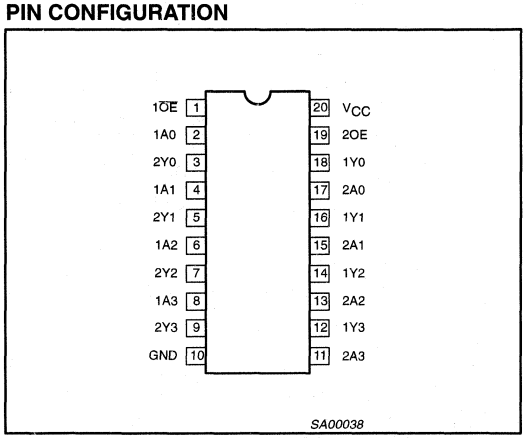
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.6 2.7	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT241 N	74ABT241 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT241 D	74ABT241 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT241 DB	74ABT241 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT241 PW	74ABT241PW DH	SOT360-1

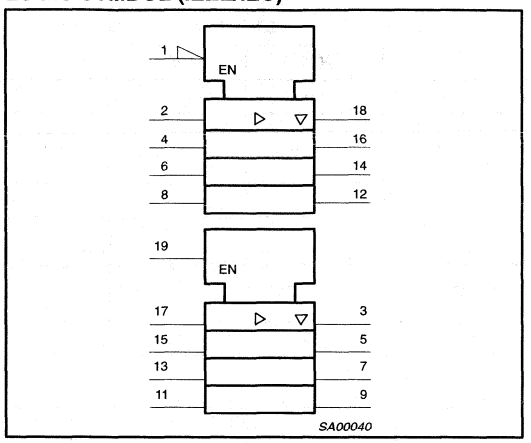
PIN CONFIGURATION



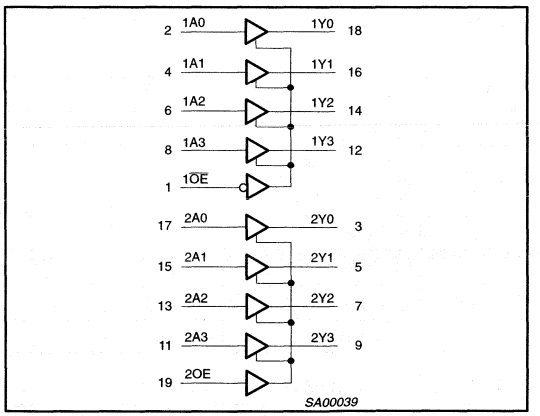
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
17, 15, 13, 11	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
3, 5, 7, 9	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, 2OE	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	2OE	2An	1Yn	2Yn
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = V_{CC}; V_{OE} = GND		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100 µsec is permitted.

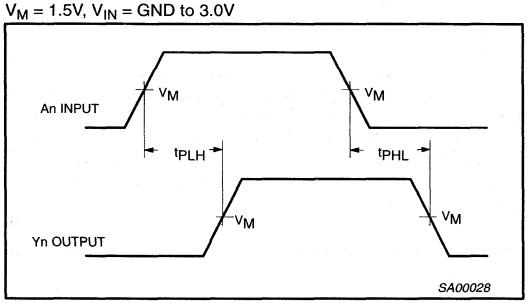
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

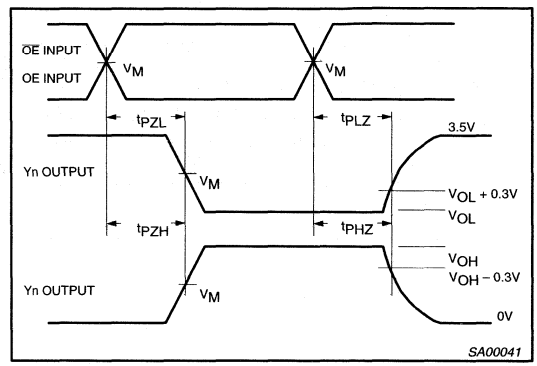
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.6 2.7	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.3	3.2 4.3	6.3 5.8	1.1 1.3	6.8 6.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.6 1.0	3.6 2.6	6.1 5.4	1.6 1.0	7.1 5.9	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

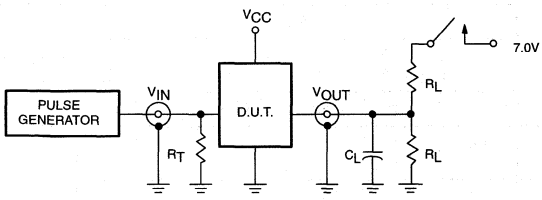


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

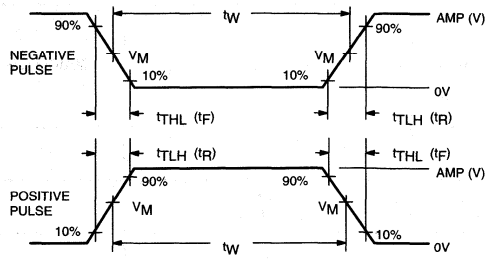


Waveform 2. Waveforms Showing the 3–State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal buffer with 30Ω series termination resistors (3-State)

74ABT2241

FEATURES

- Octal bus interface
- 3-State buffers
- Power-up 3-State
- Output capability: +12mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT2241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT2241 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, 2OE), each controlling four of the 3-State outputs.

The 74ABT2241 is designed with 30Ω series resistance in both the High and Low states of the output. The design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transceivers.

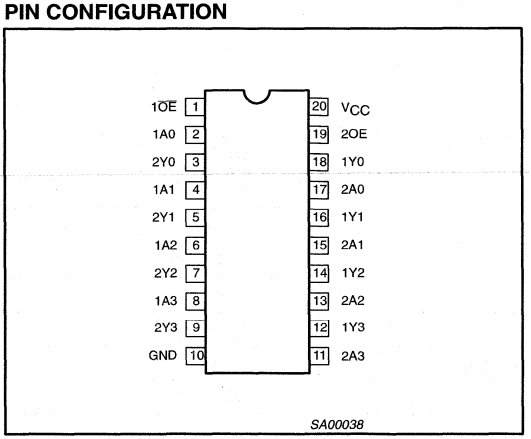
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT2241 N	74ABT2241 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT2241 D	74ABT2241 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT2241 DB	74ABT2241 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT2241 PW	7ABT2241PW DH	SOT360-1

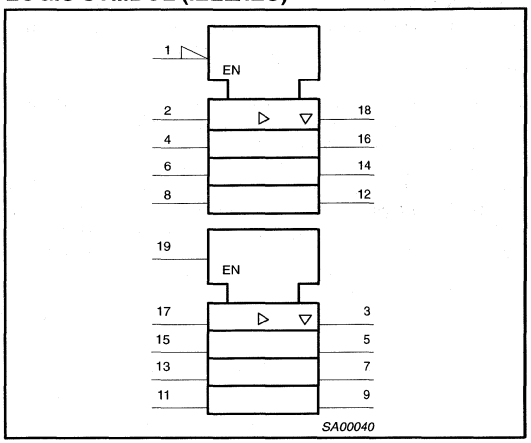
PIN CONFIGURATION



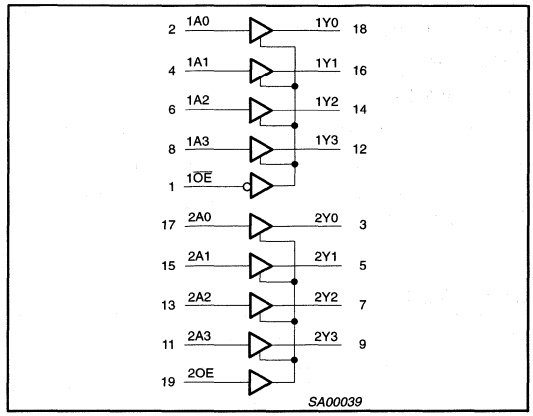
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
17, 15, 13, 11	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
3, 5, 7, 9	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, 2OE	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

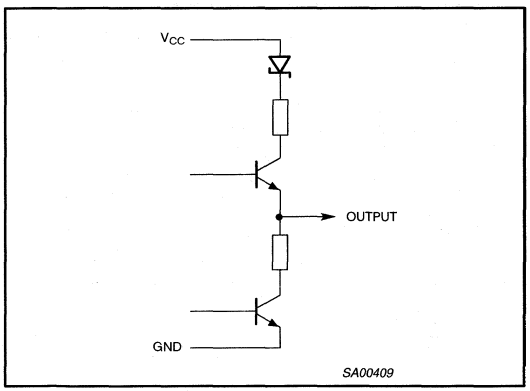
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



SCHEMATIC OF EACH OUTPUT



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	2OE	2An	1Yn	2Yn
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 5mA; V_I = V_{IL} or V_{IH}		0.32	0.55		0.55	V
		V_{CC} = 4.5V; I_{OL} = 12mA; V_I = V_{IL} or V_{IH}			0.8		0.8	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}; V_{OE} = GND		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100 µsec is permitted.

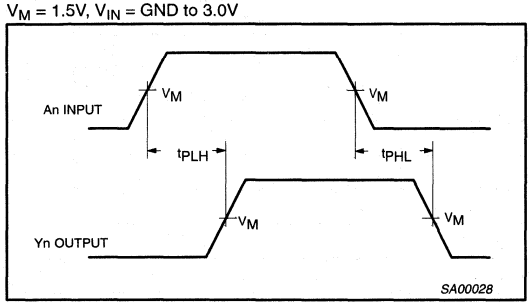
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

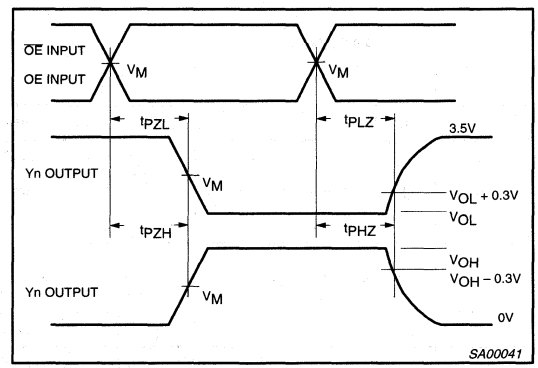
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.7 3.9	4.3 5.3	1.0 1.0	4.7 5.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 2.1	3.3 5.4	4.8 7.6	1.1 2.1	5.8 8.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.7 1.7	3.8 3.4	5.6 5.8	1.7 1.7	6.6 6.4	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

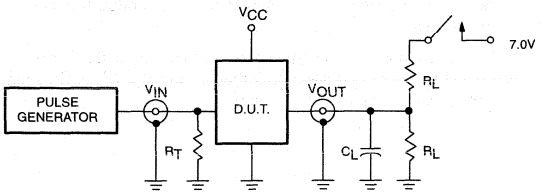


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

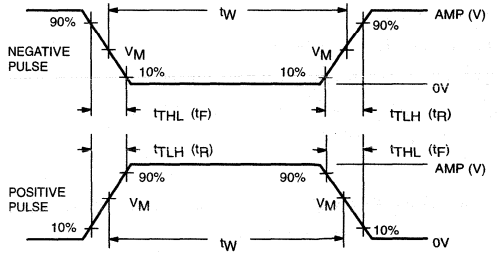


Waveform 2. Waveforms Showing the 3–State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal buffer/line driver (3-State) 74ABT244

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion capacity
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT244 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT244 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

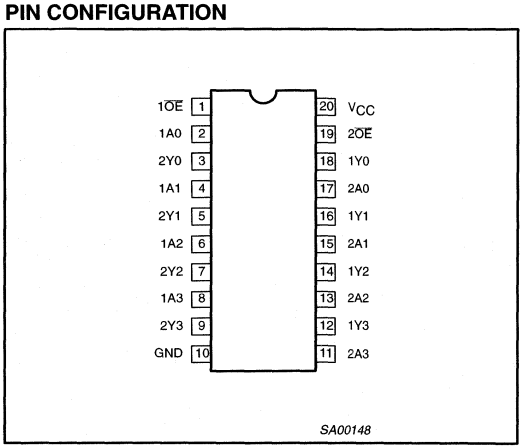
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT244 N	74ABT244 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT244 D	74ABT244 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT244 DB	74ABT244 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT244 PW	74ABT244PW DH	SOT360-1

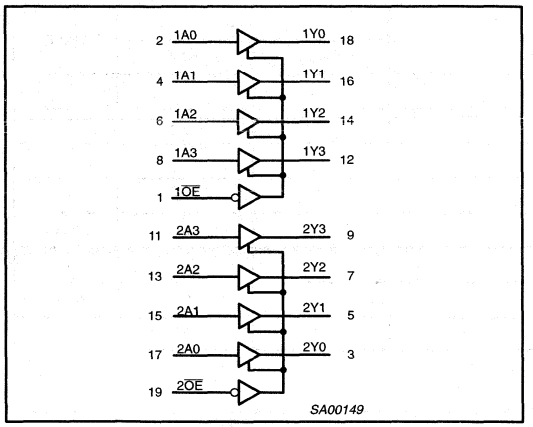
PIN CONFIGURATION



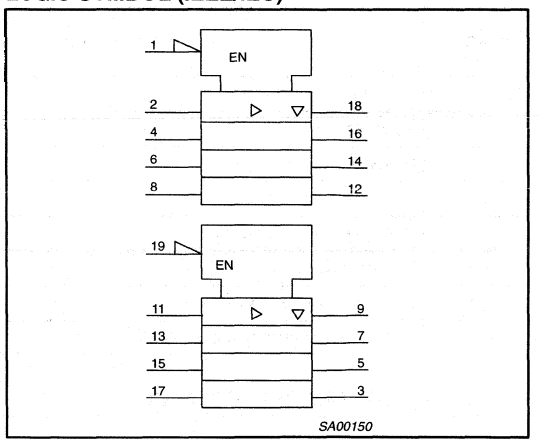
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	1Yn	2Yn
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output HIgh leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–40	–100	–180	–40	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

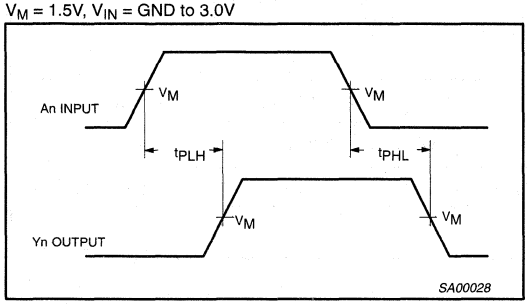
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

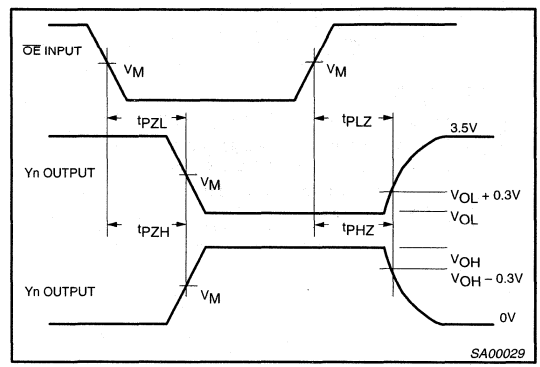
SYMBOL	PARAMETER	WAVEFORM	74ABT244					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 2.1	3.1 4.1	4.6 5.6	1.1 2.1	5.1 6.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.1 1.7	4.1 2.7	5.6 5.2	2.1 1.7	6.6 5.7	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

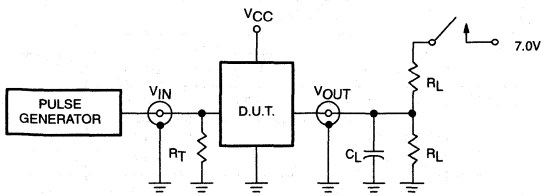


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

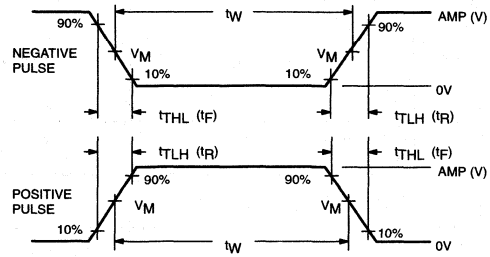


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal buffer/line driver with 30Ω series termination resistors (3-State)

74ABT2244

FEATURES

- Octal bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω, making external termination resistors unnecessary
- Output capability: +5mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Same part as 74ABT244-1
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT2244 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT2244 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

The 74ABT2244 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

The 74ABT2244 is the same as the 74ABT244-1. The part number has been changed to reflect industry standards.

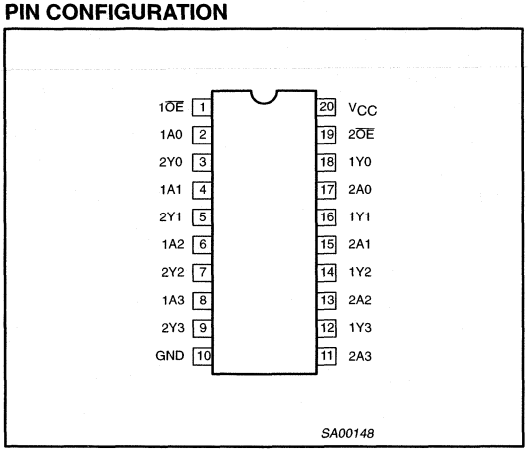
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.8 3.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT2244 N	74ABT2244 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT2244 D	74ABT2244 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT2244 DB	74ABT2244 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT2244 PW	7ABT2244PW DH	SOT360-1

PIN CONFIGURATION



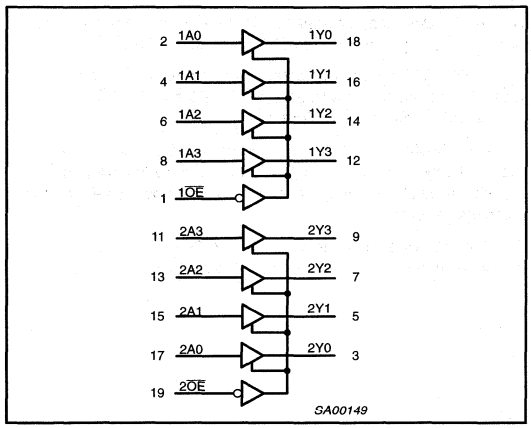
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

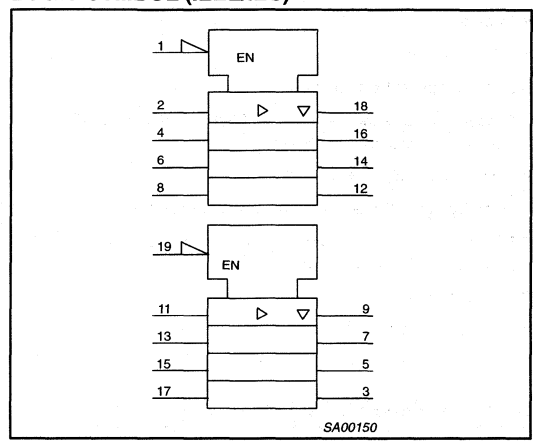
Octal buffer/line driver with 30Ω series termination resistors (3-State)

74ABT2244

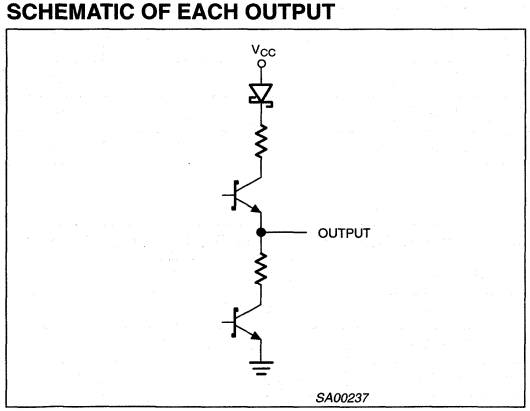
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	$2\overline{OE}$	2An	1Yn	2Yn
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 5mA; V_I = V_{IL} or V_{IH}		0.32	0.55		0.55	V
		V_{CC} = 4.5V; I_{OL} = 12mA; V_I = V_{IL} or V_{IH}			0.8		0.8	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		5.0	100		100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		5.0	50		50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		0.1	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−0.1	−50		−50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−100	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

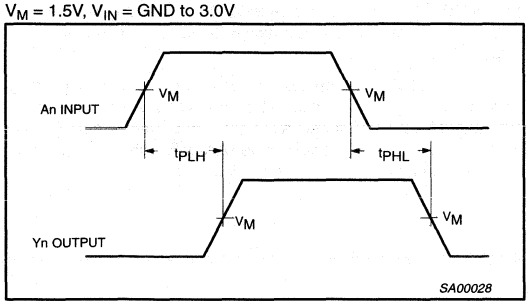
AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

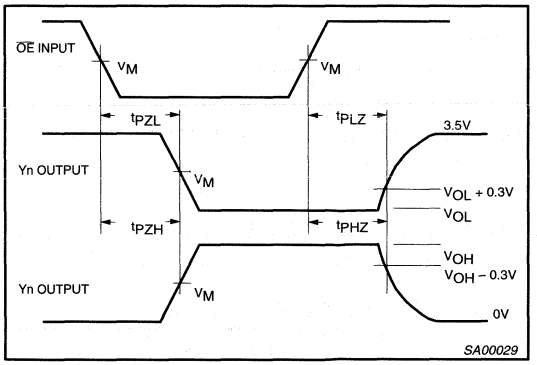
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.8 3.9	4.3 5.3	1.0 1.0	4.7 5.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 2.1	3.3 5.0	4.8 7.3	1.1 2.1	5.5 8.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.1 1.7	3.7 3.4	5.6 5.3	2.1 1.7	6.6 5.8	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

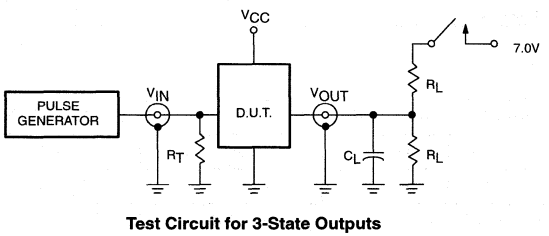


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

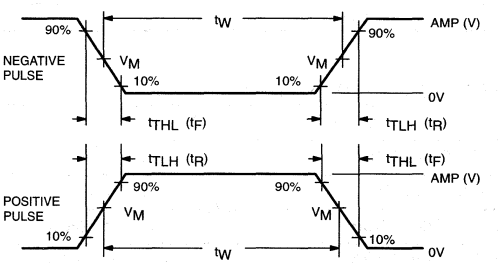


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal transceiver with direction pin (3-State) 74ABT245

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 833 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT245 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

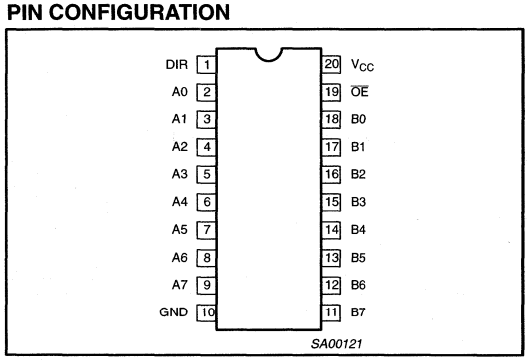
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.2 2.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT245 N	74ABT245 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT245 D	74ABT245 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT245 DB	74ABT245 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT245 PW	74ABT245PW DH	SOT360-1

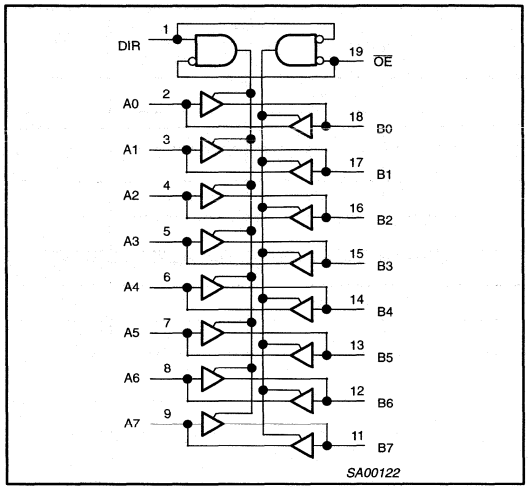
PIN CONFIGURATION



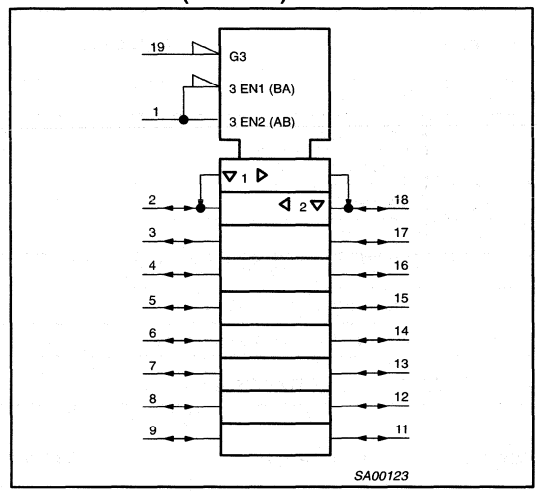
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	An = Bn	Inputs
L	H	Inputs	Bn = An
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]		V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–40	–100	–180	–40	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

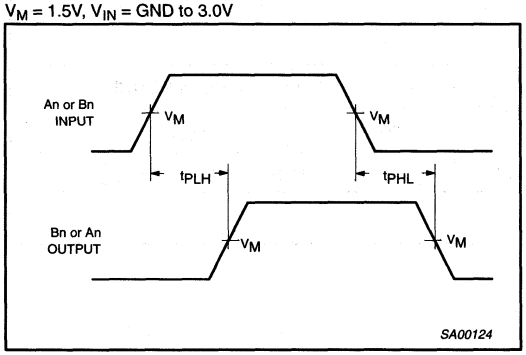
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

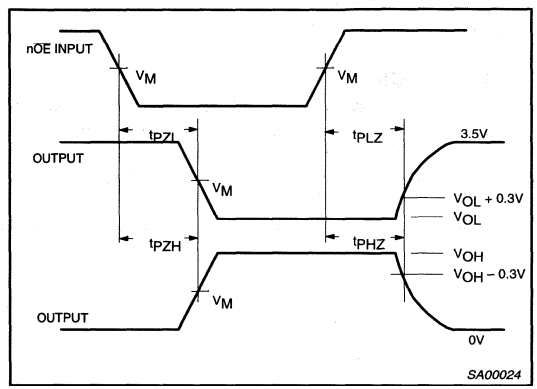
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.2 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 2.3	3.0 4.0	4.8 5.8	1.3 2.3	5.3 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.0 1.0	4.7 4.1	6.2 5.8	1.0 1.0	7.2 6.3	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

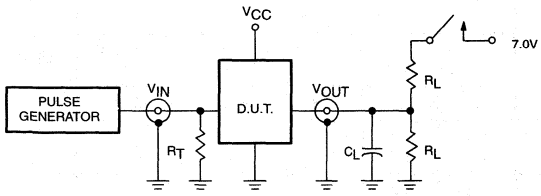


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

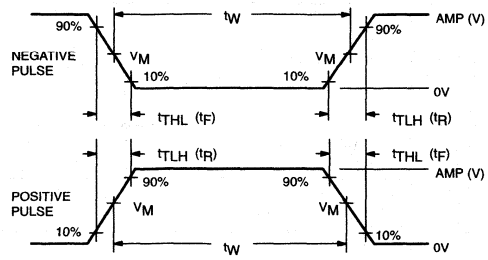


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal transceiver with direction pin and 30Ω series termination resistors (3-State)

74ABT2245

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +12mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 833 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted
- Same as 74ABT245-1
- Outputs include series resistance of 30Ω, making external termination resistors unnecessary
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT2245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT2245 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

The 74ABT2245 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

The 74ABT2245 is the same as the 74ABT245-1. The part number has been changed to reflect industry standards.

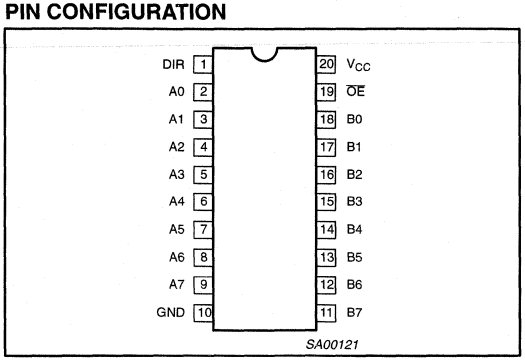
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT2245 N	74ABT2245 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT2245 D	74ABT2245 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT2245 DB	74ABT2245 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT2245 PW	7ABT2245PW DH	SOT360-1

PIN CONFIGURATION

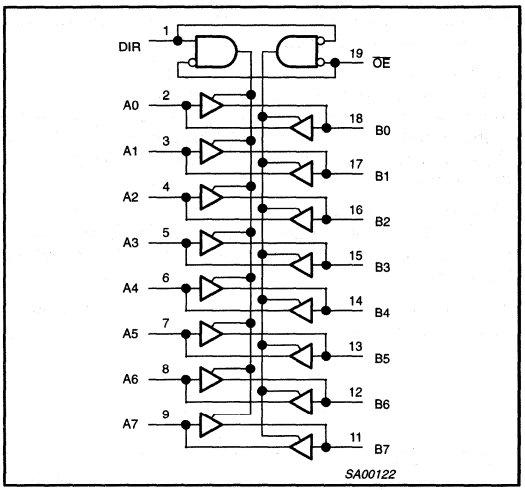


PIN DESCRIPTION

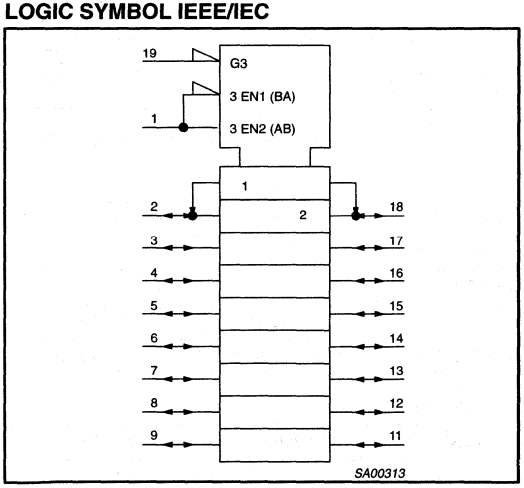
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal transceiver with direction pin and 30Ω series termination resistors (3-State) 74ABT2245

LOGIC SYMBOL



LOGIC SYMBOL IEEE/IEC

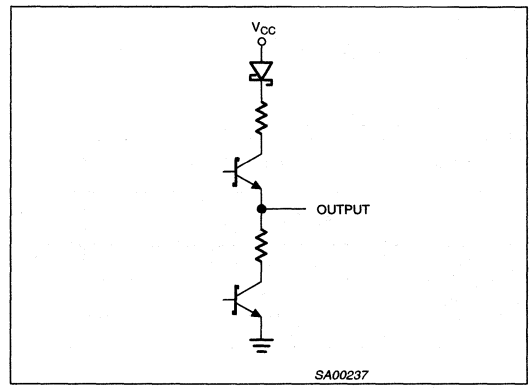


FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	An = Bn	Inputs
L	H	Inputs	Bn = An
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

SCHEMATIC OF EACH OUTPUT



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 5mA; V_I = V_{IL} or V_{IH}		0.32	0.55		0.55	V
			V_{CC} = 4.5V; I_{OL} = 12mA; V_I = V_{IL} or V_{IH}		0.5	0.8		0.8	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_{CEX}	Output high leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	−40	−100	−180	−40	−180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

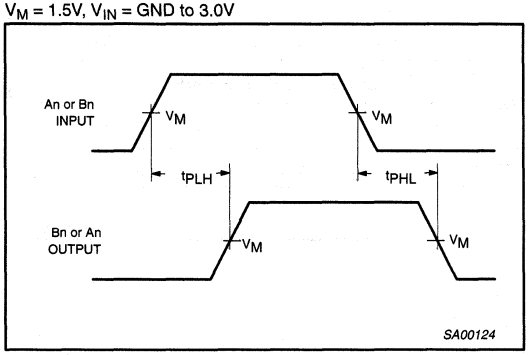
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

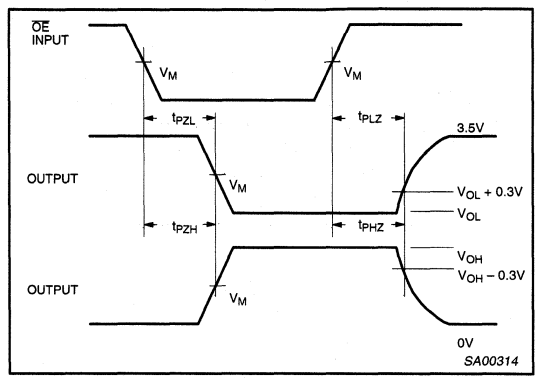
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.8 3.9	4.2 5.0	1.0 1.0	4.7 5.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 3.0	3.5 5.5	4.6 7.0	1.3 3.0	5.5 7.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.0	4.0 3.4	5.4 4.6	1.5 1.0	6.3 5.0	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

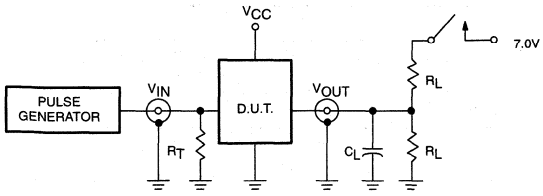


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

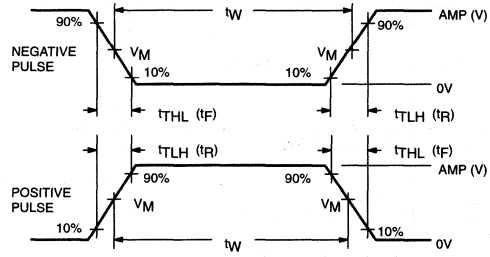


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal D-type flip-flop 74ABT273A

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- Power-up reset
- See 74ABT377 for clock enable version
- See 74ABT373 for transparent latch version
- See 74ABT374 for 3-State version
- ESD protection exceeds 2000 V per Mil Std 833 Method 3015 and 200 V per machine model.

DESCRIPTION

The 74ABT273A has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

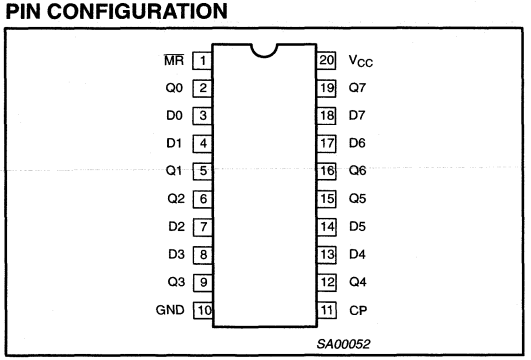
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	3.0 3.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	pF
I_{CCH}	Total supply current	Outputs High; V_{CC} =5.5V	150	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT273A N	74ABT273A N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT273A D	74ABT273A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT273A DB	74ABT273A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT273A PW	7ABT273APW DH	SOT360-1

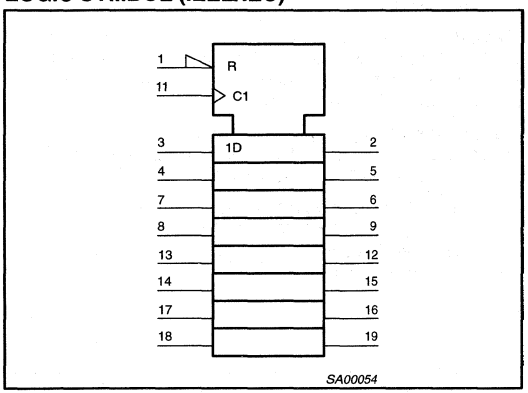
PIN CONFIGURATION



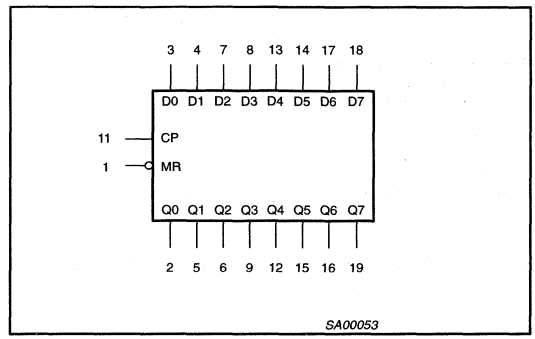
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock pulse input (active rising edge)
3, 4, 7, 8, 13, 14, 17, 18	D0 - D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 - Q7	Data outputs
1	$\overline{MR}$	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

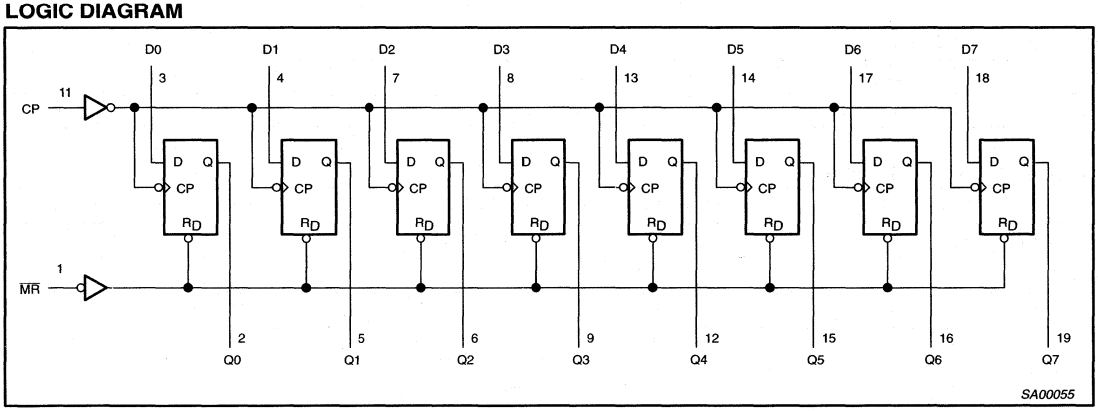
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	Dn	Q0 - Q7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-70	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		150	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	250	350		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.5 2.0	3.0 3.4	4.0 4.6	1.5 2.0	4.8 4.8	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2	2.5	4.5	6.0	2.5	6.6	ns

AC SETUP REQUIREMENTS

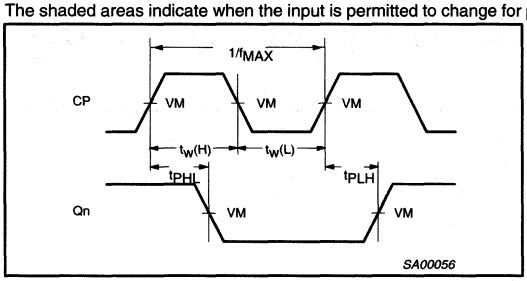
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	3	1.5 1.5	0.6 0.4	1.5 1.5	
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	3	0.7 0.7	-0.5 -0.5	0.7 0.7	ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	1	1.5 2.0	0.8 1.0	1.5 2.0	ns
$t_w(L)$	Master Reset pulse width, Low	2	1.5	0.8	1.5	ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5	0.5	1.5	ns

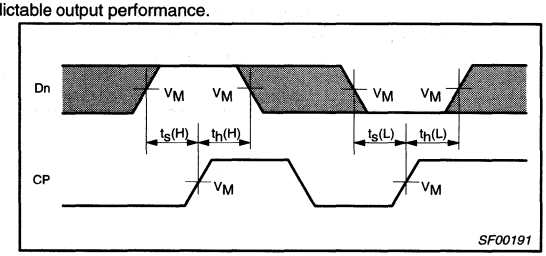
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

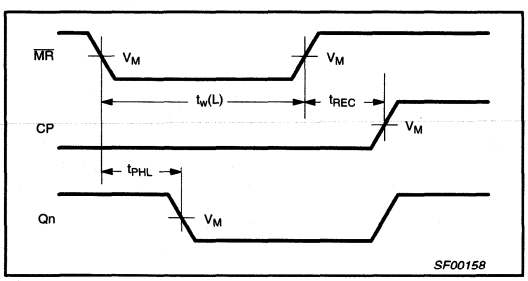
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

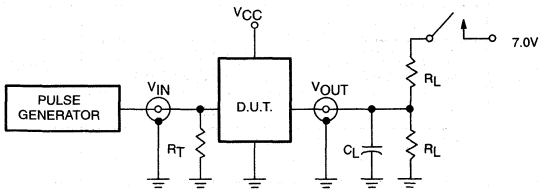


Waveform 3. Data Setup and Hold Times

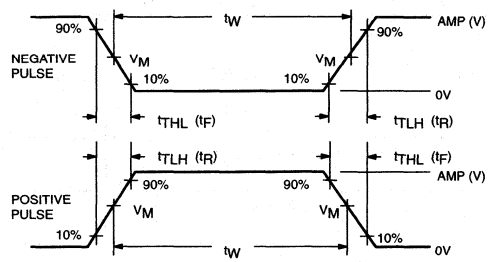


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
All	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00057

Octal transparent latch (3-State) 74ABT373A

FEATURES

- 8-bit transparent latch
- 3-State output buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT373A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT373A device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

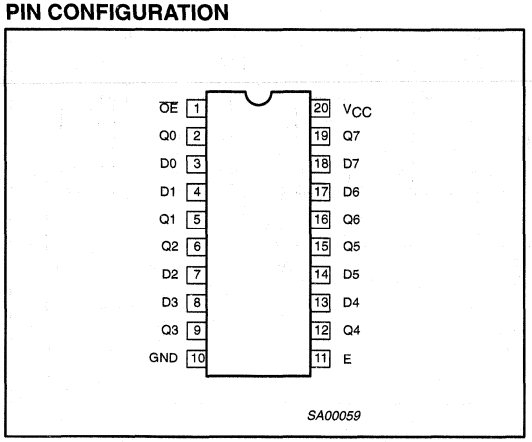
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	3.2 3.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	100	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT373A N	74ABT373A N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT373A D	74ABT373A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT373A DB	74ABTD373A B	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT373A PW	7ABT373APW DH	SOT360-1

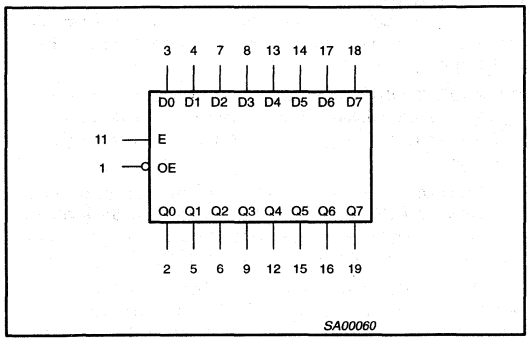
PIN CONFIGURATION



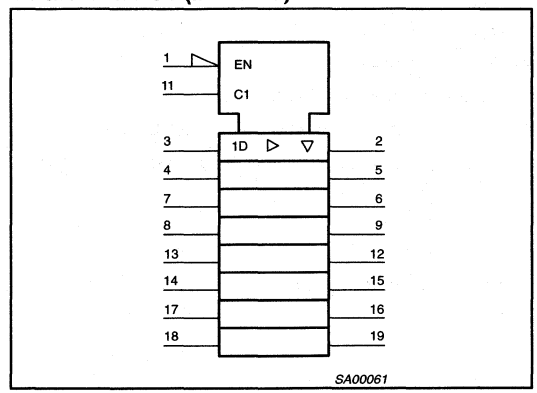
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

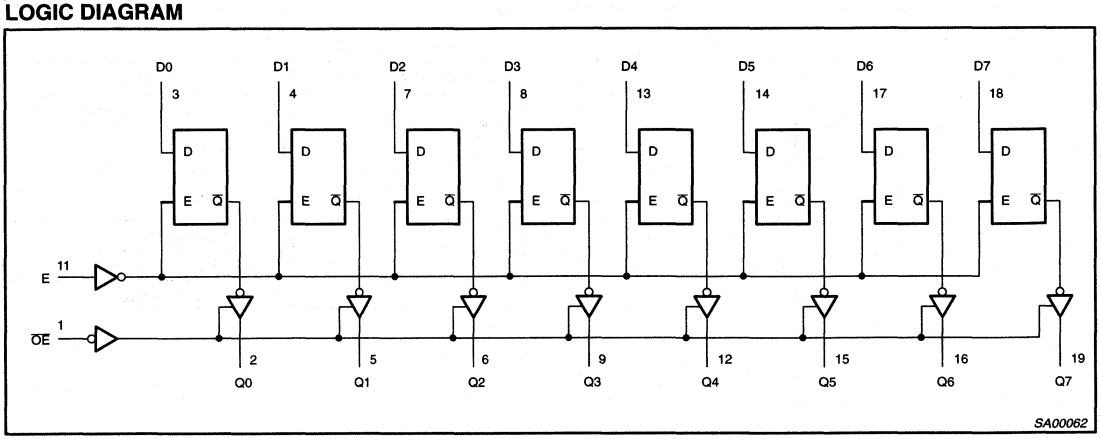


FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn	REGISTER	Q0 – Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.3	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; $V_{\overline{OE}}$ = Don't Care V_1 = GND or V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		0.1	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–0.1	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		100	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		100	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	2	1.4 1.4	3.2 3.6	4.2 4.7	1.4 1.4	4.7 5.1	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	1	1.4 1.9	3.2 3.7	4.2 4.8	1.4 1.9	4.8 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.2 2.1	3.1 4.2	4.2 5.2	1.2 2.1	5.1 5.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.3 1.2	3.4 3.0	4.6 4.1	1.3 1.2	5.1 4.3	ns

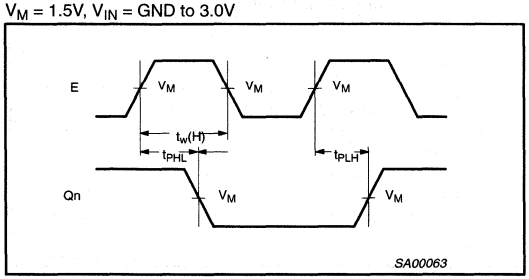
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

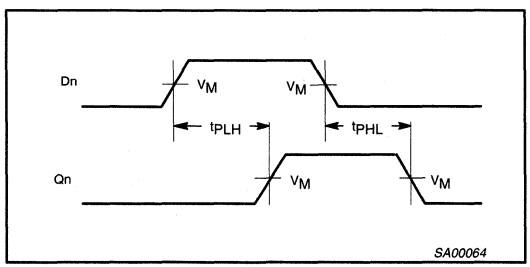
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to E	3	1.5 1.0	0.7 0.4	1.5 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to E	3	1.0 1.0	0.0 –0.5	1.0 1.0	ns
$t_w(H)$	E pulse width High	1	2.5	1.7	2.5	ns

AC WAVEFORMS

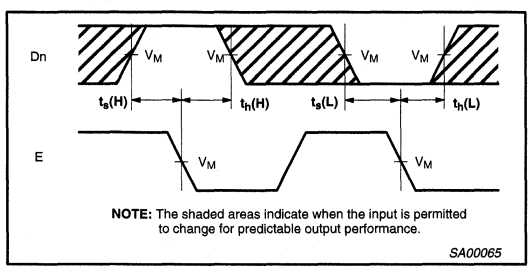
V_M = 1.5V, V_{IN} = GND to 3.0V



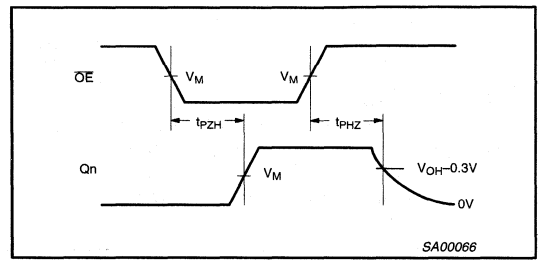
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



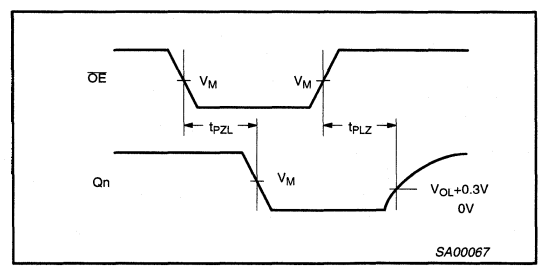
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

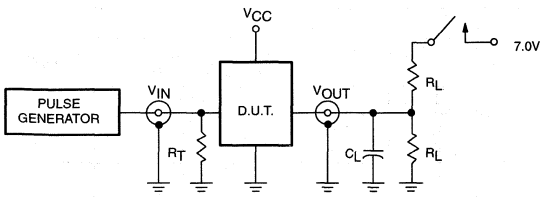


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

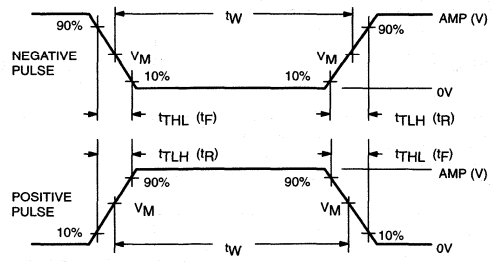


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal D-type flip-flop; positive-edge trigger (3-State)

74ABT374A

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT374A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT374A is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

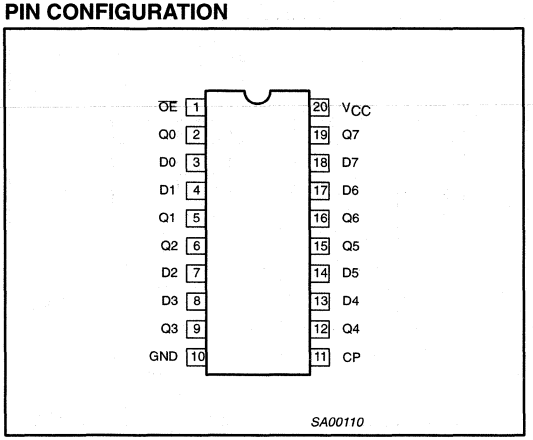
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	3.4 3.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT374A N	74ABT374A N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT374A D	74ABT374A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT374A DB	74ABT374A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT374A PW	7ABT374APW DH	SOT360-1

PIN CONFIGURATION



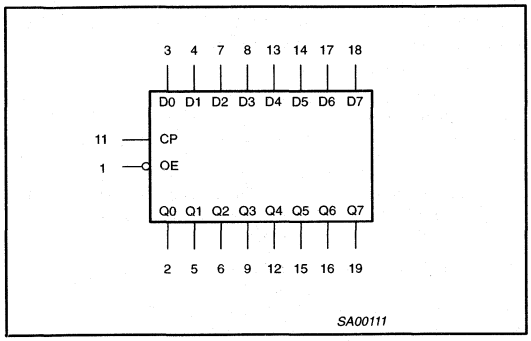
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

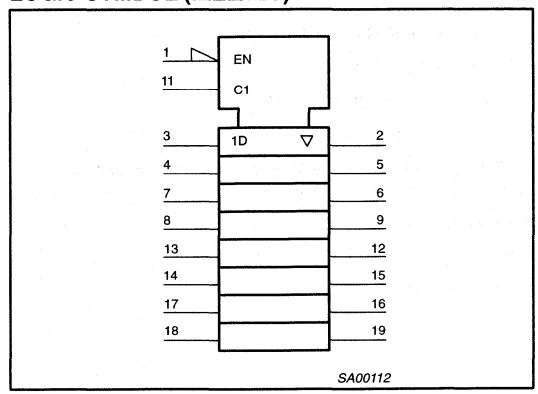
Octal D-type flip-flop; positive-edge trigger (3-State)

74ABT374A

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

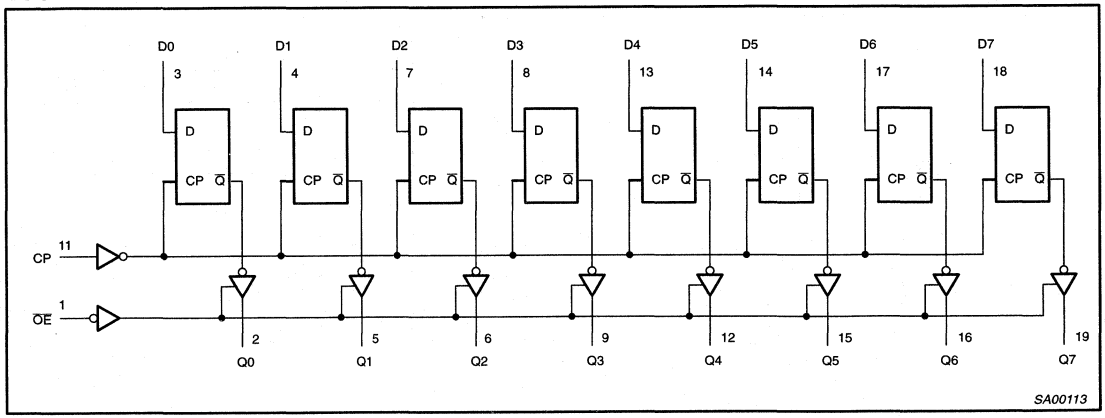


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn		Q0 – Q7	
L	↑	l	L	L	Latch and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 0.0V; I_O = 1mA; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = Don't Care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 0.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−100	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	200	300		200		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.7 2.0	3.4 3.8	4.5 4.9	1.7 2.0	5.1 5.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.2 2.2	3.5 4.3	4.5 5.4	1.2 2.2	5.4 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.8 1.5	3.6 3.0	4.7 4.1	1.8 1.5	5.2 4.3	ns

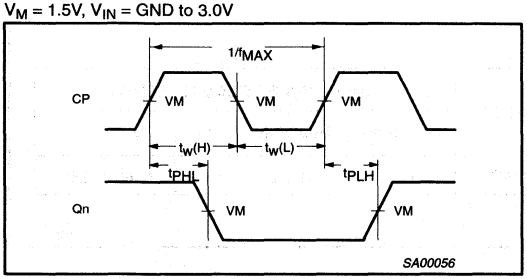
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

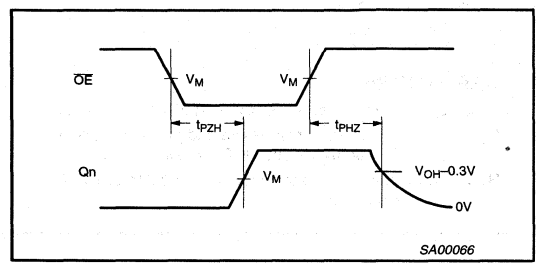
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	2	1.5 1.2	0.6 0.3	1.5 1.2	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	2	1.0 1.0	–0.3 –0.5	1.0 1.0	ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	1	2.0 2.8	0.8 1.0	2.0 2.8	ns

AC WAVEFORMS

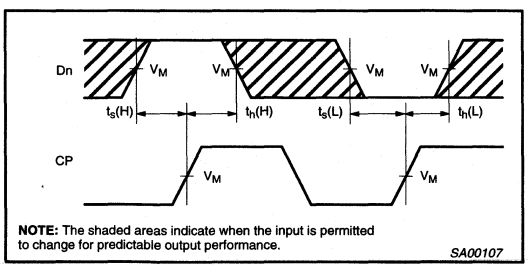
V_M = 1.5V, V_{IN} = GND to 3.0V



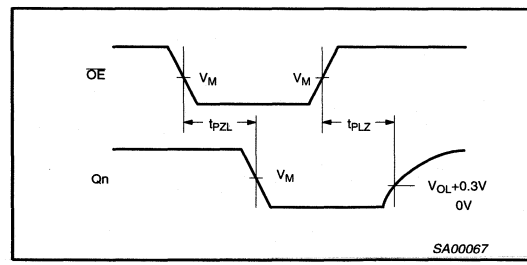
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

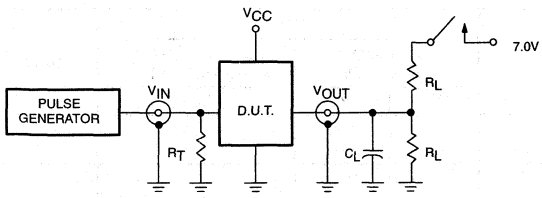


Waveform 2. Data Setup and Hold Times

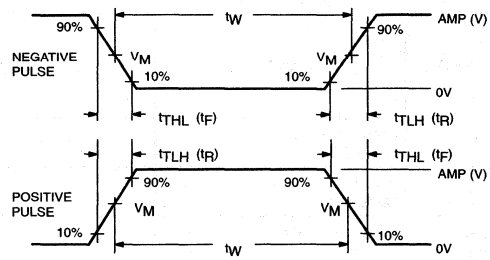


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal D-type flip-flop with enable | 74ABT377A

FEATURES

- Ideal for addressable register applications
- 8-bit positive edge-triggered register
- Enable for address and data synchronization applications
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up reset

DESCRIPTION

The 74ABT377A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT377A has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneousiy when the Enable ($\overline{E}$) input is Low.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

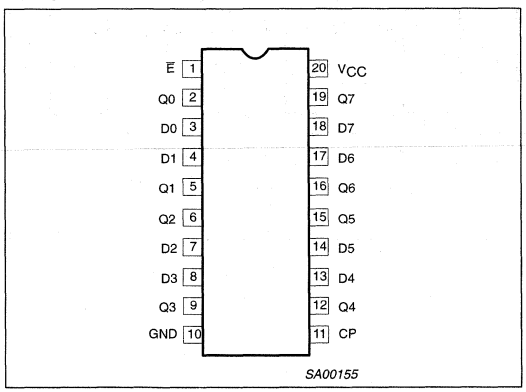
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	3.1 3.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
I_{CCH}	Total current supply	Outputs High; V_{CC} = 5.5V	500	nA

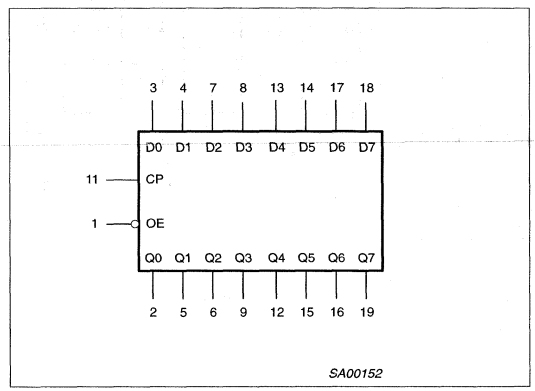
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT377A N	74ABT377A N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT377A D	74ABT377A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT377A DB	74ABT377A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT377A PW	7ABT377PWA DH	SOT360-1

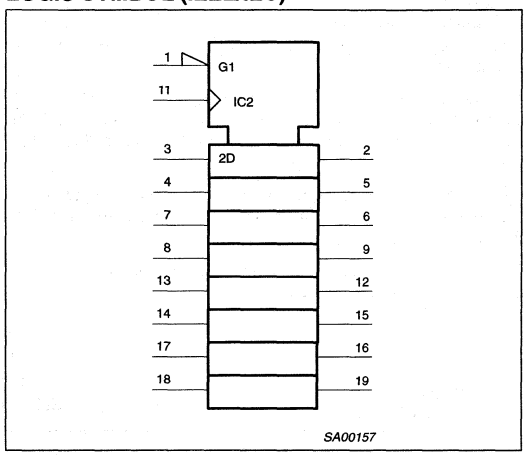
PIN CONFIGURATION



LOGIC SYMBOL



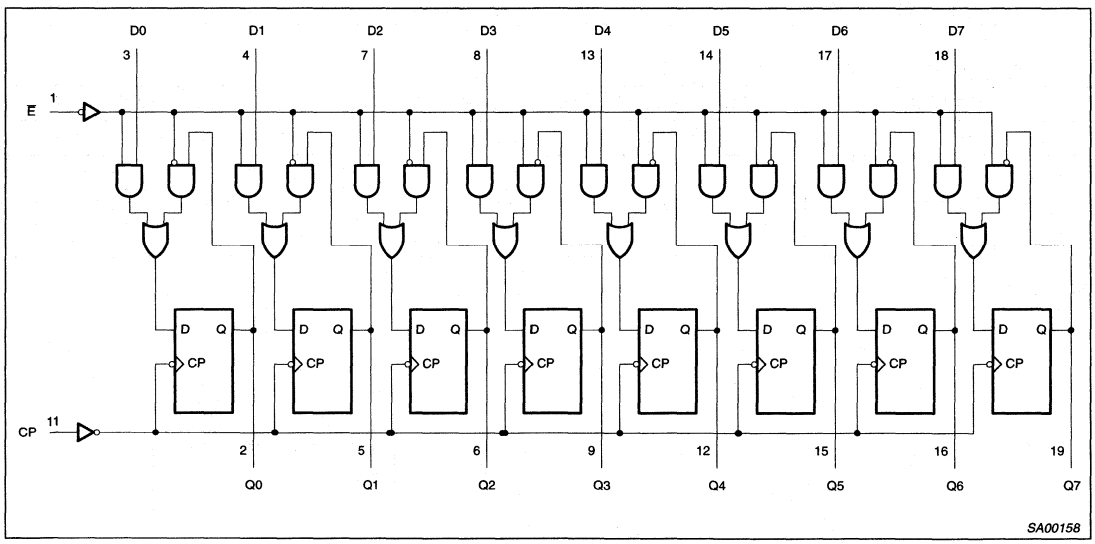
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{E}$	Enable input (active–Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	Dn	Qn	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS[1]					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	150	250		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.8 2.2	3.1 3.6	4.0 4.7	1.8 2.2	4.8 4.9	ns

NOTE:
1. Limits may vary among suppliers.

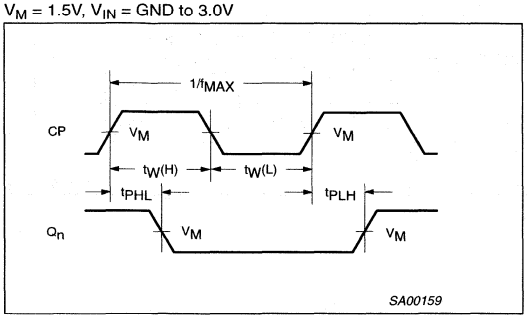
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

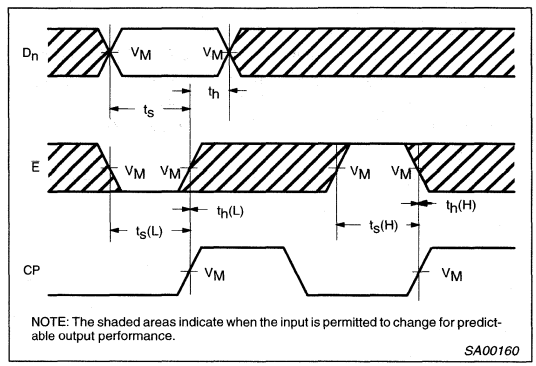
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	2	1.5 1.5	0.7 0.5	1.5 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	2	1.0 1.0	–0.4 –0.6	1.0 1.0	ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	2	2.0 2.0	1.1 1.0	2.0 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	2	1.0 1.0	–0.9 –0.1	1.0 1.0	ns
$t_w(H)$ $t_w(L)$	Clock Pulse width High or Low	1	1.5 2.0	0.7 1.0	1.5 2.0	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

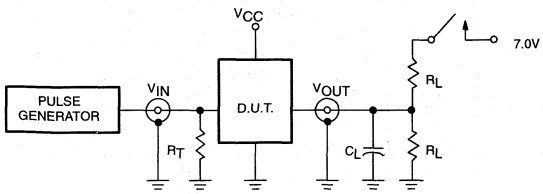


Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency

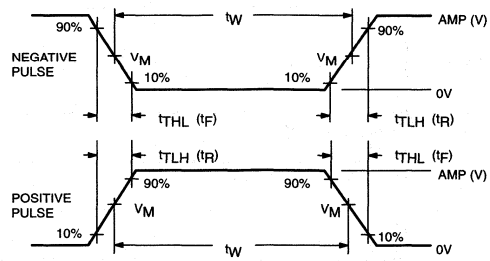


Waveform 2. Data and Enable Setup and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
All	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00057

Octal D-type flip-flop, inverting (3-State) 74ABT534A

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT534A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT534A is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

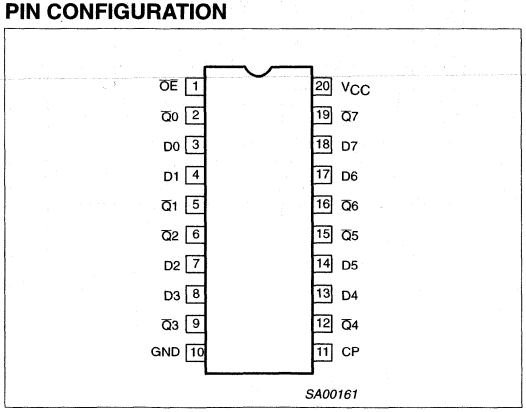
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}$n	C_L = 50pF; V_{CC} = 5V	3.3 3.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	6.5	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT534A N	74ABT534A N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT534A D	74ABT534A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT534A DB	74ABT534A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT534A PW	7ABT534APW DH	SOT360-1

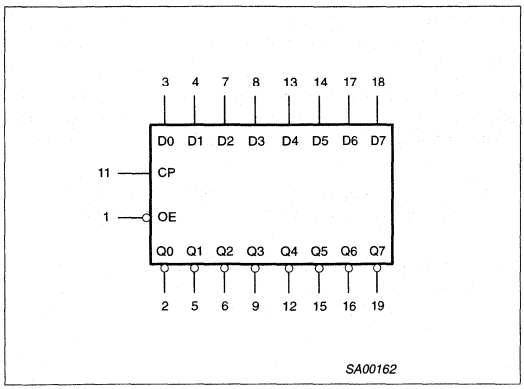
PIN CONFIGURATION



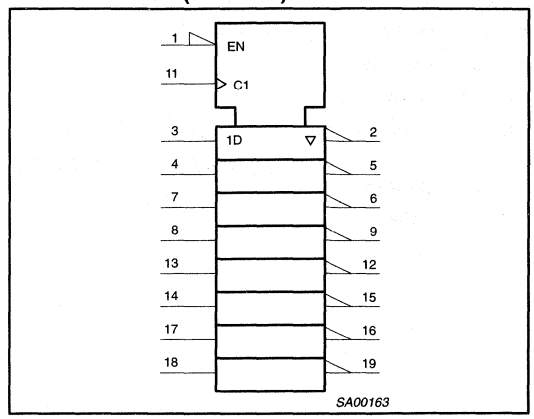
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}$0-$\overline{Q}$7	Inverting 3-State outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

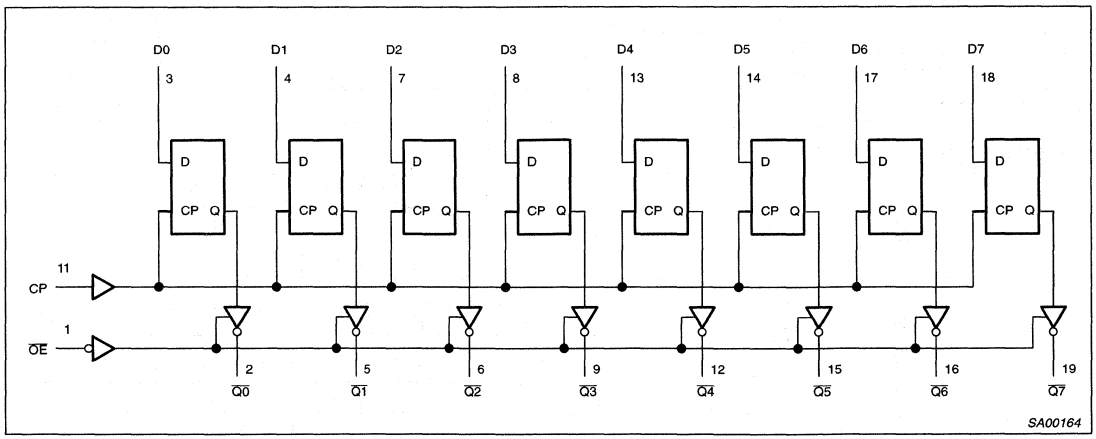


FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	$\overline{Q0} - \overline{Q7}$	
L	↑	l	L	H	Latch and read register
L	↑	h	H	L	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		0.1	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−0.1	−10		−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		0.1	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−100	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		100	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		100	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	350		125		ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}$n	1	2.0[1] 2.4[1]	3.3 3.6	4.2[1] 4.7[1]	2.0 2.4	5.0[1] 5.1[1]	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.0 2.6	3.1 3.9	4.2 4.9[1]	1.0 2.6	5.0 5.5[1]	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.8[1] 1.6[1]	3.3 2.8	4.3[1] 3.6[1]	1.8[1] 1.6[1]	4.6[1] 4.1[1]	ns

NOTE:
1. This datasheet limit may vary among suppliers.

AC SETUP REQUIREMENTS

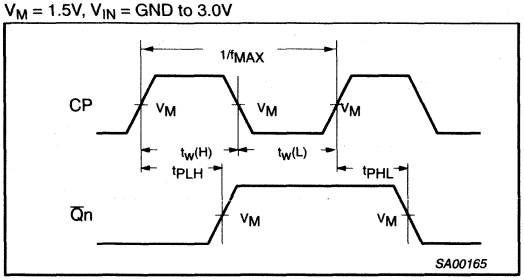
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	2	1.0[1] 1.0[1]	0.4 0.3	1.0[1] 1.0[1]	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	2	0.5 0.5	–0.3 –0.4	0.5 0.5	ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	1	1.5[1] 2.0[1]	0.8 1.0	1.5[1] 2.0[1]	ns

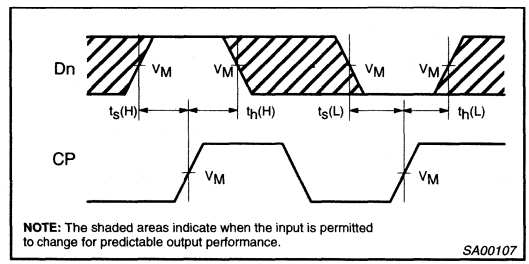
NOTE:
1. This datasheet limit may vary among suppliers.

AC WAVEFORMS

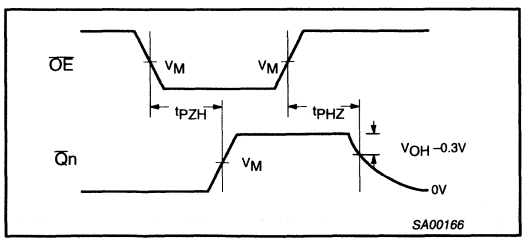
V_M = 1.5V, V_{IN} = GND to 3.0V



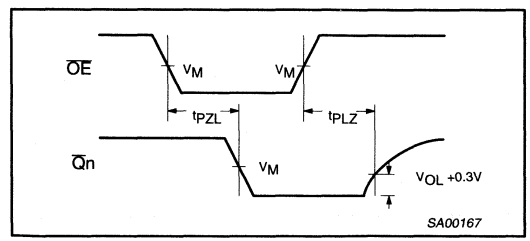
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

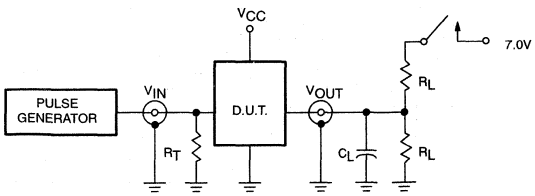


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

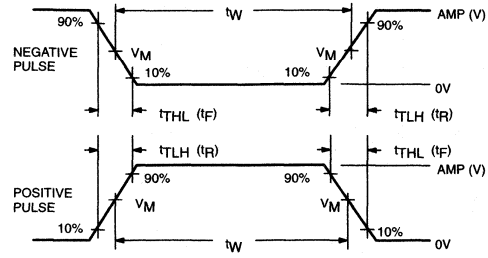


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal buffer, inverting (3-State) 74ABT540

FEATURES

- Octal bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Efficient pinout to facilitate PC board layout
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT540 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT540 device is an octal inverting buffer that is ideal for driving bus lines. The device features input and outputs on opposite sides of the package to facilitate printed circuit board layout.

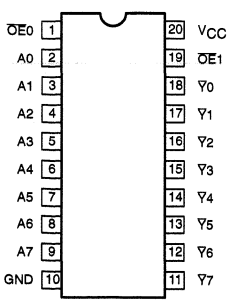
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	μA

ORDERING INFORMATION

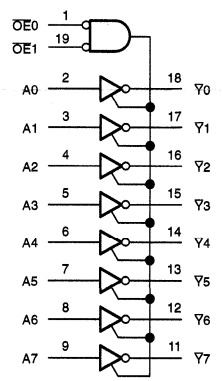
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT540 N	74ABT540 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT540 D	74ABT540 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT540 DB	74ABT540 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT540 PW	74ABT540PW DH	SOT360-1

PIN CONFIGURATION



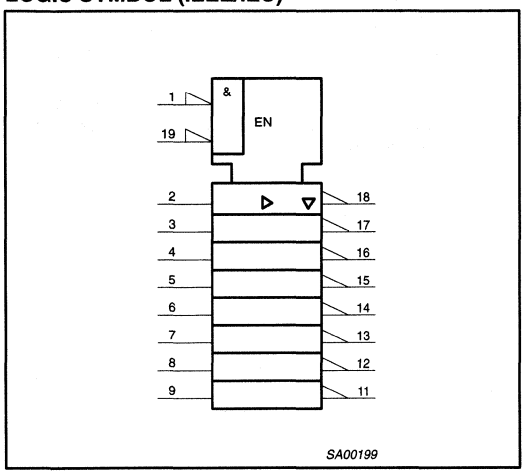
SA00197

LOGIC SYMBOL



SA00198

LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}0 - \overline{Y}7$	Data outputs
1, 19	$\overline{OE}0$, $\overline{OE}1$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}0$	$\overline{OE}1$	An	$\overline{Y}n$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	mA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

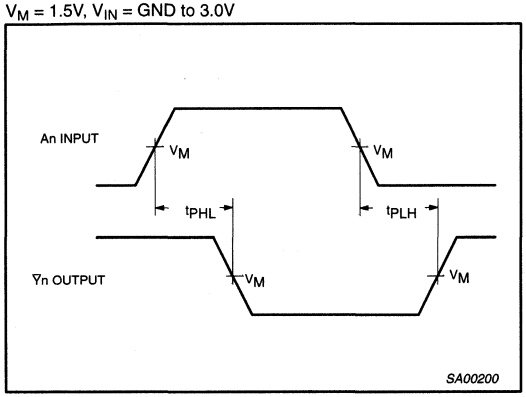
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

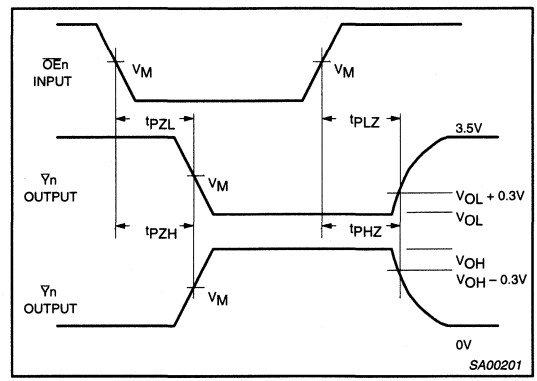
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	1	1.0 1.0	2.9 3.1	4.1 4.3	1.0 1.0	4.8 4.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.1	4.1 4.6	4.9 5.8	1.1 1.1	5.9 6.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.2	3.6 2.9	6.8 5.7	1.5 1.2	7.3 6.2	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

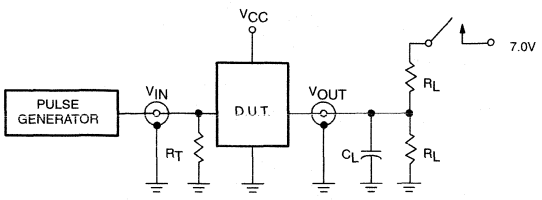


Waveform 1. Waveforms Showing the Input (An) to Output ($\overline{Y}$n) Propagation Delays

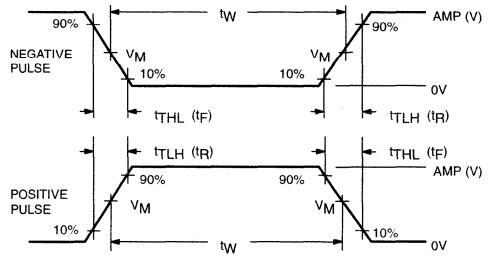


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal buffer/line driver (3-State) 74ABT541

FEATURES

- Octal bus interface
- Functions similar to the 'ABT241
- Provides ideal interface and increases fan-out of MOS Microprocessors
- Efficient pinout to facilitate PC board layout
- 3-State buffer outputs sink 64mA and source 32mA
- Power-up 3-State
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT541 device is an octal buffer that is ideal for driving bus lines. The outputs are all capable of sinking 64mA and sourcing 32mA. The device features input and outputs on opposite sides of the package to facilitate printed circuit board layout.

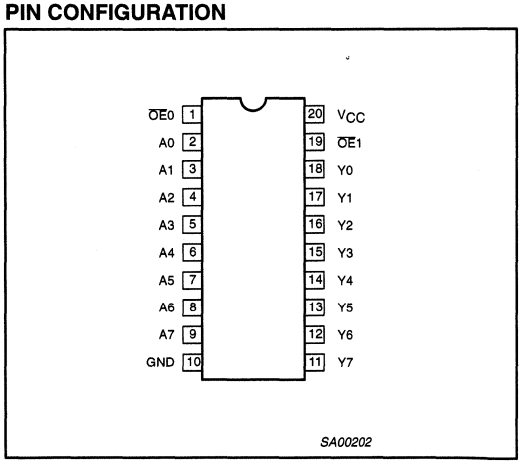
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

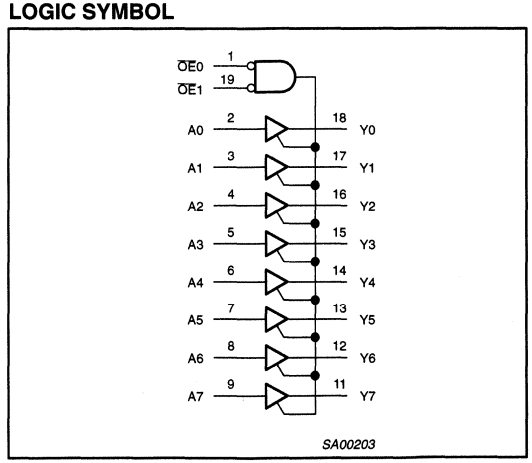
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT541 N	74ABT541 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT541 D	74ABT541 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT541 DB	74ABT541 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT541 PW	74ABT541PW DH	SOT360-1

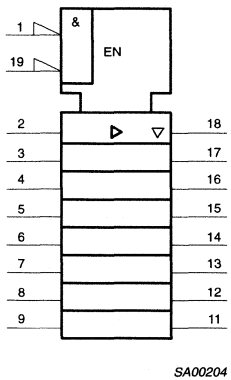
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs
18, 17, 16, 15, 14, 13, 12, 11	Y0 – Y7	Data outputs
1, 19	$\overline{OE}0$, $\overline{OE}1$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}0$	$\overline{OE}1$	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-state output current[3]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–40	–100	–180	–40	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

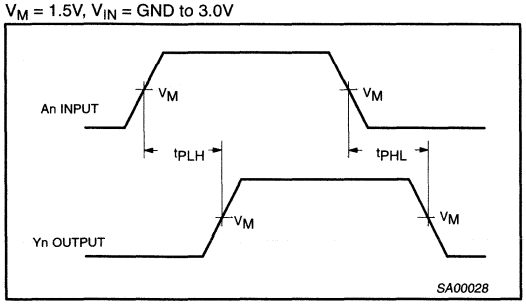
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

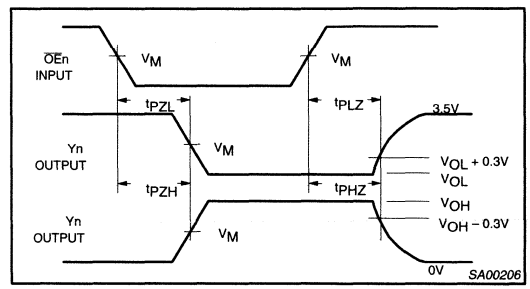
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{amb} = +25°C$ $V_{CC} = +5.0V$			$T_{amb} = -40°C$ to $+85°C$ $V_{CC} = +5.0V \pm 0.5V$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 2.1	3.1 4.4	4.8 5.9	1.1 2.1	5.3 6.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.1 1.7	5.1 4.7	6.6 6.2	2.1 1.7	7.1 6.7	ns

AC WAVEFORMS

$V_M = 1.5V$, V_{IN} = GND to 3.0V

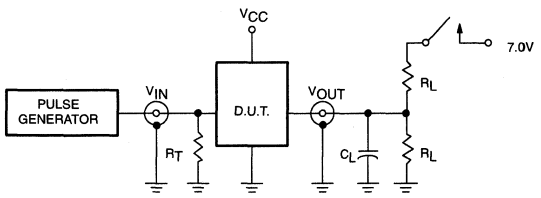


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

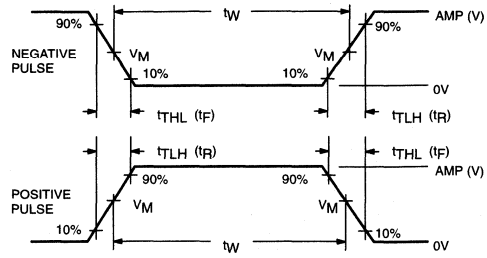


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal latched transceiver with dual enable (3-State)

74ABT543A

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/–32mA
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT543A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT543A Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 74ABT543A contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

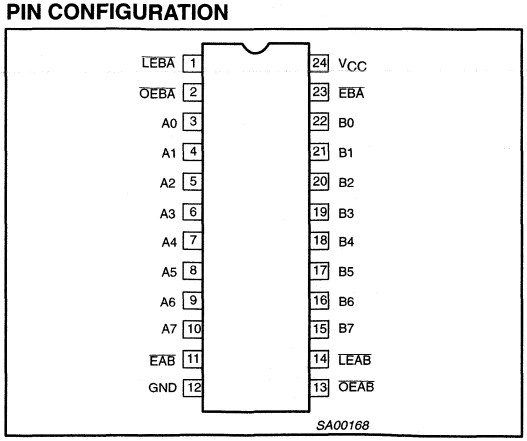
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9 3.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT543A N	74ABT543A N	SOT222-1
20-Pin plastic SO	–40°C to +85°C	74ABT543A D	74ABT543A D	SOT137-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT543A DB	74ABT543A DB	SOT340-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT543A PW	7ABT543APW DH	SOT355-1

PIN CONFIGURATION



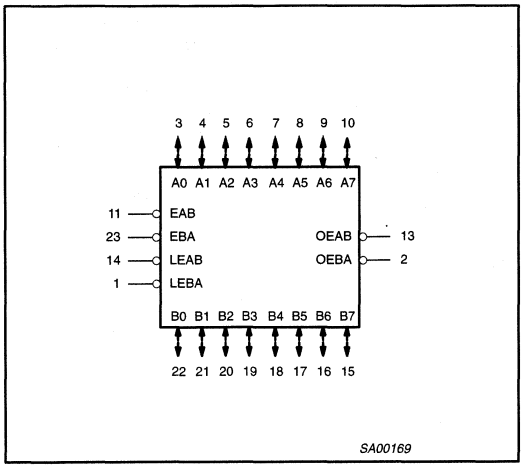
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (active-Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (active-Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	A0 – A7	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	B0 – B7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

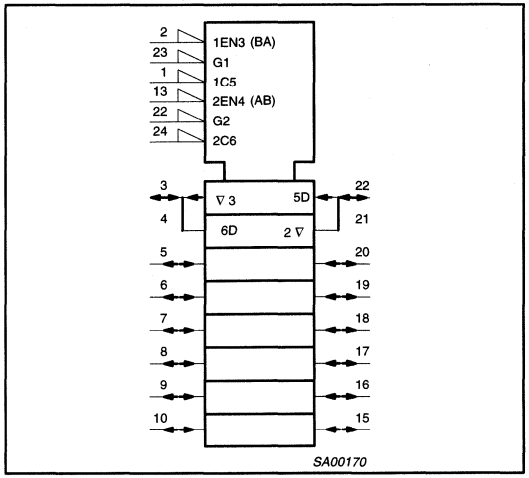
Octal latched transceiver with dual enable (3-State)

74ABT543A

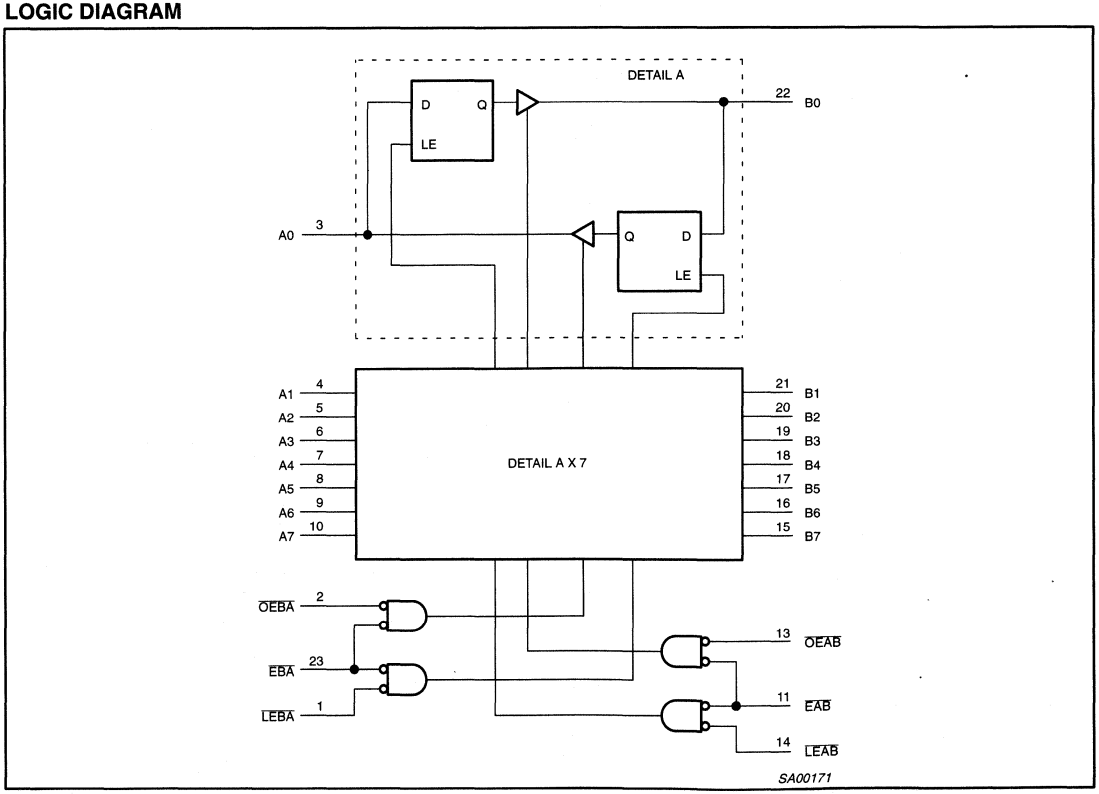
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	EXX	$\overline{LEXX}$	An or Bn	Bn or An	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.2		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.7		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.3		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.3	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5V; I_O = 1mA; VI = GND or V_{CC}		0.13	.55		.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–40	–65	–180	–40	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	2	1.0 1.9	2.9 3.6	4.5 5.2	1.0 1.9	5.2 5.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	1 2	1.0 2.1	3.4 4.3	5.1 6.0	1.0 2.1	6.2 6.7	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	1.0 2.0	3.2 4.3	5.1 5.9	1.0 2.0	6.2 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	2.0 1.0	4.0 3.0	5.7 4.6	2.0 1.0	6.2 5.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	1.0 2.0	3.4 4.4	5.1 6.1	1.0 2.0	6.2 6.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	2.0 1.0	3.6 3.0	5.4 4.6	2.0 1.0	5.9 5.0	ns

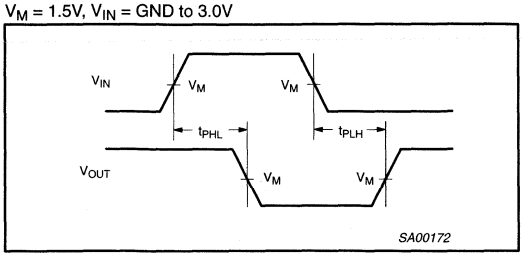
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

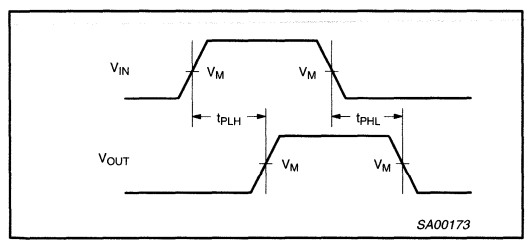
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	2.5 3.0	1.0 1.4	2.5 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	0.5 0.5	–0.8 –0.6	0.5 0.5	ns
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	3.5 3.0	1.3 1.4	3.5 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	0.5 0.5	–0.8 –0.6	0.5 0.5	ns
$t_w(L)$	Latch enable pulse width, Low	3	3.5	1.0	3.5	ns

AC WAVEFORMS

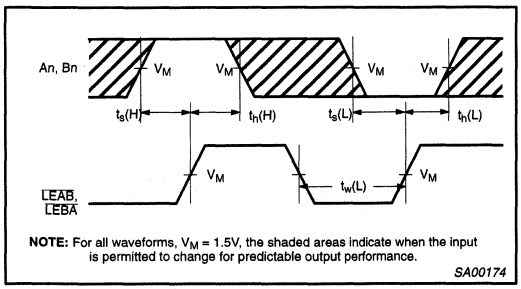
V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Propagation Delay For Inverting Output

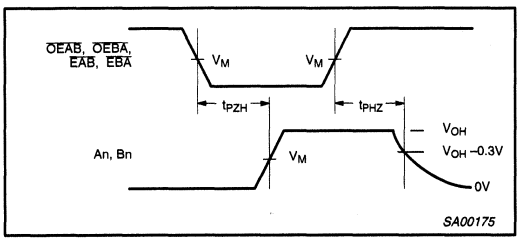


Waveform 2. Propagation Delay For Non-Inverting Output

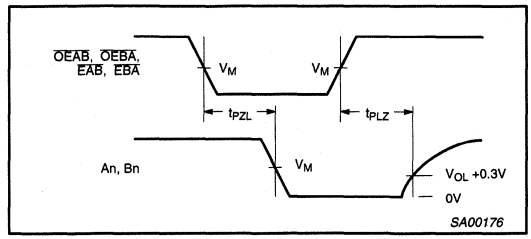


NOTE: For all waveforms, V_M = 1.5V, the shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data Setup and Hold Times And Latch Enable Pulse Width

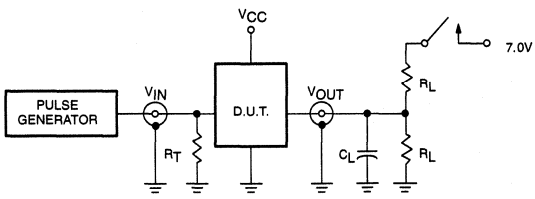


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

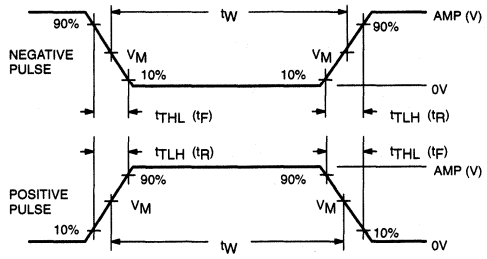


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal latched transceiver with dual enable, inverting (3-State)

74ABT544

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/–32mA
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT544 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 74ABT544 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and invert the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

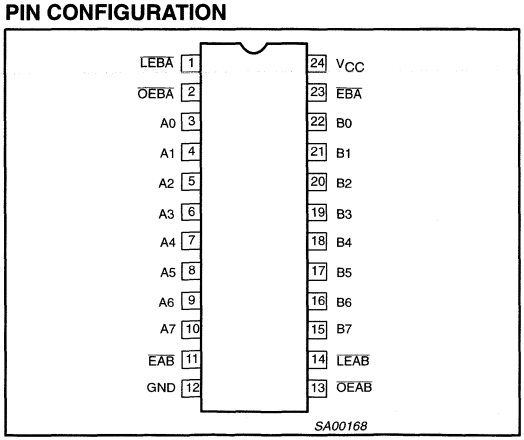
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay $\overline{An}$ to $\overline{Bn}$ or $\overline{Bn}$ to $\overline{An}$	C_L = 50pF; V_{CC} = 5V	3.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	110	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT544 N	74ABT544 N	SOT222-1
20-Pin plastic SO	–40°C to +85°C	74ABT544 D	74ABT544 D	SOT137-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT544 DB	74ABT544 DB	SOT340-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT544 PW	74ABT544PW DH	SOT355-1

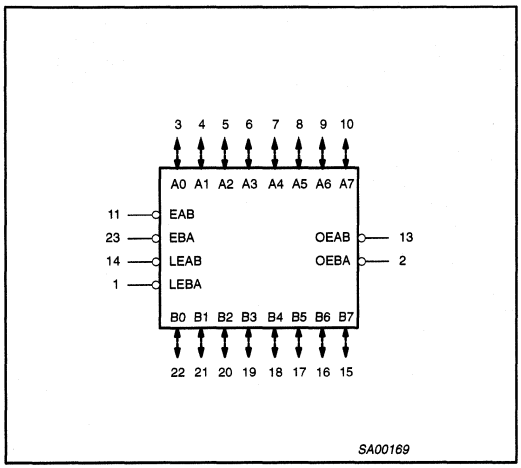
PIN CONFIGURATION



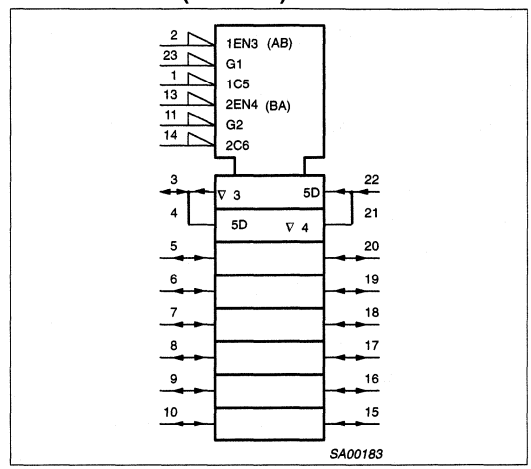
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (active-Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (active-Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	$\overline{A0}$ – $\overline{A7}$	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	$\overline{B0}$ – $\overline{B7}$	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

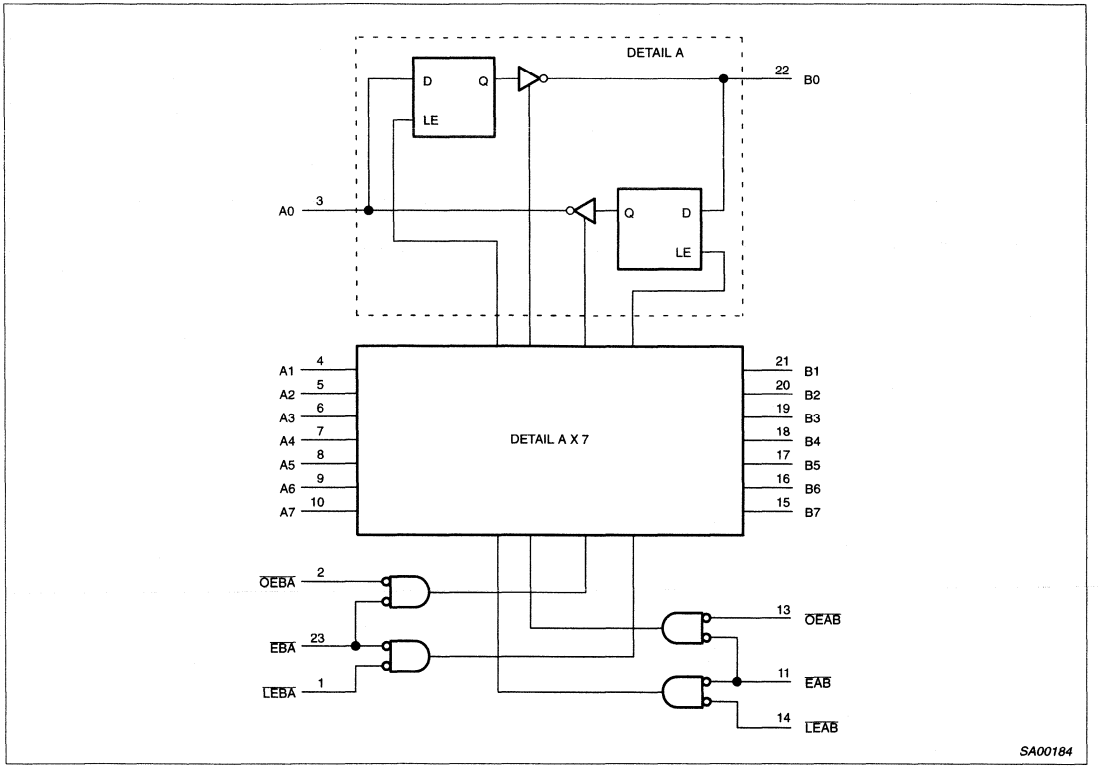


FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	EXX	$\overline{LEXX}$	An or Bn	An or Bn	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	L H	Latch + Display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
NC= No change
Z = High impedance or "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.2		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.7		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.3		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current — Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
	Input leakage current — Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–65	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip–flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition of 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	2	1.1 1.4	3.6 3.9	5.1 5.4	1.1 1.4	6.1 6.4	ns
t_{PLH} t_{PHL}	Propagation delay LEBA to An, LEAB to Bn	1, 2	1.6 2.1	4.1 4.6	5.6 6.1	1.6 2.1	6.6 7.1	ns
t_{PZH} t_{PZL}	Output enable time OEBA to An, OEAB to Bn	4 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time OEBA to An, OEAB to Bn	4 5	2.5 1.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns
t_{PZH} t_{PZL}	Output enable time EBA to An, EAB to Bn	4 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time EBA to An, EAB to Bn	4 5	2.5 1.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns

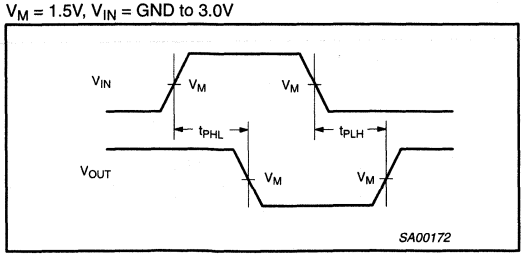
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

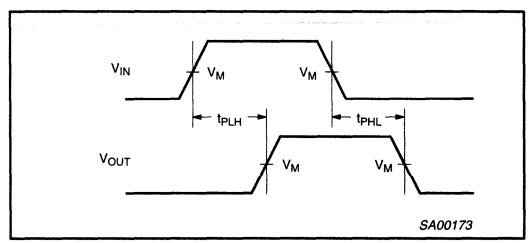
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time An to LEAB, Bn to LEBA	3	3.0 3.0	1.5 0.6	3.0 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time An to LEAB, Bn to LEBA	3	0.5 0.5	–0.3 –1.3	0.5 0.5	ns
$t_s(H)$ $t_s(L)$	Setup time An to EAB, Bn to EBA	3	3.0 3.0	1.5 0.6	3.0 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time An to EAB, Bn to EBA	3	0.5 0.5	–0.2 –1.3	0.5 0.5	ns
$t_w(L)$	Latch enable pulse width, Low	3	3.5	1.8	3.5	ns

AC WAVEFORMS

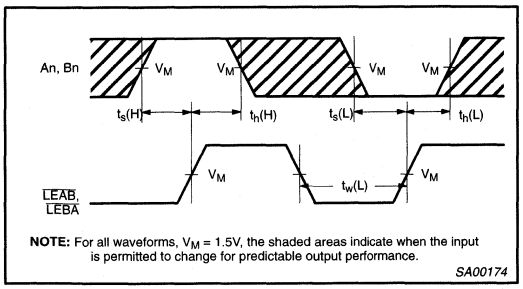
V_M = 1.5V, V_{IN} = GND to 3.0V



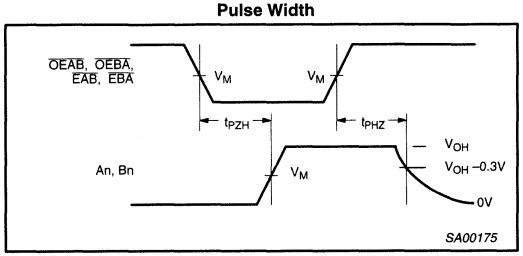
Waveform 1. Propagation Delay For Inverting Output



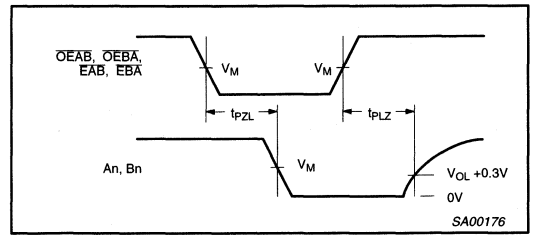
Waveform 2. Propagation Delay For Non–Inverting Output



Waveform 3. Data Setup and Hold Times And Latch Enable Pulse Width

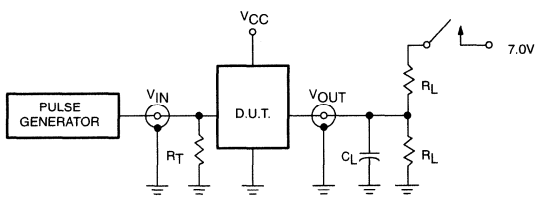


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

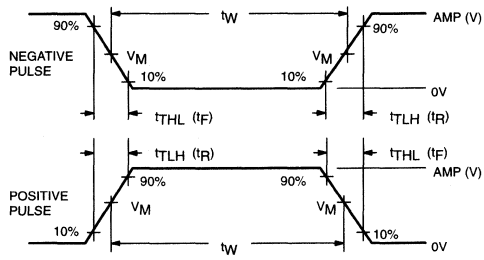


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal D-type transparent latch (3-State) 74ABT573A

FEATURES

- 74ABT573A is flow-through pinout version of 74ABT373
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State output buffers
- Common output enable
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT573A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT573A device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 74ABT573A is functionally identical to the 74ABT373 but has a flow-through pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

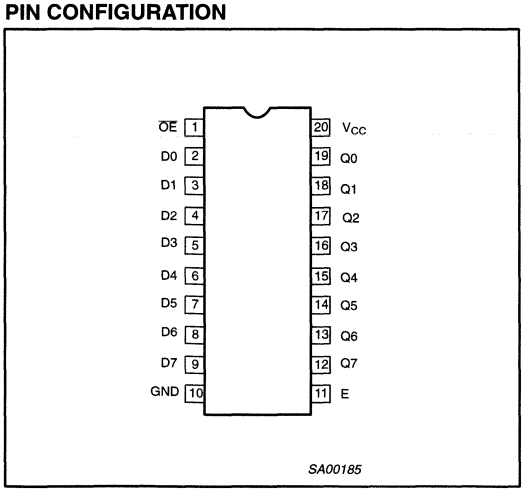
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	2.8 3.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	6	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT573A N	74ABT573A N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT573A D	74ABT573A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT573A DB	74ABT573A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT573A PW	7ABT573APW DH	SOT360-1

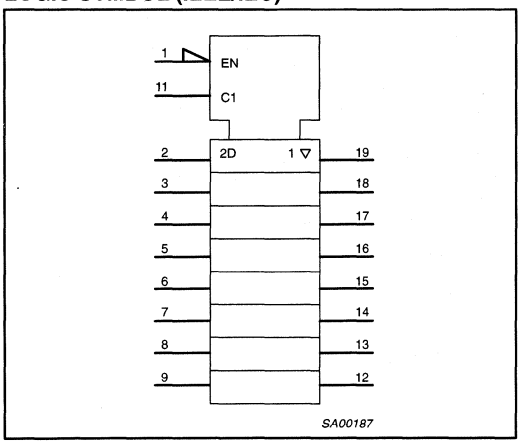
PIN CONFIGURATION



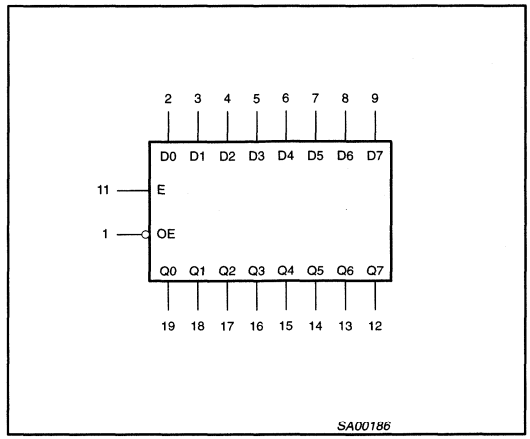
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL

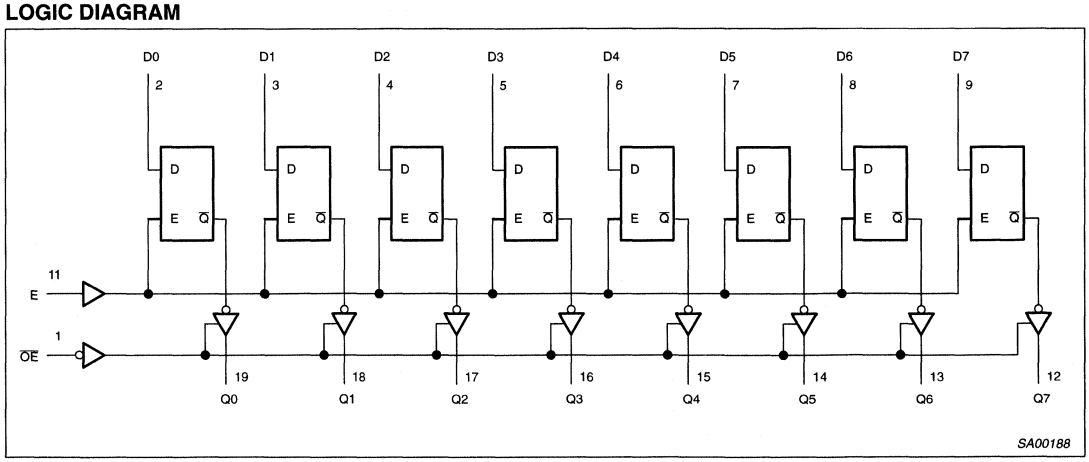


FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn	REGISTER	Q0 – Q7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]	V_{CC} = 2.0V; V_O = 0.5V; $\overline{V_{OE}}$ = Don't Care; V_I = GND or V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–40		–180	–40	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		100	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		100	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	2	1.5 2.2	2.8 3.3	4.0 4.8	1.5 2.2	4.5 5.3	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	1	1.2 1.8	2.5 3.0	4.0 4.4	1.2 1.8	4.5 4.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.2 2.7	3.0 3.8	4.5 5.3	1.2 2.7	5.2 5.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.5 1.2	2.8 2.2	4.1 3.4	1.5 1.2	4.5 3.8	ns

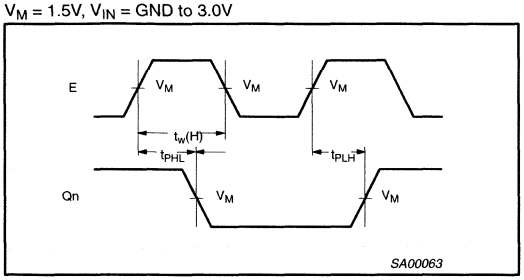
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

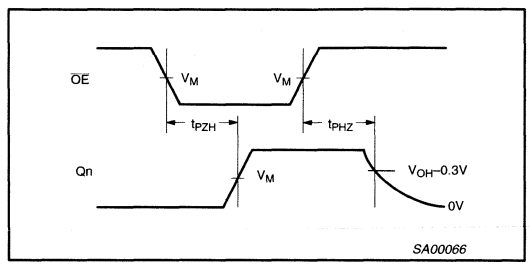
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to E	3	1.0 1.0	0.3 0.2	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to E	3	1.0 1.0	–0.1 –0.2	1.0 1.0	ns
$t_w(H)$	E pulse width High	1	2.0	0.7	2.0	ns

AC WAVEFORMS

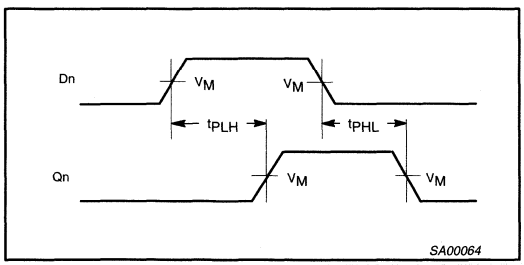
V_M = 1.5V, V_{IN} = GND to 3.0V



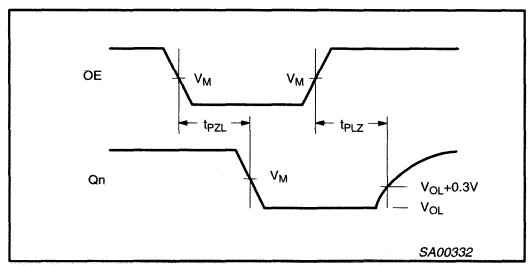
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



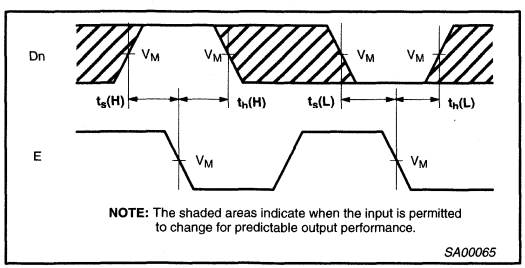
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Propagation Delay for Data to Outputs

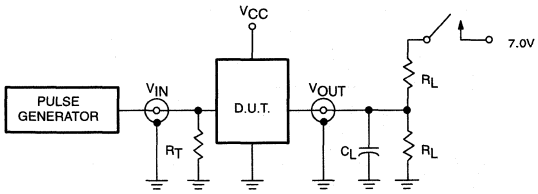


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

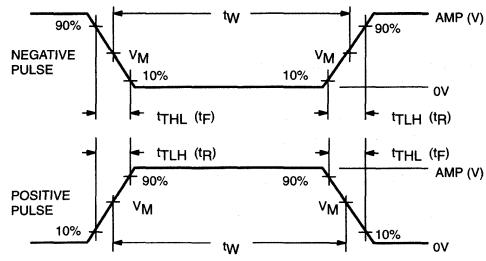


Waveform 3. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal D-type flip-flop (3-State) 74ABT574A

FEATURES

- 74ABT574A is flow-through pinout version of 74ABT374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Power-up 3-State
- Power-up reset
- Common output enable
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Live insertion/extraction permitted.

DESCRIPTION

The 74ABT574A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT574A is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The state of each D input (one set-up time before the Low-to-High clock transition) is transferred to the corresponding flip-flop's Q output.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "off" state, which means they will neither drive nor load the bus.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

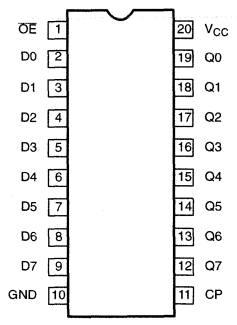
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	3.0 3.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	6	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	100	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT574A N	74ABT574A N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT574A D	74ABT574A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT574A DB	74ABT574A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT574A PW	7ABT574APW DH	SOT360-1

PIN CONFIGURATION



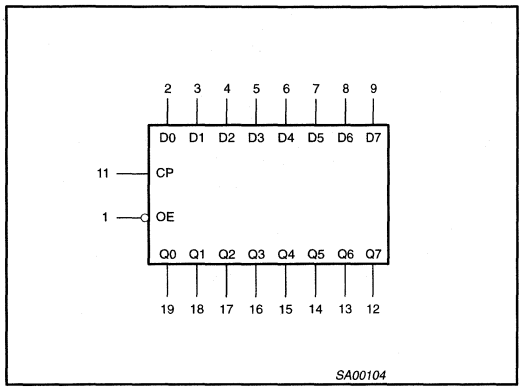
SA00103

PIN DESCRIPTION

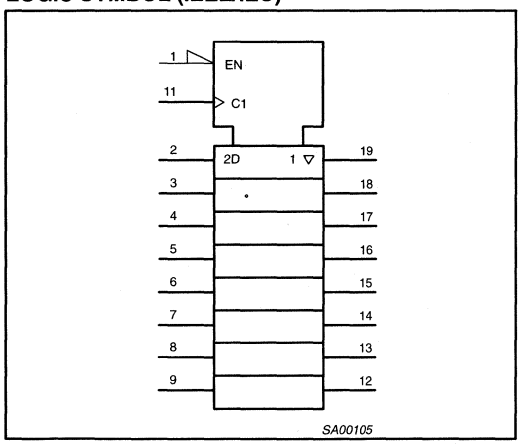
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal D-type flip-flop (3-State) 74ABT574A

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

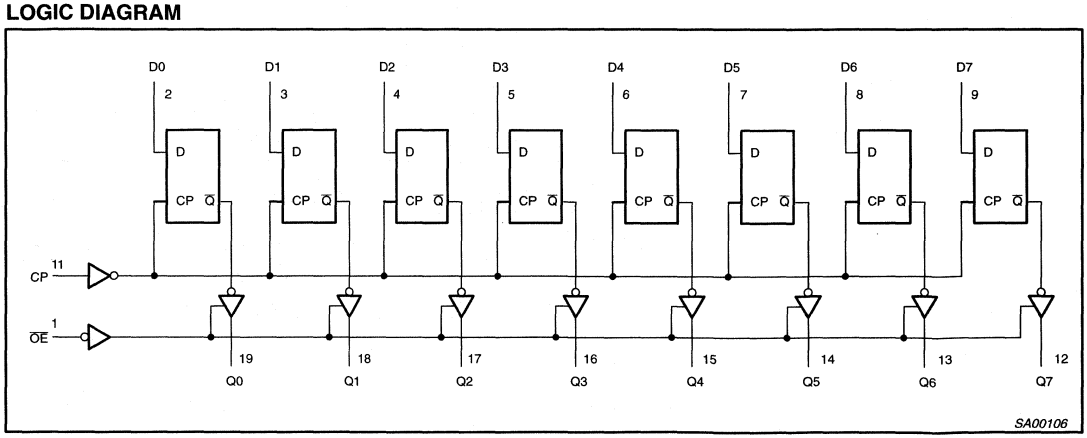


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn		Q0 – Q7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low–to–High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low–to–High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–40		–180	–40	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		100	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		100	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10 msec. From V_{CC} = 2.1V to V_{CC} = 5V ±10% a transition time of up to 100 µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Min	Min	Max	
f_{MAX}	Maximum clock frequency	1	150	400		150		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.5 2.0	3.0 3.4	4.4 4.7	1.5 2.0	5.0 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.0 2.5	2.9 3.8	4.1 5.2	1.0 2.5	5.0 5.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.8 1.4	3.1 2.6	4.3 3.8	1.8 1.4	5.0 4.0	ns

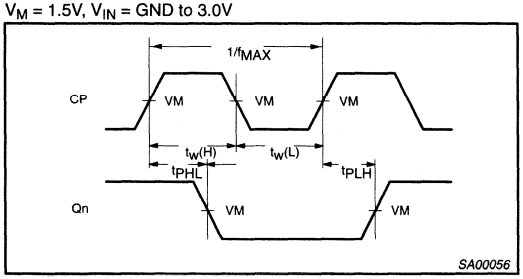
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

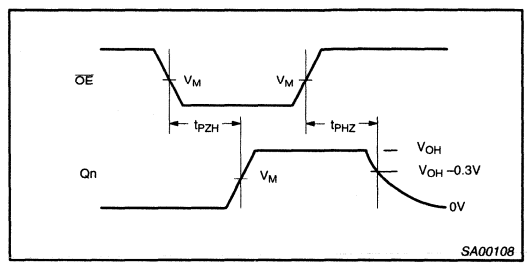
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	2	1.0 1.0	0.6 0.2	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	2	1.0 1.0	–0.7 –0.4	1.0 1.0	ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	1	2.0 2.0	0.7 0.8	2.0 2.0	ns

AC WAVEFORMS

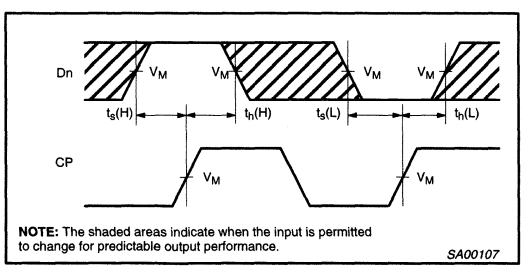
V_M = 1.5V, V_{IN} = GND to 3.0V



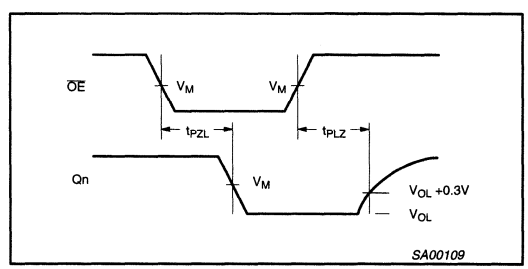
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

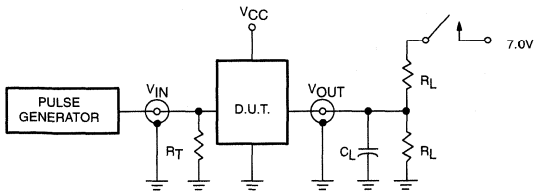


Waveform 2. Data Setup and Hold Times

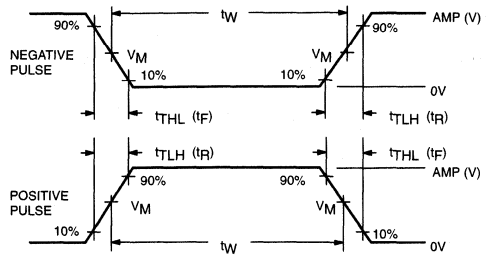


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal transceiver with dual enable, inverting (3-State)

74ABT620

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Power-up 3-State
- Live insertion/extraction permitted
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT620 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT620 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The 74ABT620 is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

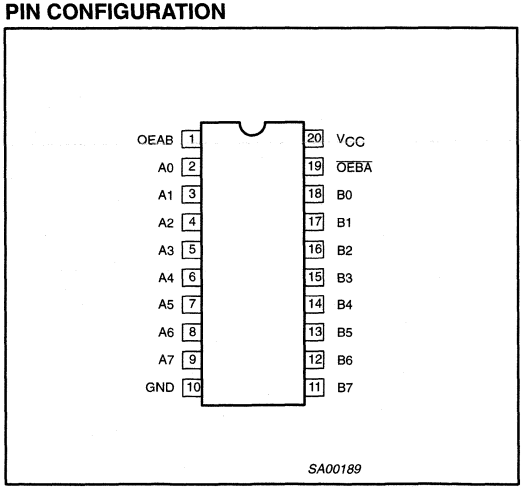
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance OEAB, $\overline{OEBA}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT620 N	74ABT620 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT620 D	74ABT620 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT620 DB	74ABT620 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT620 PW	74ABT620PW DH	SOT360-1

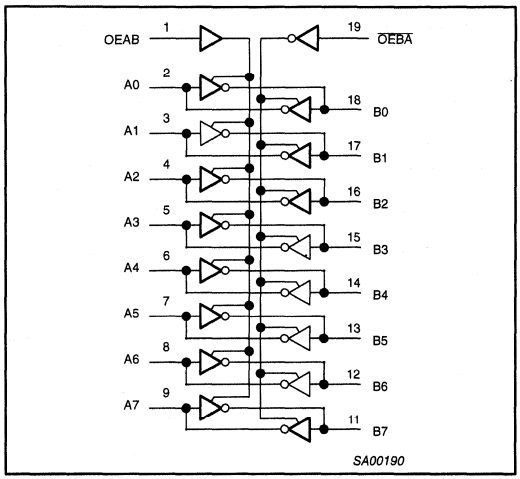
PIN CONFIGURATION



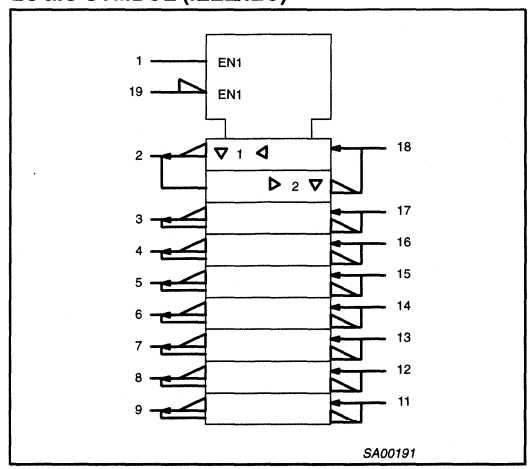
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Output enable input, A side to B side (active-High)
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Output enable input, B side to A side (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS
$\overline{OEBA}$	OEAB	An Bn
L	L	$\overline{B}$n Inputs
H	H	Inputs $\overline{A}$n
H	L	Z Z
L	H	$\overline{B}$n Inputs or Inputs $\overline{A}$n

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} and $V_{\overline{OE}}$ = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.05	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

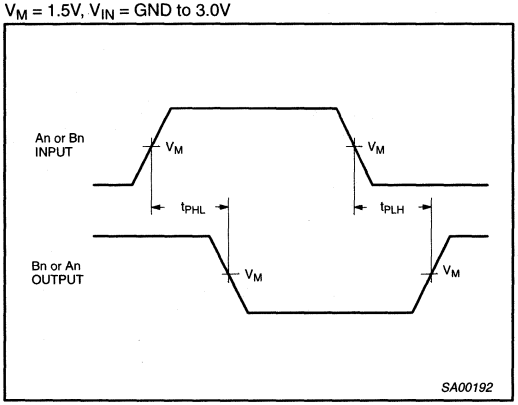
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

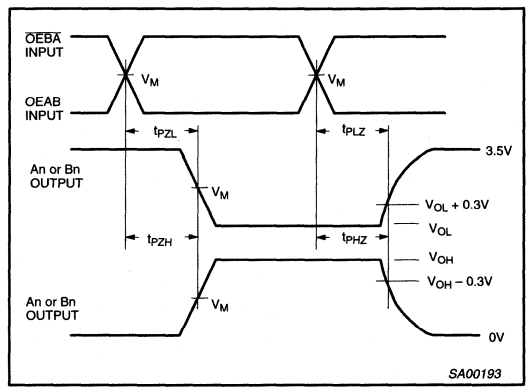
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.9 3.1	4.1 4.3	1.0 1.0	4.8 4.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	2	1.3 1.0	3.2 2.7	4.6 6.1	1.3 1.0	5.5 7.1	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	2	2.0 1.4	5.0 4.0	6.3 5.4	2.0 1.4	7.0 5.8	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	2	1.6 2.0	4.6 4.2	6.2 5.9	1.6 2.0	6.8 6.4	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	2	1.2 1.1	3.9 2.9	5.6 4.7	1.2 1.1	6.5 5.6	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

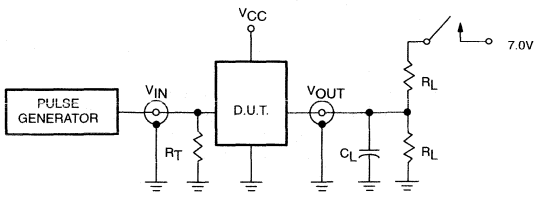


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

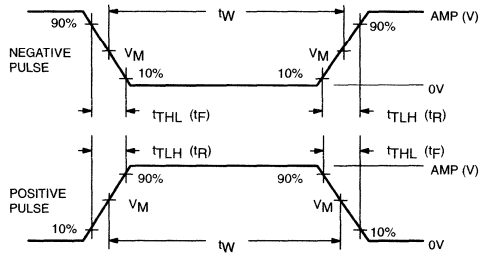


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal transceiver with dual enable, non-inverting (3-State)

74ABT623

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Power-up 3-State
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT623 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT623 device is an octal transceiver featuring non–inverting 3-State bus compatible outputs in both send and receive directions. The 74ABT623 is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

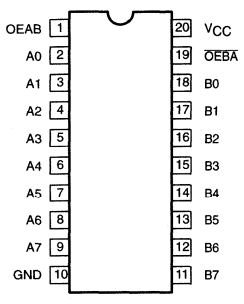
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.6 2.7	ns
C_{IN}	Input capacitance OEAB, $\overline{OEBA}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT623 N	74ABT623 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT623 D	74ABT623 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT623 DB	74ABT623 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT623 PW	74ABT623PW DH	SOT360-1

PIN CONFIGURATION

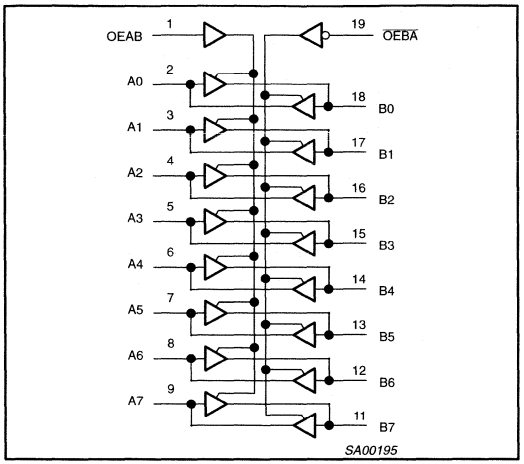


SA00189

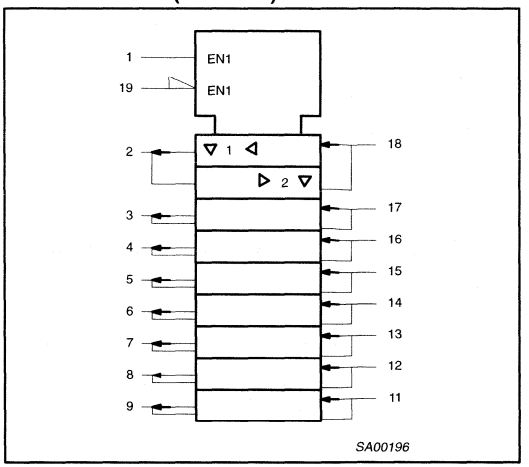
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Output enable input, A side to B side (active-High)
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Output enable input, B side to A side (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OEBA}$	OEAB	An	Bn
L	L	An = Bn	Inputs
H	H	Inputs	Bn = An
H	L	Z	Z
L	H	An = Bn	Bn = An

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5.0	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]		V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}; V_{OE} = GND		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

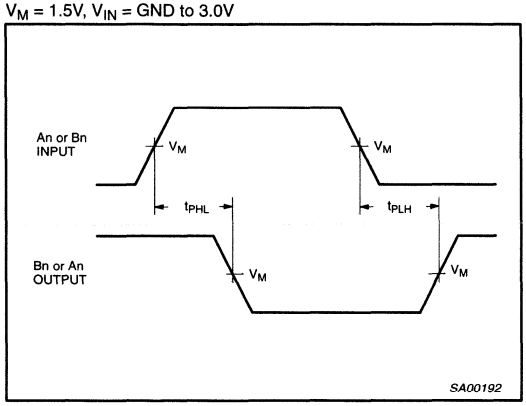
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

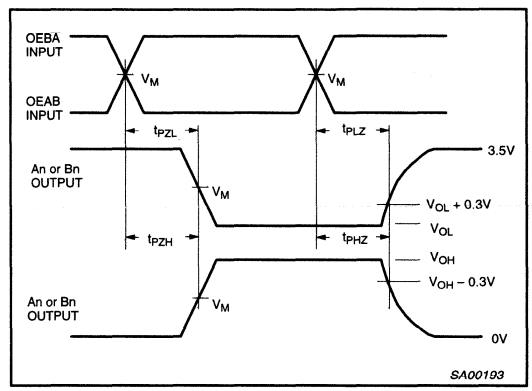
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.6 2.7	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.7 1.7	3.4 4.8	6.5 6.5	1.7 1.7	7.5 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time to High and Low level	2	1.7 1.7	3.6 3.1	6.5 6.5	1.7 1.7	7.5 7.5	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

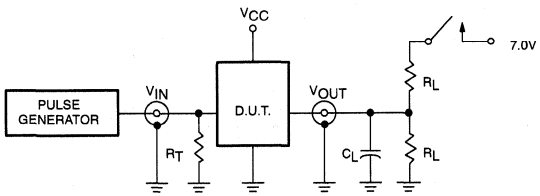


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

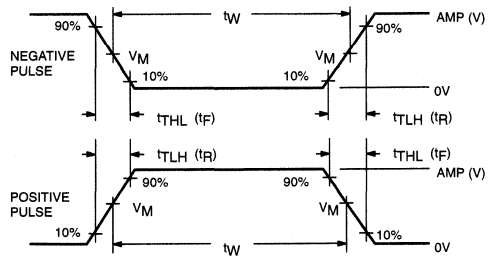


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal transceiver with direction pin, inverting (3-State)

74ABT640

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Power-up 3-State
- Live insertion/extraction permitted
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT640 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT640 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

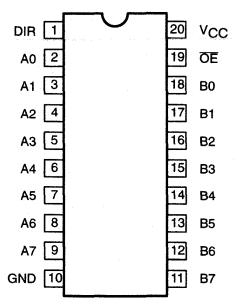
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.1	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT640 N	74ABT640 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT640 D	74ABT640 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT640 DB	74ABT640 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT640 PW	74ABT640PW DH	SOT360-1

PIN CONFIGURATION

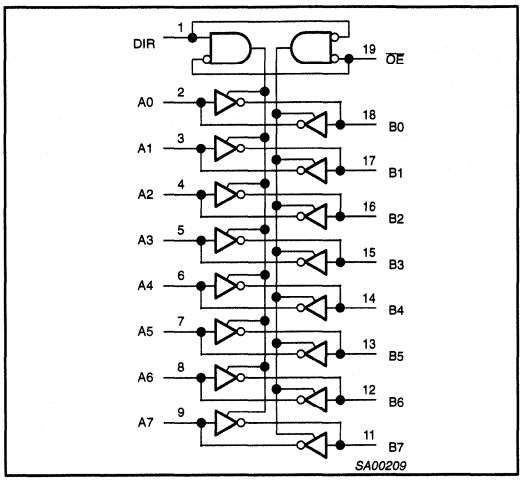


SA00208

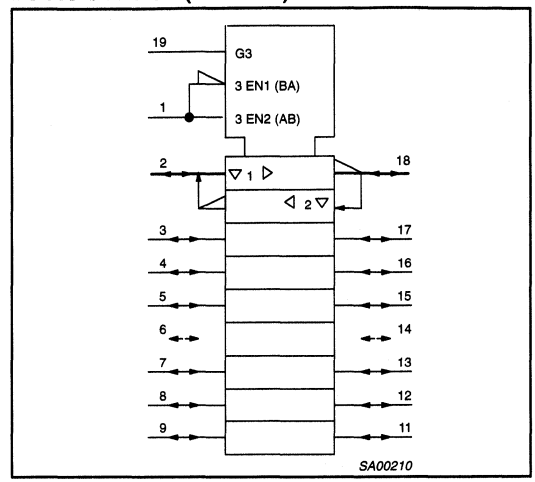
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input, B side to A side (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	$\overline{B}n$	Inputs
L	H	Inputs	$\overline{A}n$
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.05	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ±10% a transition time of up to 100µsec is permitted.

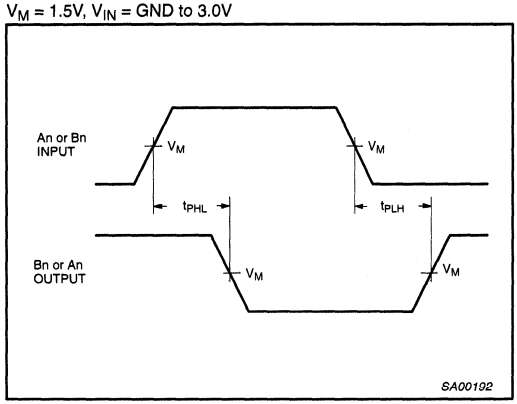
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

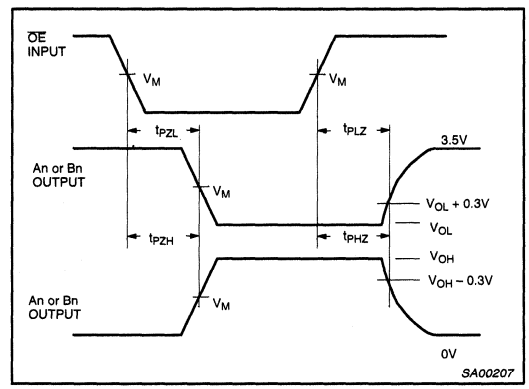
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.5	2.8 3.1	4.2 4.3	1.0 1.5	4.9 4.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.3	3.6 3.2	4.9 5.9	1.5 1.3	5.8 7.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	2.5 2.0	5.2 4.1	6.5 5.3	2.5 2.0	6.8 5.5	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

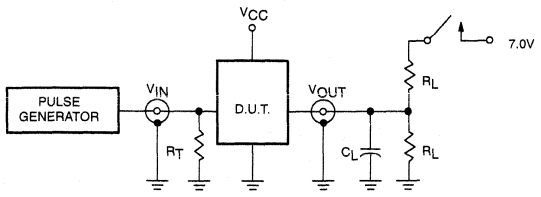


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

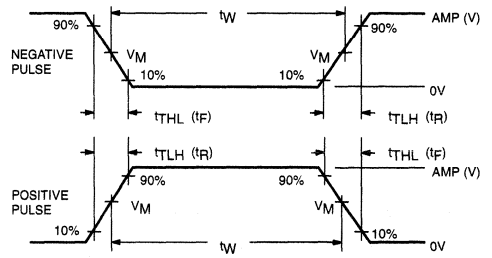


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal bus transceiver/register (3-State) 74ABT646A

FEATURES

- Combines 74ABT245 and 74ABT374 type functions in one device
- Independent registers for A and B buses
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiplexed real-time and stored data
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT646A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT646A transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (Low). In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74ABT646A.

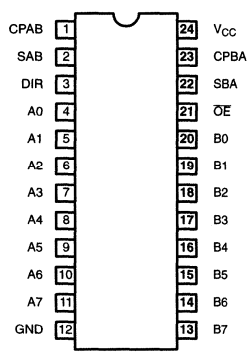
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.2 3.7	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT646A N	74ABT646A N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT646A D	74ABT646A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT646A DB	74ABT646A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT646A PW	7ABT646APW DH	SOT355-1

PIN CONFIGURATION

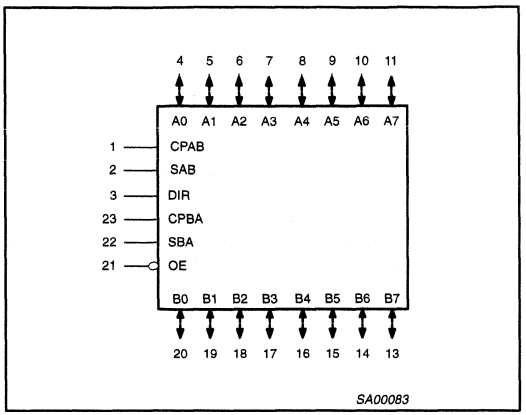


SA00082

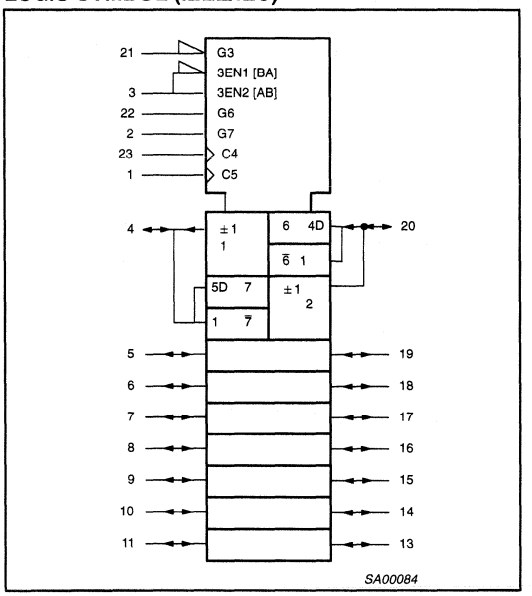
PIN DESCRIPTION

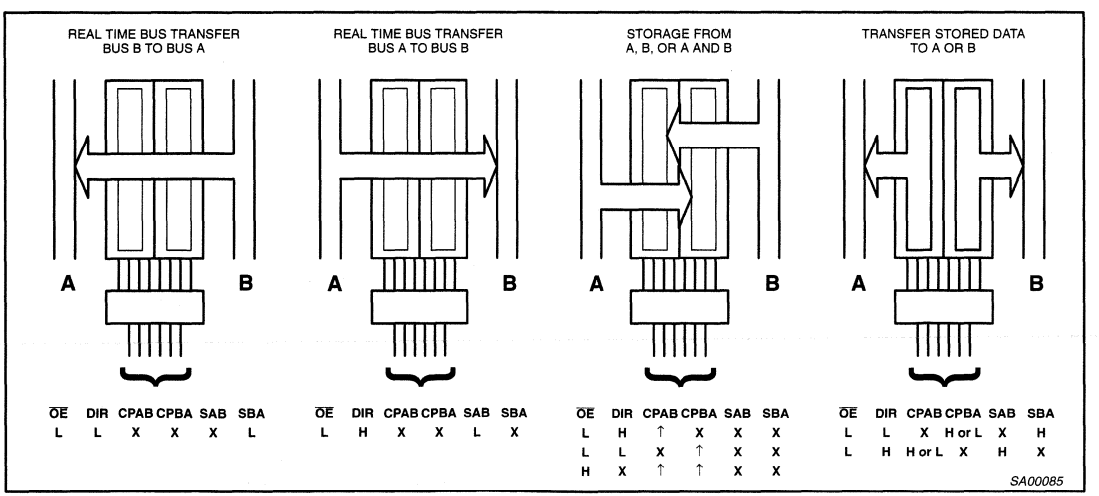
PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



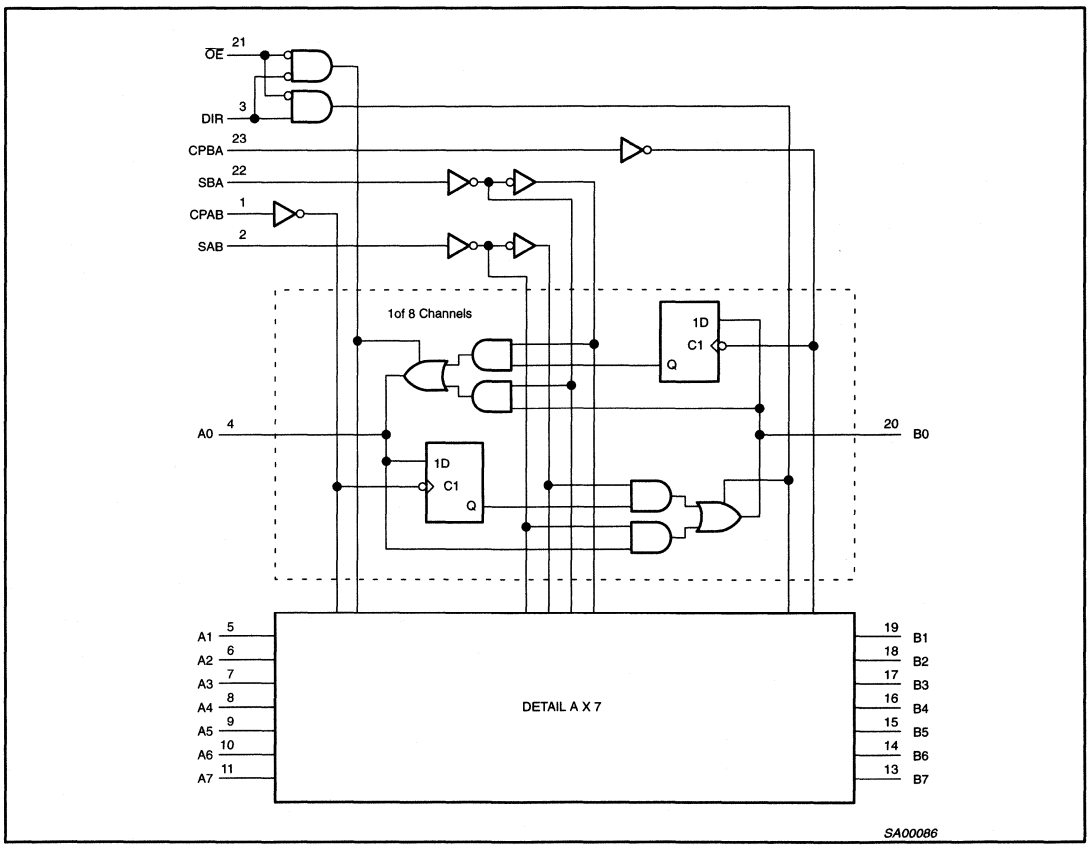


FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.0		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.5		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low–level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.3	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3–State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3–State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1, 5]		V_{CC} = 5.5V; V_O = 2.5V	–40	–65	–180	–40	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.6	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.
5. This data sheet limit may vary among suppliers.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	350		125		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.2 1.7	3.9 4.4	5.1 5.2[1]	2.2 1.7	5.6 5.6	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.5 1.5	3.2 3.7	4.3 4.6	1.5 1.5	4.8 5.4	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	2 3	1.5 1.5	3.8 4.4	5.1 5.3[1]	1.5 1.5	6.5 5.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	5 6	1.5 3.0	3.5 4.5	5.3 7.4	1.5 3.0	6.3 8.8	ns
t_{PHZ}[1] t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	5 6	1.5 1.5	4.0 3.3	4.8[1] 4.0	1.5 1.5	5.3[1] 4.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	5 6	1.5 2.5	3.9 4.7	5.7 9.0	1.2 2.5	6.7 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	5 6	1.5 1.5	4.0 3.5	5.0 4.7	1.5 1.5	5.7 6.0	ns

1. This data sheet limit may vary among suppliers.

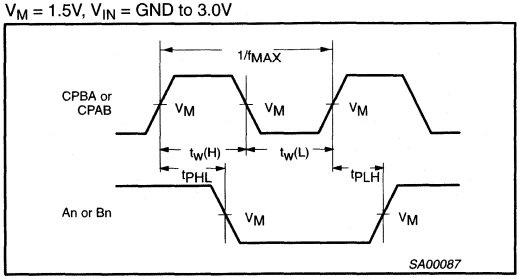
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

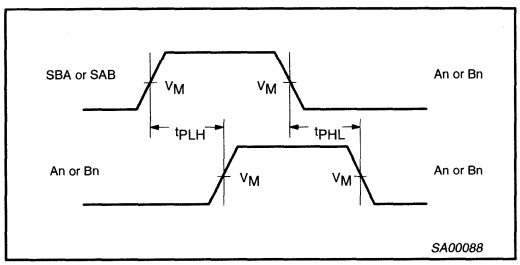
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
t_s(H) t_s(L)	Setup time An to CPAB, Bn to CPBA	4	3.0 3.0	0.7 0.7	3.0 3.0	ns
t_h(H) t_h(L)	Hold time An to CPAB, Bn to CPBA	4	0.0 0.0	–0.5 –0.5	0.0 0.0	ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	1	4.0 4.0	0.9 1.4	4.0 4.0	ns

AC WAVEFORMS

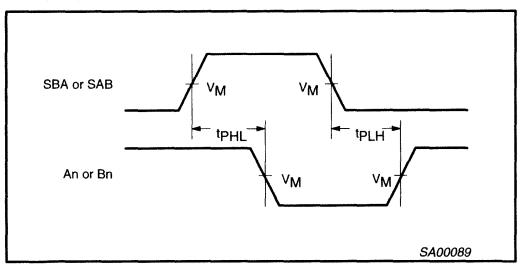
V_M = 1.5V, V_{IN} = GND to 3.0V



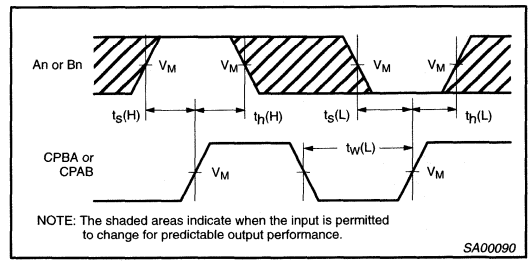
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



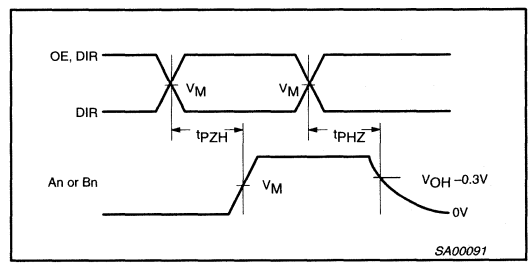
Waveform 2. Propagation Delay, SAB to Bn or SBA to An, An to Bn or Bn to An



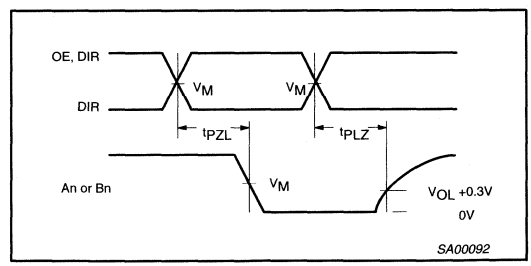
Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times

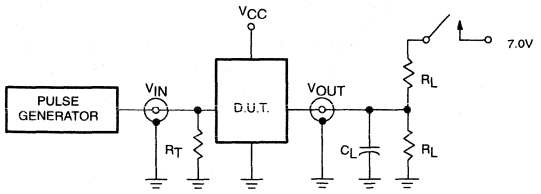


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

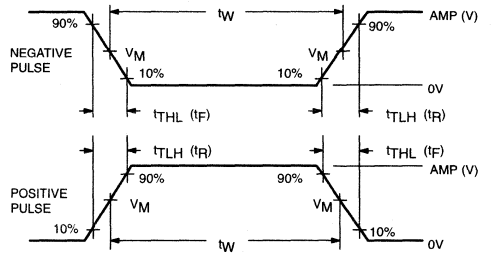


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal bus transceiver/register, inverting (3-State) 74ABT648

FEATURES

- Combines 74ABT245 and 74ABT374 type functions in one device
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: +64mA/–32mA
- Power-up 3-state
- Power-up reset
- Live insertion/extraction permitted
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT648 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT648 transceiver/register consists of bus transceiver circuits with inverting 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (Low). In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. Outputs from real-time, or stored registers will be inverted. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74ABT648.

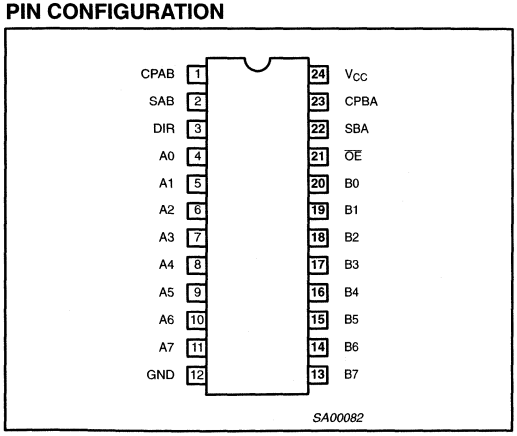
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	5.9	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT648 N	74ABT648 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT648 D	74ABT648 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT648 DB	74ABT648 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT648 PW	74ABT648PW DH	SOT360-1

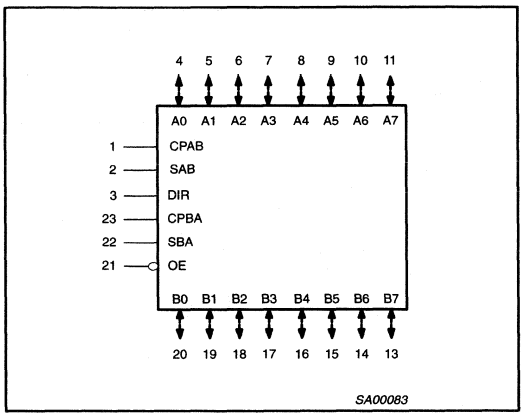
PIN CONFIGURATION



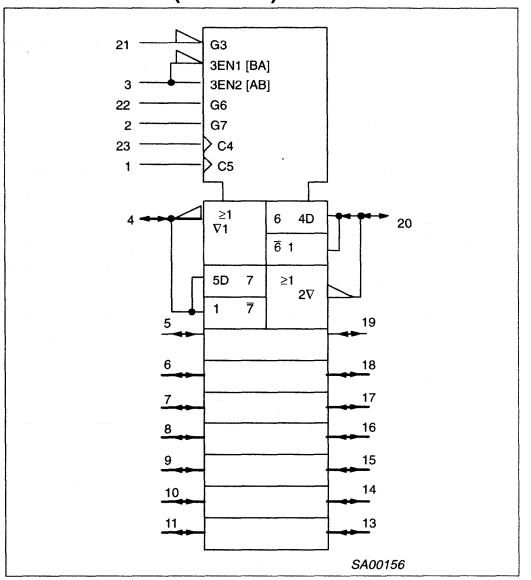
PIN DESCRIPTION

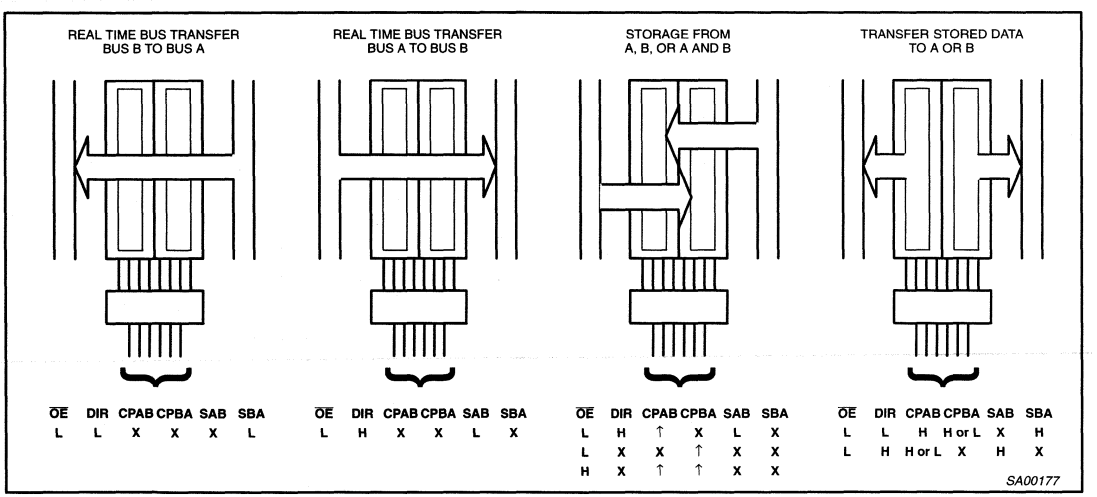
PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



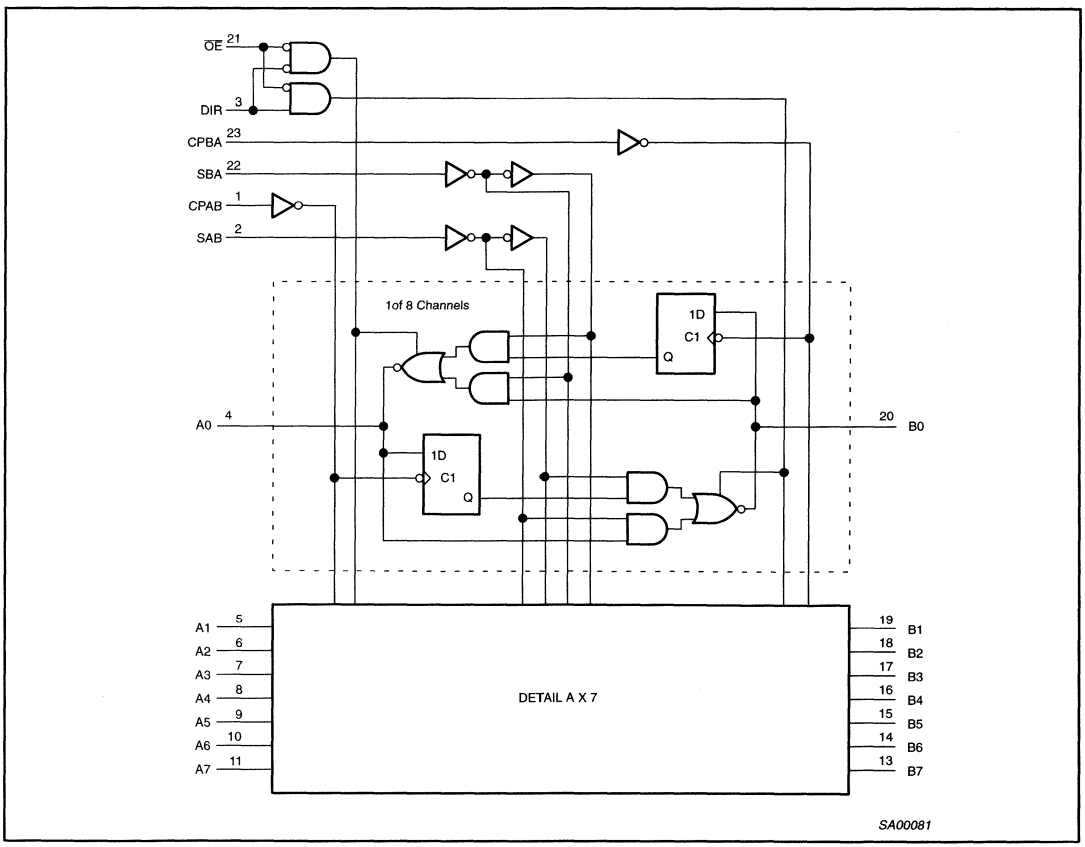


FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.2		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.7		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.3		2.0		V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power–up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = Don't care		±5.0	±50		±50	µA
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current		V_{CC} = 5.5V; V_O = 5.5 V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–65	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1 to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	200		125		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.2 1.7	5.3 5.9	6.8 7.4	2.2 1.7	7.8 8.4	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2 3	1.0 1.5	3.6 4.2	5.1 5.6	1.0 1.5	6.1 6.3	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	2 3	1.5 1.5	4.9 5.4	6.1 6.9	1.5 1.5	7.1 7.7	ns
t_{PZH} t_{PZL}	Output enable time OE to An or Bn	5 6	1.0 2.1	4.3 5.5	5.3 7.4	1.0 2.1	6.3 8.8	ns
t_{PHZ} t_{PLZ}	Output disable time OE to An or Bn	5 6	1.5 1.5	6.2 6.0	7.3 7.0	1.5 1.5	8.3 7.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	5 6	1.2 2.5	4.8 6.0	5.7 9.0	1.2 2.5	6.7 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	5 6	1.5 1.5	5.9 6.3	6.7 7.2	1.5 1.5	7.7 8.2	ns

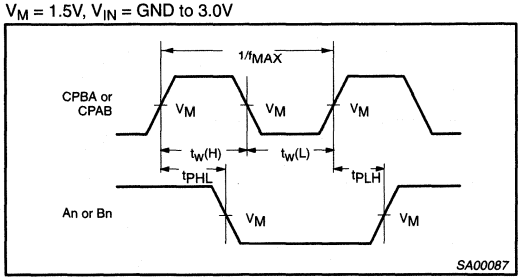
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

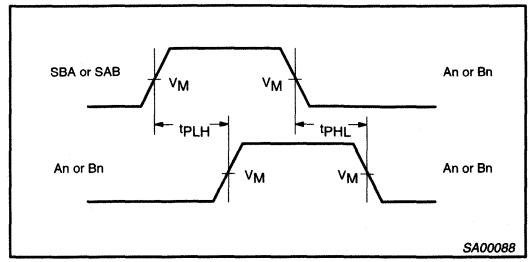
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time An to CPAB, Bn to CPBA	4	3.0 3.0	1.5 1.0	3.0 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time An to CPAB, Bn to CPBA	4	0.0 0.0	−0.4 −1.0	0.0 0.0	ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	1	3.5 4.0	2.6 1.0	3.5 4.0	ns

AC WAVEFORMS

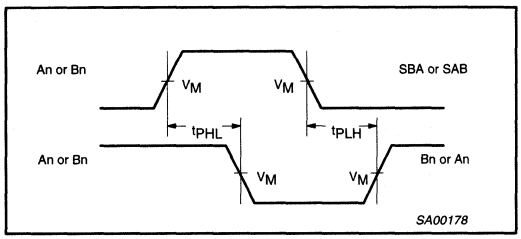
V_M = 1.5V, V_{IN} = GND to 3.0V



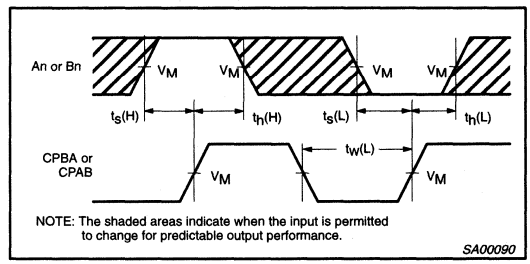
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



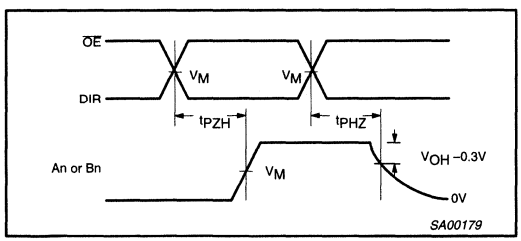
Waveform 2. Propagation Delay, SAB to Bn or SBA to An



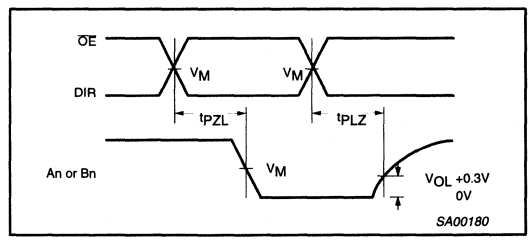
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times

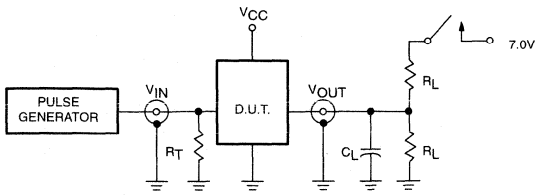


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

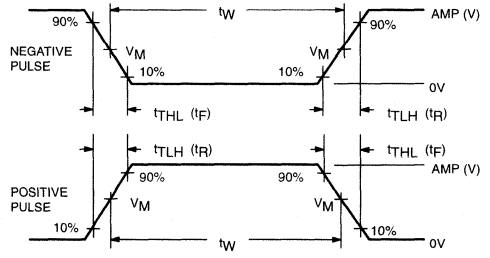


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal transceiver/register, inverting (3-State) 74ABT651

FEATURES

- Independent registers for A and B buses
- The 74ABT651 is the inverting version of the 74ABT652
- Multiplexed real-time and stored data
- 3-State outputs
- Live insertion/extraction permitted.
- Power-up 3-State
- Power-up reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT651 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT651 transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT651.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.

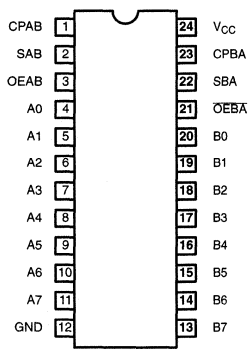
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50pF; V_{CC} = 5V	3.8 4.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT651 N	74ABT651 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT651 D	74ABT651 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT651 DB	74ABT651 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT651 PW	74ABT651PW DH	SOT355-1

PIN CONFIGURATION

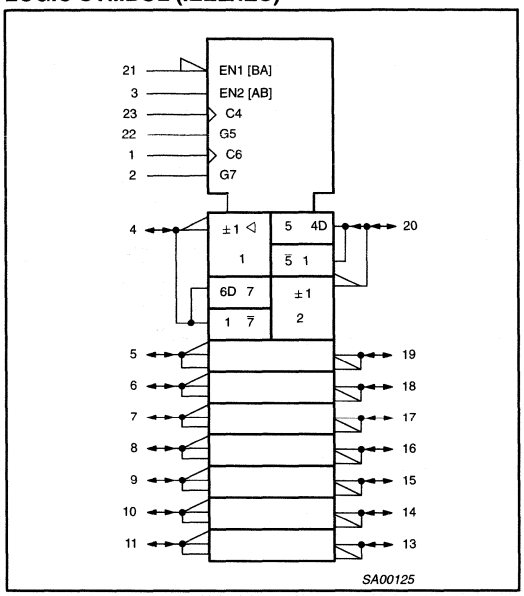


SA00094

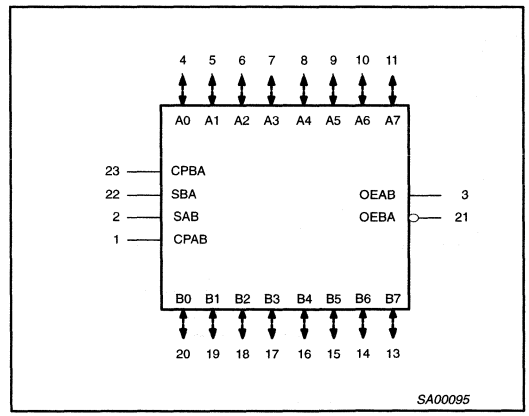
PIN DESCRIPTION

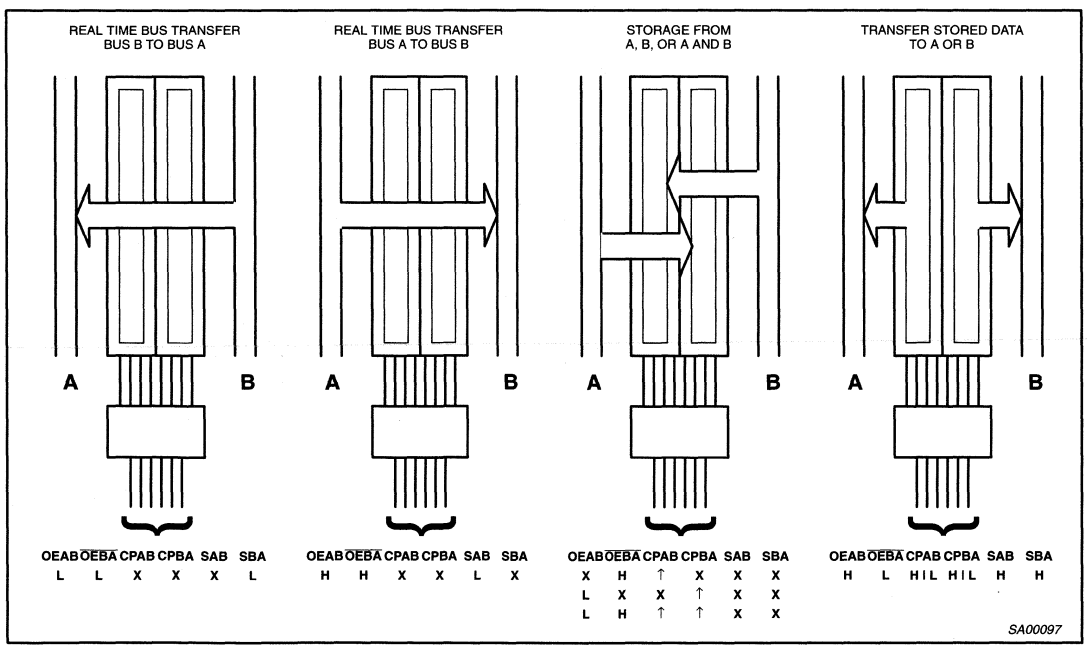
PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / OEBA	A to B Output Enable input / B to A Output Enable input (active–Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



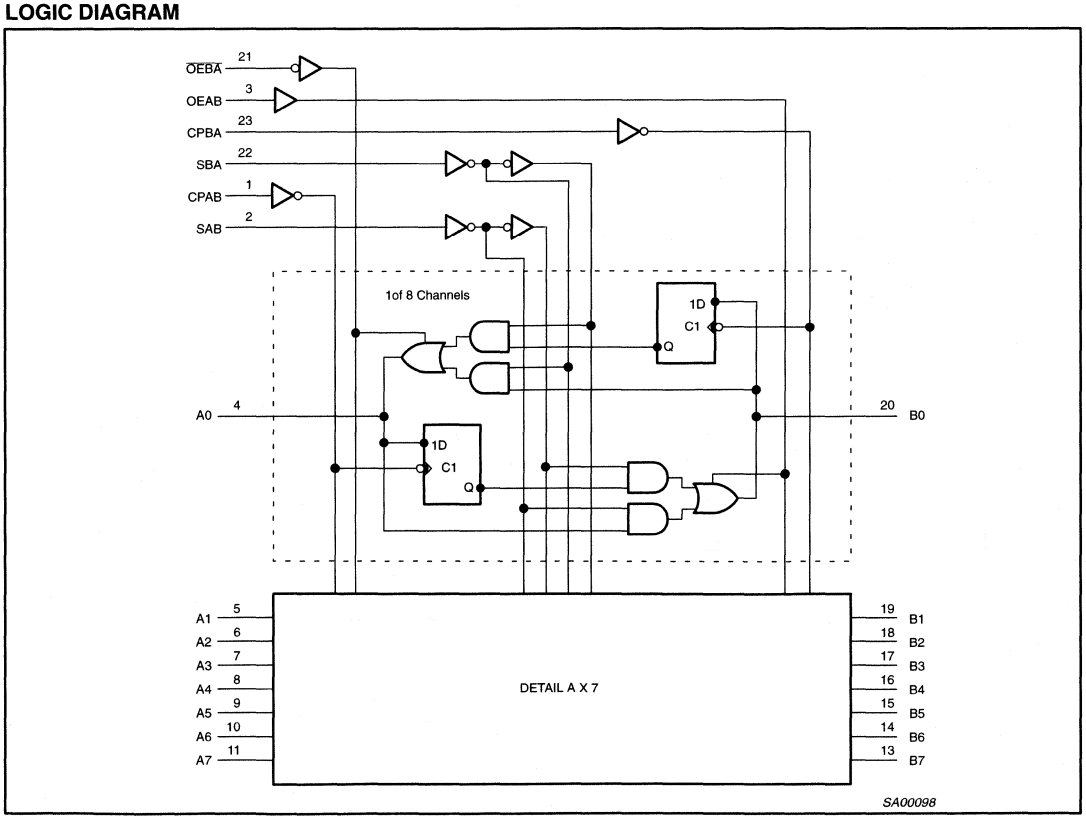


FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time $\overline{A}$ data to B bus Store $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. 1Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.2		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.7		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.30		2.0		V
V_{OL}	Low–level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}[3]	Power-up output low voltage		V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; $V_{\overline{OE}}$ = Don't Care; V_I = GND or V_{CC}		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3–State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3–State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–40	–65	–180	–40	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	300		125		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.2 1.7	3.8 4.4	5.1 5.1	2.2 1.7	5.6 5.6	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.5 1.5	3.2 3.7	5.1 4.6	1.5 1.5	6.2 5.4	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	3	1.5 1.5	3.8 4.4	5.1 4.9	1.5 1.5	6.5 5.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	5 6	1.3 2.5	3.7 4.7	4.6 6.8	1.3 2.5	5.8 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	5 6	1.5 1.5	4.0 3.2	4.5 3.8	1.5 1.5	5.0 4.1	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	5 6	1.8 2.9	3.4 4.5	6.1 6.5	1.8 2.9	6.5 7.4	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	5 6	1.5 1.5	3.8 3.1	4.5 4.4	1.5 1.5	5.5 5.1	ns

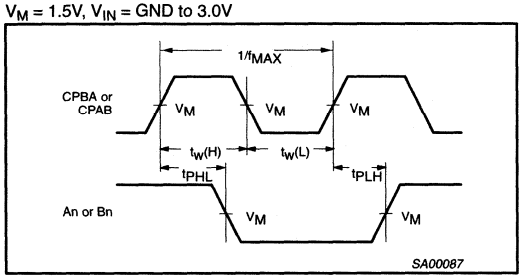
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

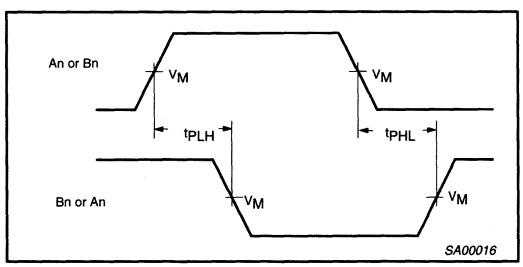
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time An to CPAB, Bn to CPBA	4	3.0 3.0	1.2 0.8	3.0 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time An to CPAB, Bn to CPBA	4	0.0 0.0	−0.8 −0.9	0.0 0.0	ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	1	4.0 4.0	1.2 1.1	4.0 4.0	ns

AC WAVEFORMS

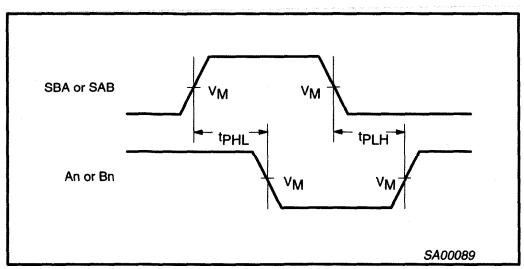
V_M = 1.5V, V_{IN} = GND to 3.0V



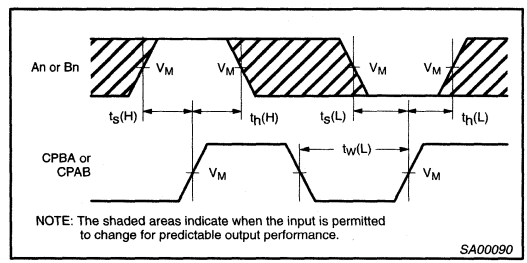
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



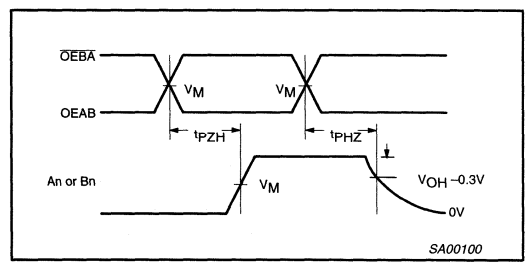
Waveform 2. Propagation Delay, An to Bn or Bn to An



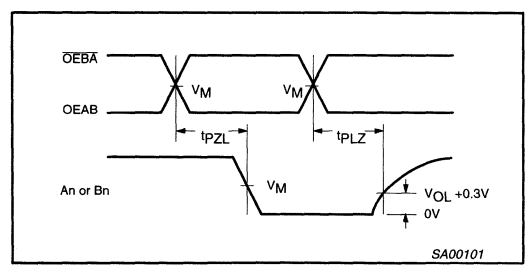
Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times

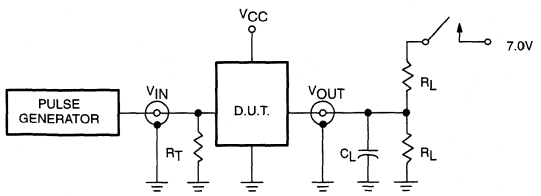


Waveform 5. 3–State Output Enable Time to High Level and Output Disable Time from High Level

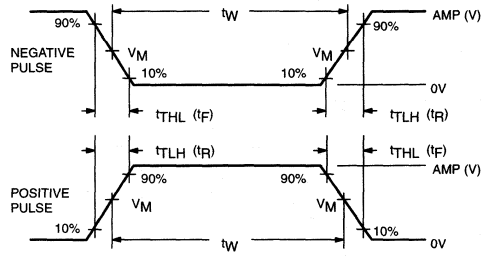


Waveform 6. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal transceiver/register, non-inverting (3-State) 74ABT652A

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT652A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT652A transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

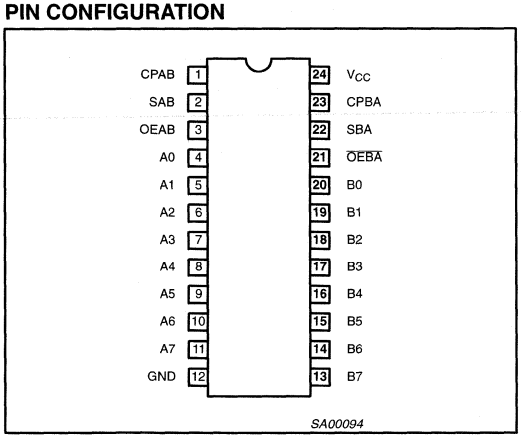
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50pF; V_{CC} = 5V	3.7 4.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT652A N	74ABT652A N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT652A D	74ABT652A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT652A DB	74ABT652A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT652A PW	7ABT652APW DH	SOT355-1

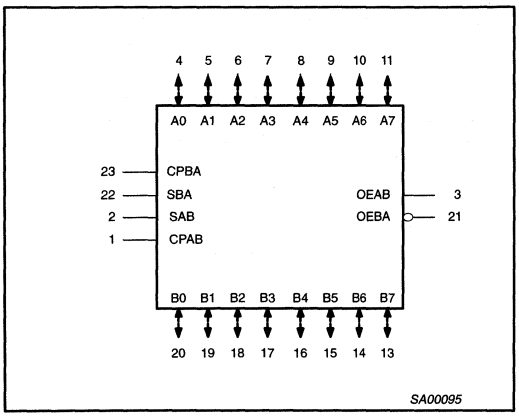
PIN CONFIGURATION



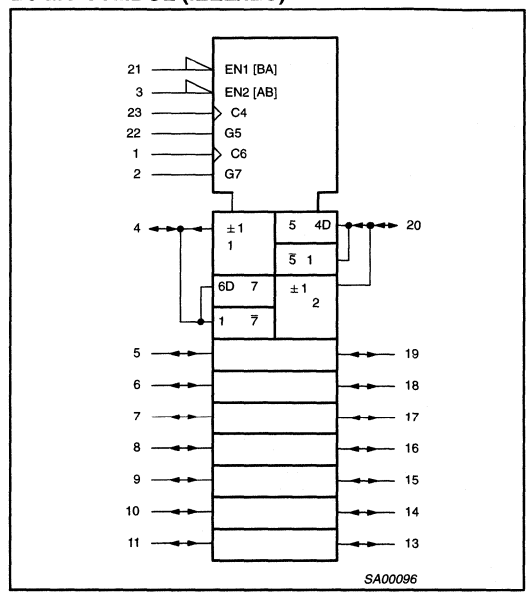
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / $\overline{OEBA}$	A to B Output Enable input / B to A Output Enable input (active–Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

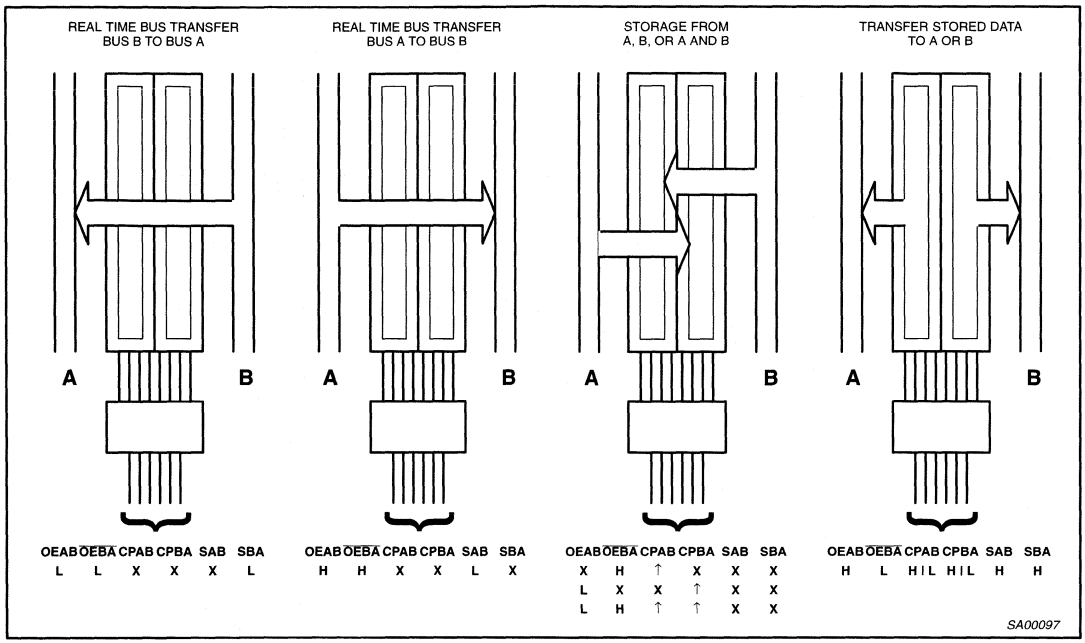
INPUTS						DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

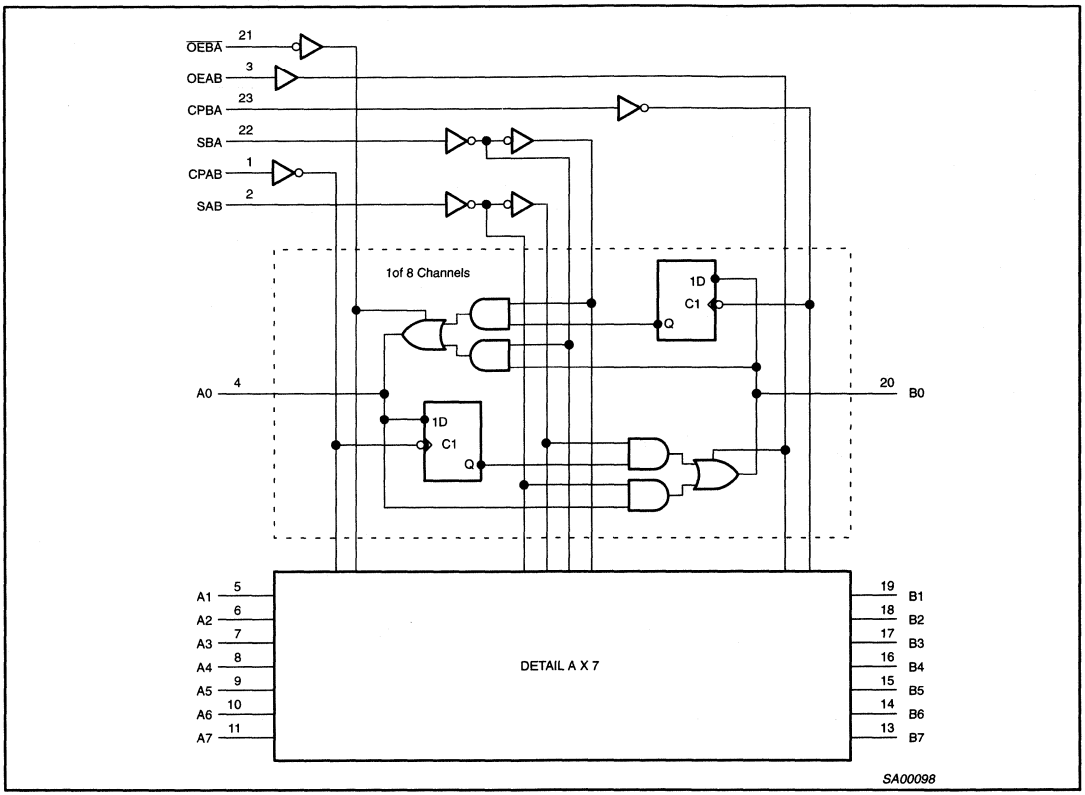
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT652A.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.0		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.5		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.3	0.55		0.55	V
V_{RST}[3]	Power-up output low voltage	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current — Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
	Input leakage current — Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care; $\overline{V_{OE}}$ = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1, 5]	V_{CC} = 5.5V; V_O = 2.5V	–40	–65	–180	–40	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.
5. This data sheet limit may vary among suppliers.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	300		125		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.2 1.7	3.7 4.3	5.1 5.1	2.2 1.7	5.6 5.6	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.5 1.5	3.0 3.6	4.3 4.6	1.5 1.5	4.8 5.4	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	3	1.5 1.5	3.5 4.2	5.1 5.2[1]	1.5 1.5	6.5 5.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	5 6	2 3	3.2 4.5	4.6 6.8	2 3	5.8 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	5 6	1.5 1.5	3.9 2.9	4.7[1] 3.8	1.5 1.5	5.3[1] 4.1	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	5 6	2 3	3.5 4.7	6.1 6.5	2 3	6.5 7.4	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	5 6	1.5 1.5	3.8 3.0	4.6[1] 4.4	1.5 1.5	5.5 5.1	ns

1. This data sheet limit may vary among suppliers.

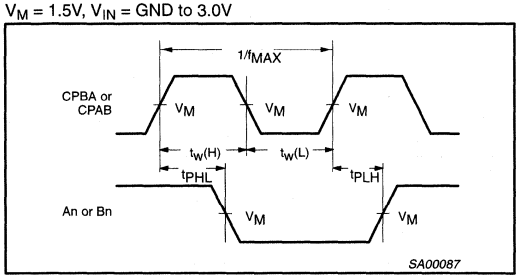
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

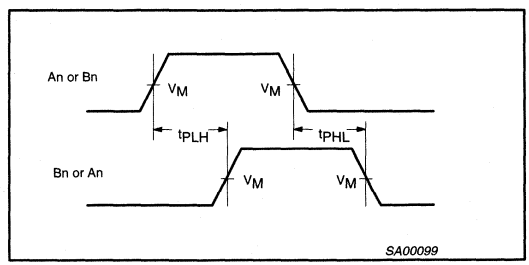
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Min	Max	
t_s(H) t_s(L)	Setup time An to CPAB, Bn to CPBA	4	3.0 3.0	0.7 0.7	3.0 3.0		ns
t_h(H) t_h(L)	Hold time An to CPAB, Bn to CPBA	4	0.0 0.0	–0.5 –0.5	0.0 0.0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	1	4.0 4.0	1.0 1.0	4.0 4.0		ns

AC WAVEFORMS

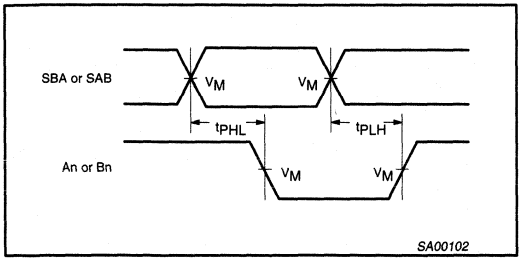
V_M = 1.5V, V_{IN} = GND to 3.0V



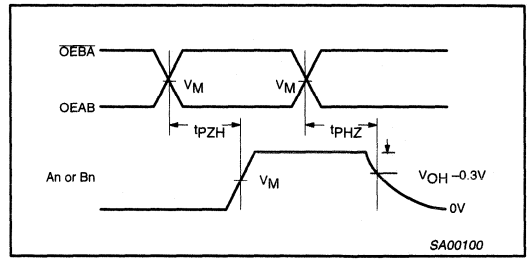
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



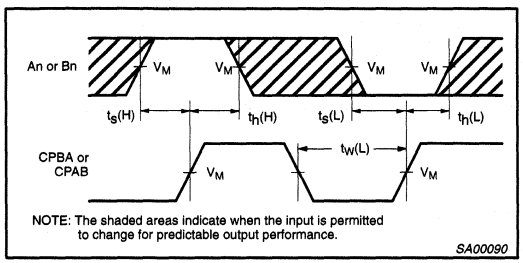
Waveform 2. Propagation Delay, An to Bn or Bn to An



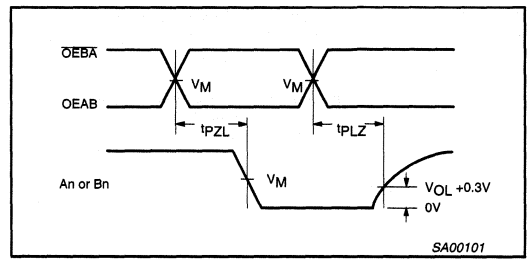
Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

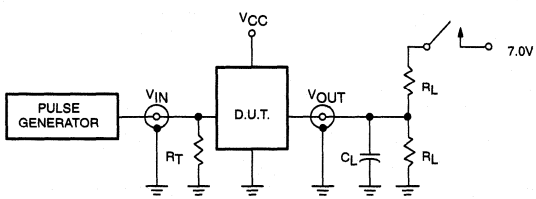


Waveform 4. Data Setup and Hold Times

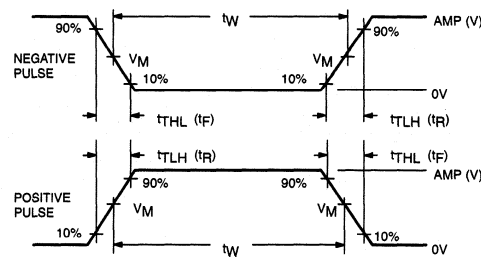


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal transceiver with parity generator/checker (3-State)

74ABT657

FEATURES

- Combinational functions in one package
- Low static and dynamic power dissipation with high speed and high output drive
- Output capability: +64mA/–32mA
- Power-up 3-State
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT657 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT657 is an octal transceiver featuring non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 64mA. The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

The Output Enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B ($T/\overline{R}$ = High) and an input when receiving from port B to A port ($T/\overline{R}$ = Low). When transmitting ($T/\overline{R}$ = High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode ($T/\overline{R}$ = Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERROR}$ will be High, signifying no error.

(2) even and the parity (PARITY) input is High, then $\overline{ERROR}$ will be asserted Low, indicating an error.

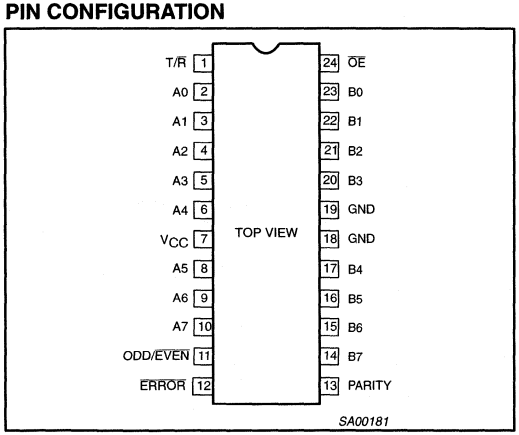
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT657 N	74ABT657 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT657 D	74ABT657 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT657 DB	74ABT657 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT657 PW	74ABT657PW DH	SOT355-1

PIN CONFIGURATION



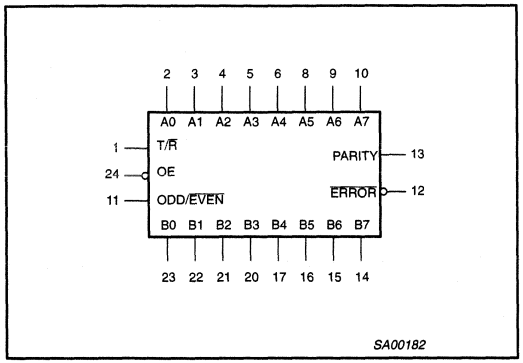
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
13	PARITY	Parity output
11	ODD/$\overline{EVEN}$	Parity select input
12	$\overline{ERROR}$	Error output
1	$T/\overline{R}$	Transmit/receive input
2, 3, 4, 5, 6, 8, 9, 10	A0 - A7	A port 3-State outputs
23, 22, 21, 20, 17, 16, 15, 14	B0 - B7	B port 3-State outputs
24	$\overline{OE}$	Output enable input (active-Low)
18, 19	GND	Ground (0V)
7	V_{CC}	Positive supply voltage

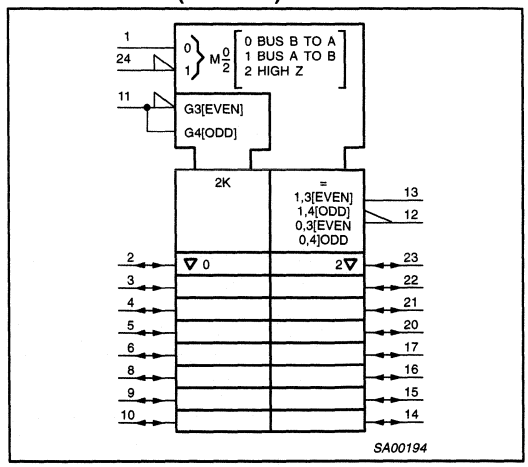
Octal transceiver with parity generator/checker (3-State)

74ABT657

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

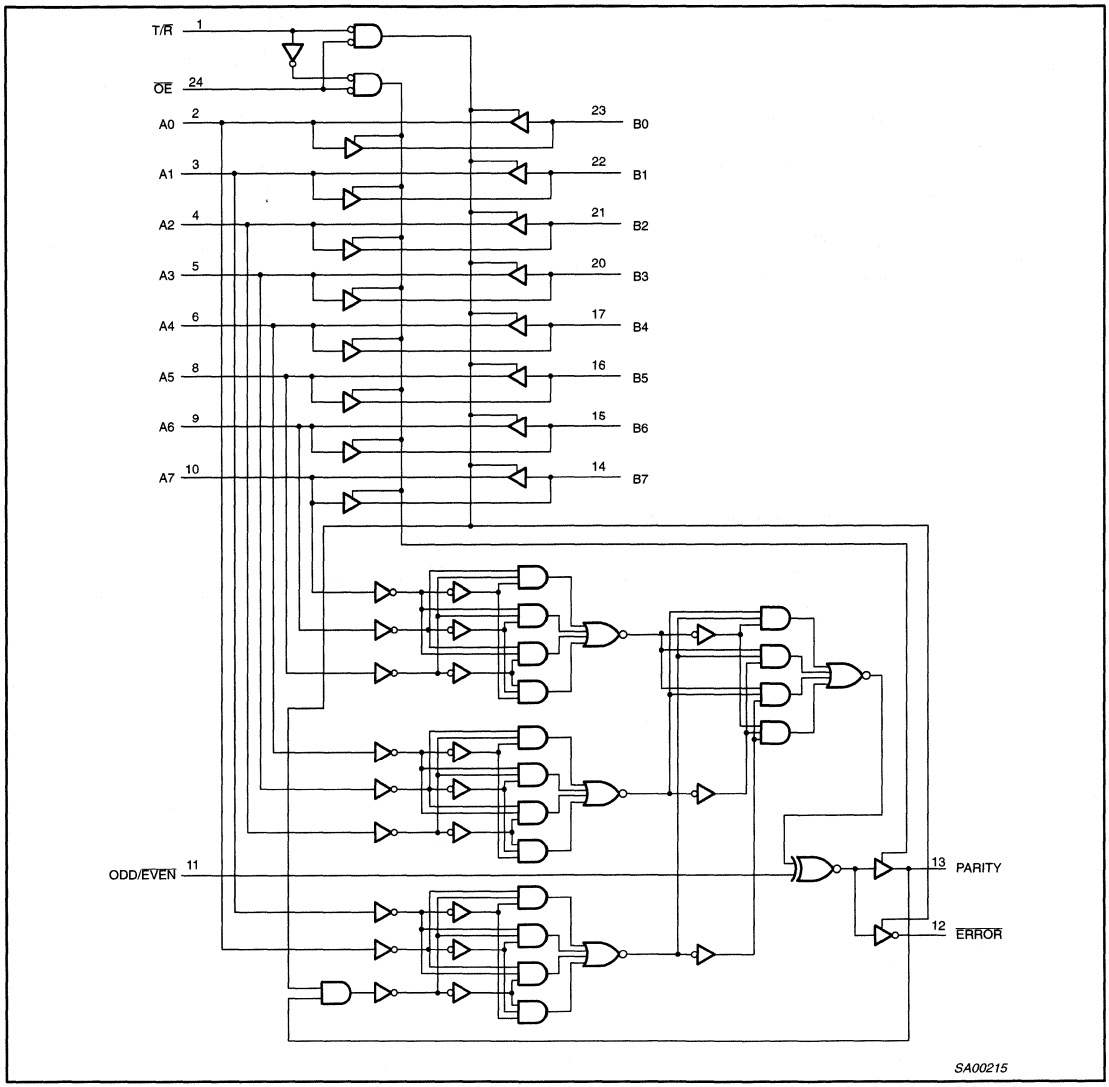


FUNCTION TABLE

NUMBER OF HIGH INPUTS	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	3-State

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU}I_{PD}$	Power-up/down 3-State output current[3]		V_{CC} 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}		±5.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

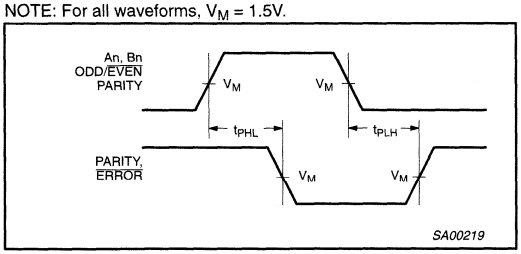
SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.1 1.2	3.3 3.0	5.0 4.3	1.1 1.2	5.5 4.8	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	1, 2	2.5 2.8	6.5 7.0	8.7 9.1	2.5 2.8	10.1 10.6	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to PARITY, $\overline{ERROR}$	1, 2	1.7 1.9	5.0 5.0	6.6 6.6	1.7 1.9	7.3 7.3	ns
t_{PLH} t_{PHL}	Propagation delay Bn to $\overline{ERROR}$	1, 2	3.9 4.0	9.2 9.6	11.7 12.1	3.9 4.0	13.8 14.5	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{ERROR}$	1, 2	2.7 3.2	6.0 6.4	7.6 8.0	2.7 3.2	9.4 9.4	ns
t_{PZH} t_{PZL}	Output enable time[1] to High or Low level	3, 4	1.3 1.9	3.8 4.4	5.6 7.0	1.3 1.9	6.6 8.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	3, 4	2.4 2.7	5.1 5.4	7.0 7.6	2.4 2.7	7.6 8.1	ns

NOTES:

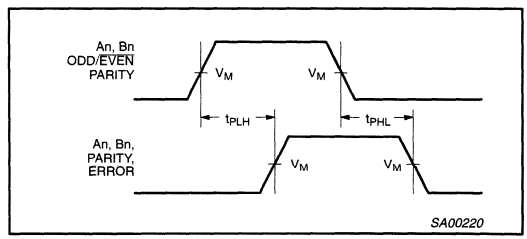
1. These delay times reflect the 3-State recovery time only and do not include the delay through the buffers and the parity check circuitry which affect the $\overline{ERROR}$ output. To assure *valid* information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output. *Valid* data at the $\overline{ERROR}$ pin ≥ (B to A) + (A to PARITY).

AC WAVEFORMS

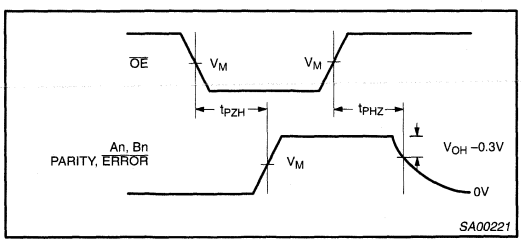
NOTE: For all waveforms, $V_M = 1.5V$.



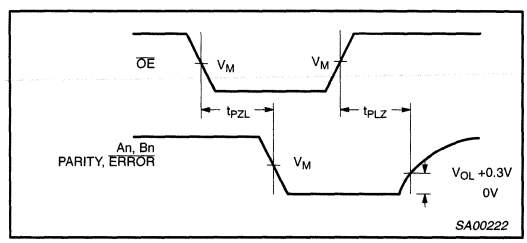
Waveform 1. Propagation Delay For Inverting Output



Waveform 2. Propagation Delay For Non-Inverting Output

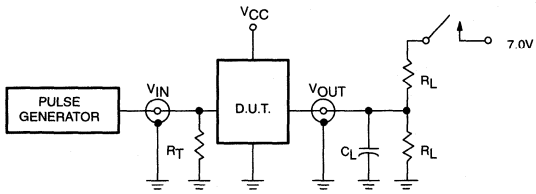


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

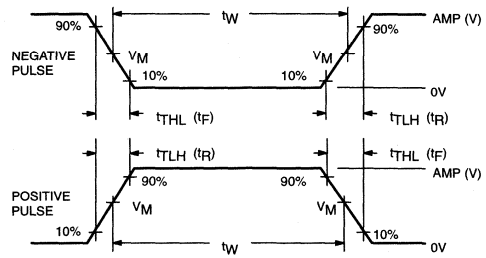


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

10-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT821

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up Reset

DESCRIPTION

The 74ABT821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT821 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT821 is a buffered 10-bit wide version of the 74ABT374/74ABT534 functions.

The 74ABT821 is a 10-bit, edge triggered register coupled to ten 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($\overline{OE}$) controls all ten 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

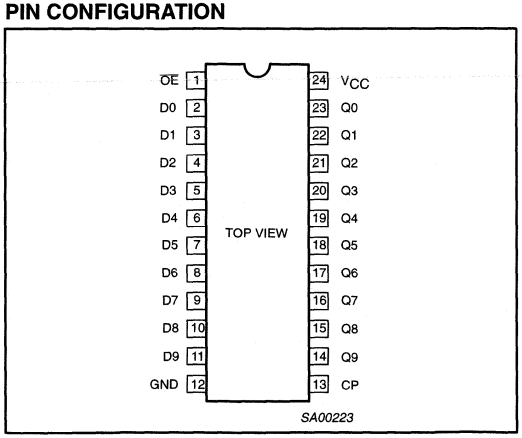
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	4.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT821 N	74ABT821 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT821 D	74ABT821 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT821 DB	74ABT821 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT821 PW	74ABT821PW DH	SOT355-1

PIN CONFIGURATION



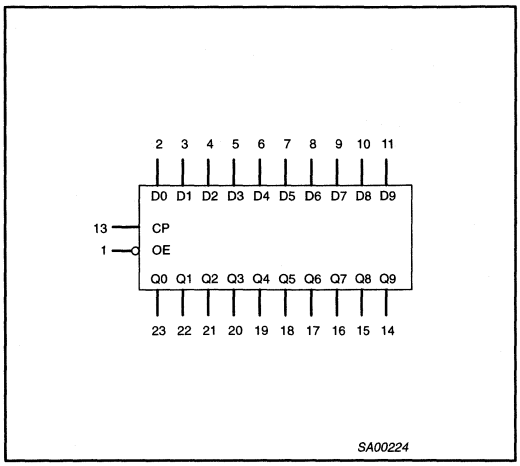
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D0-D9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q0-Q9	Data outputs
13	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

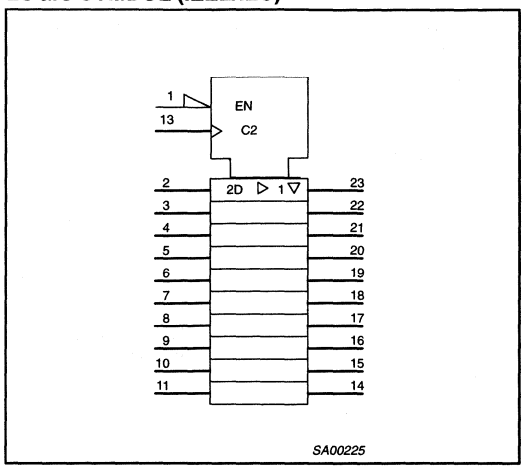
10-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT821

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



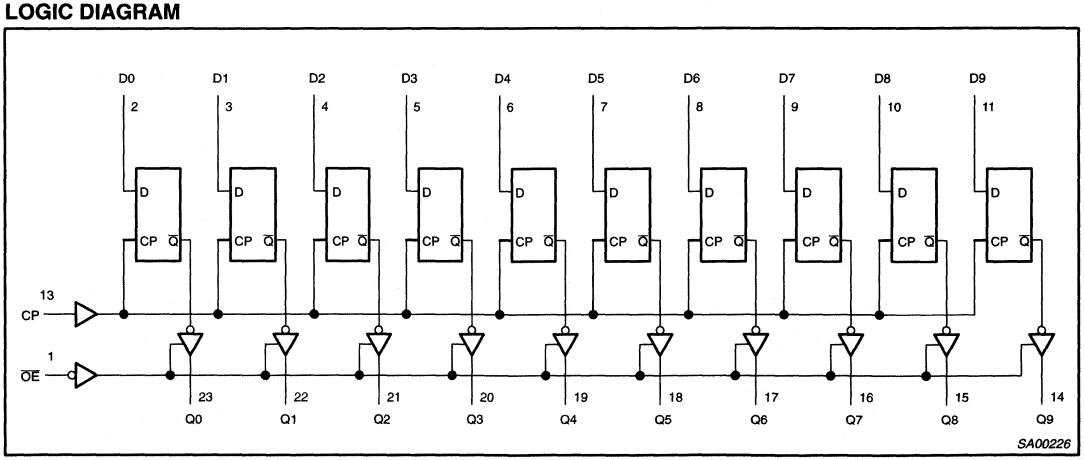
FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 – Q9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition

NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		25	38		38	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Typ	Max	
f_{MAX}	Maximum clock frequency	1	125	185		125		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	2.1 2.8	4.1 4.6	5.6 6.2	2.1 2.8	6.2 6.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.0 2.2	3.0 4.1	4.5 5.6	1.0 2.2	5.3 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	2.7 2.8	4.7 4.6	6.2 6.1	2.7 2.8	6.7 6.5	ns

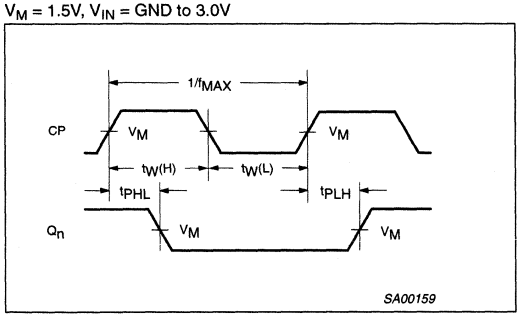
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

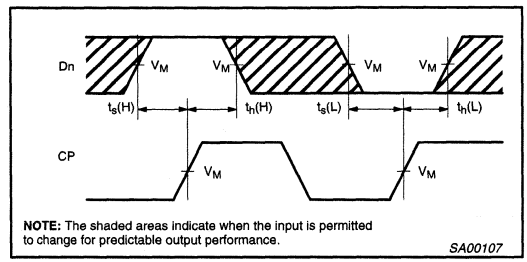
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	2	2.1 2.1	0.5 0.3	2.1 2.1	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	2	1.3 1.3	0.0 –0.3	1.3 1.3	ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	1	2.9 3.8	1.8 2.8	2.9 3.8	ns

AC WAVEFORMS

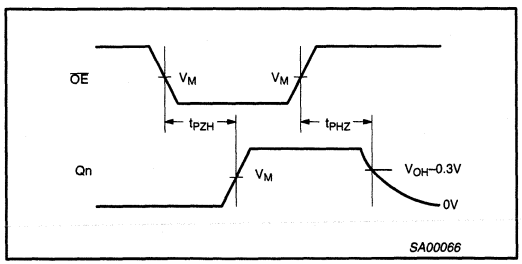
V_M = 1.5V, V_{IN} = GND to 3.0V



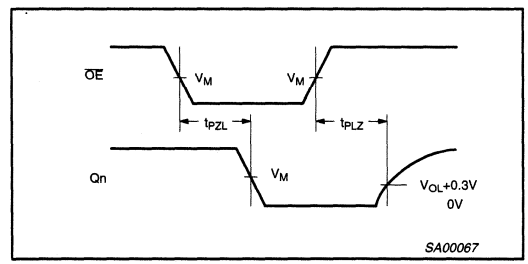
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

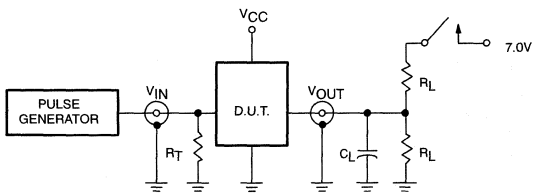


Waveform 3. 3–State Output Enable Time to High Level and Output Disable Time from High Level

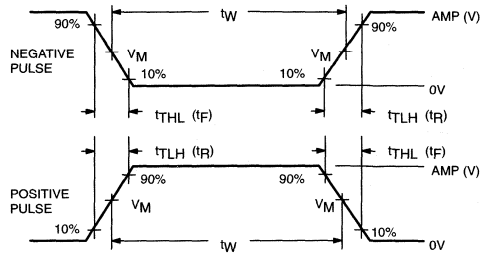


Waveform 4. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

9-bit D-type flip-flop with reset and enable (3-State)

74ABT823

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up Reset

DESCRIPTION

The 74ABT823 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT823 is a 9-bit wide buffered register with Clock Enable ($\overline{CE}$) and Master Reset ($\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The register is fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

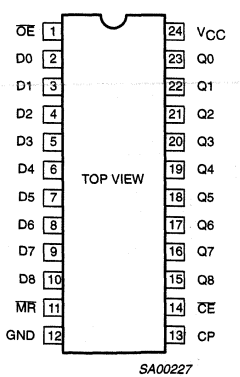
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	4.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT823 N	74ABT823 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT823 D	74ABT823 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT823 DB	74ABT823 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT823 PW	74ABT823PW DH	SOT355-1

PIN CONFIGURATION



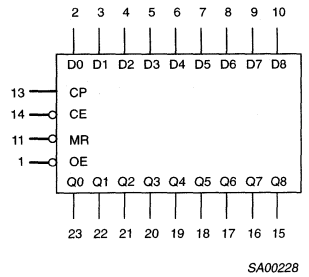
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0-D8	Data inputs
23, 22, 21, 20, 19,18, 17, 16, 15	Q0-Q8	Data outputs
13	CP	Clock pulse input (active rising edge)
14	$\overline{CE}$	Clock enable input (active-Low)
11	$\overline{MR}$	Master reset input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

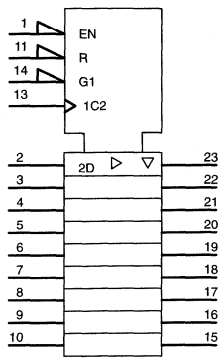
9-bit D-type flip-flop with reset and enable (3-State)

74ABT823

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

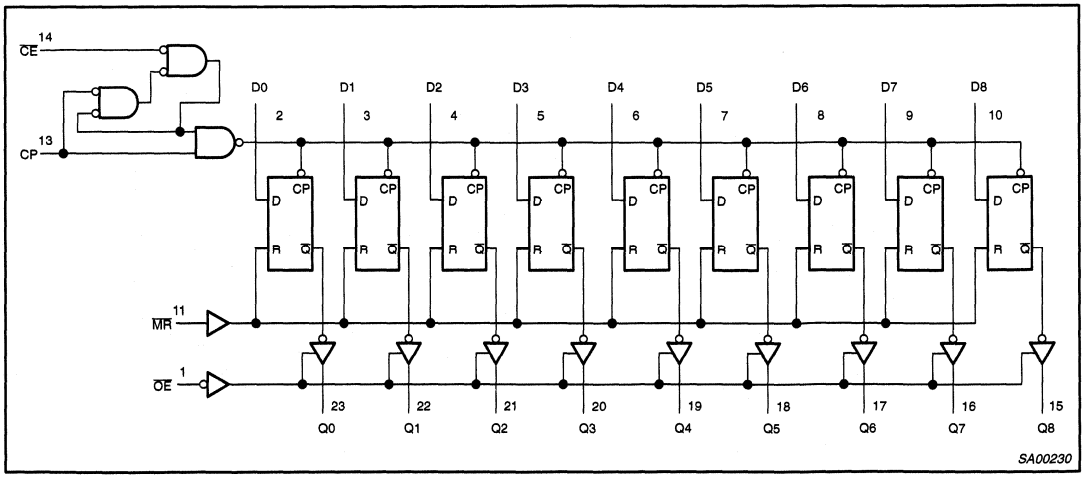


FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	Dn	Q0 – Q8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]	V_{CC} = 2.0V; V_O = 0.5V; $V_{\overline{OE}} = V_{CC}$; V_I = GND or V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		27	34		34	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	200		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	2.1 2.2	4.3 4.4	5.9 6.1	2.1 2.2	6.8 6.7	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2	2.0	4.1	6.3	2.0	7.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.0 2.2	3.0 4.1	4.5 5.6	1.0 2.2	5.3 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	2.7 2.8	4.8 5.0	6.2 6.4	2.7 2.8	6.9 6.9	ns

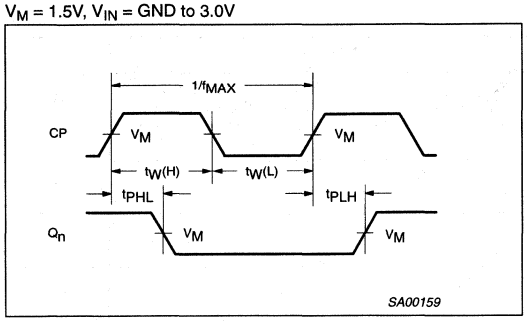
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

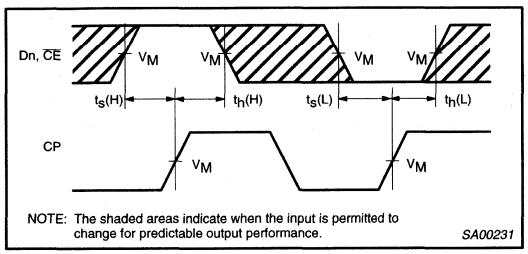
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	3	2.1 2.1	0.5 0.2	2.1 2.1	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	3	1.3 1.3	0.0 –0.3	1.3 1.3	ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	1	2.9 3.8	1.9 2.8	2.9 3.8	ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	3	2.0 3.3	–0.5 1.5	2.0 3.3	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	3	1.0 2.0	–1.4 0.7	1.0 2.0	ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	2	5.5	4.0	5.5	ns
t_{rec}	Recovery time $\overline{MR}$ to CP	2	2.5	0.6	2.5	ns

AC WAVEFORMS

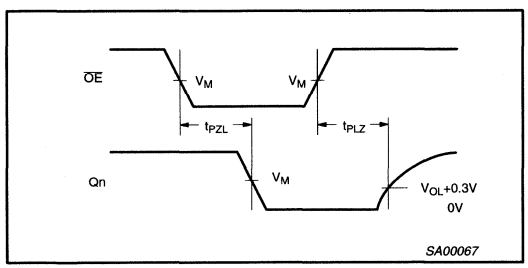
V_M = 1.5V, V_{IN} = GND to 3.0V



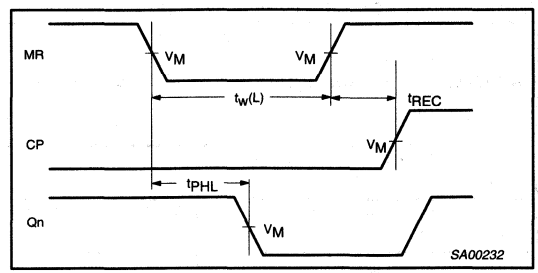
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



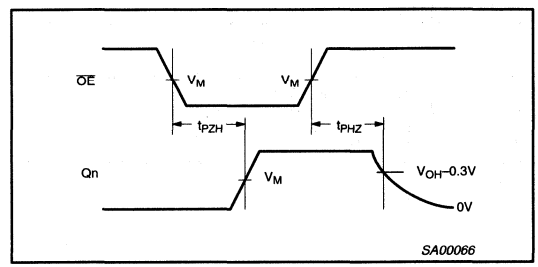
Waveform 3. Data Setup and Hold Times



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

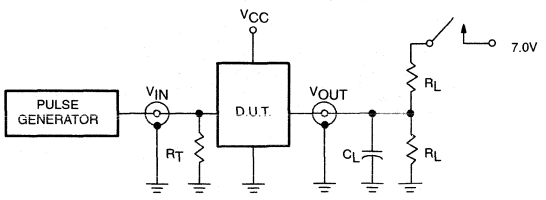


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

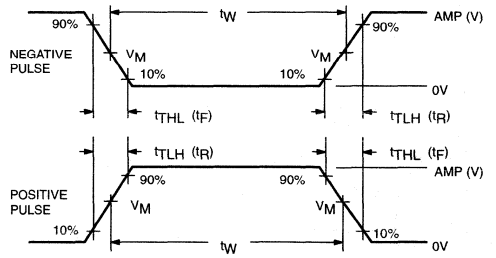


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

10-bit buffer/line driver, non-inverting (3-State) 74ABT827

FEATURES

- Ideal where high speed, light loading, or increased fan-in are required
- Flow through pinout architecture for microprocessor oriented applications
- Output capability: +64mA/–32mA
- Slim 300 mil-wide plastic 24-pin package
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT827 10-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE}0$, $\overline{OE}1$) for maximum control flexibility.

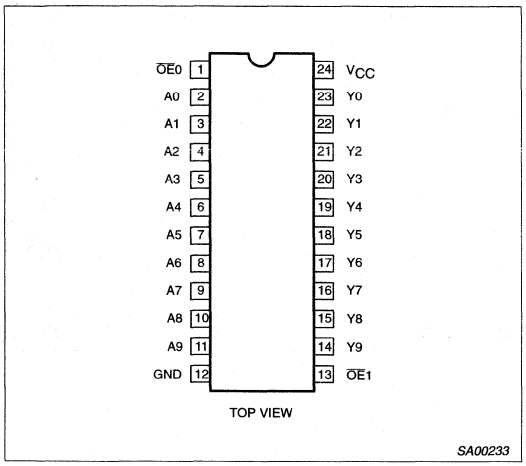
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 5V	3.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT827 N	74ABT827 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT827 D	74ABT827 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT827 DB	74ABT827 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT827 PW	74ABT827PW DH	SOT355-1

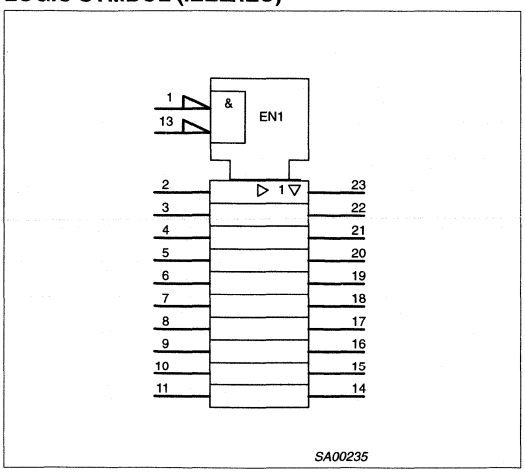
PIN CONFIGURATION



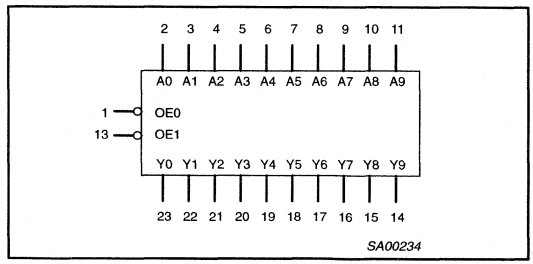
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 13	$\overline{OE}0$, $\overline{OE}1$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A0-A9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Y0-Y9	Data outputs
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL

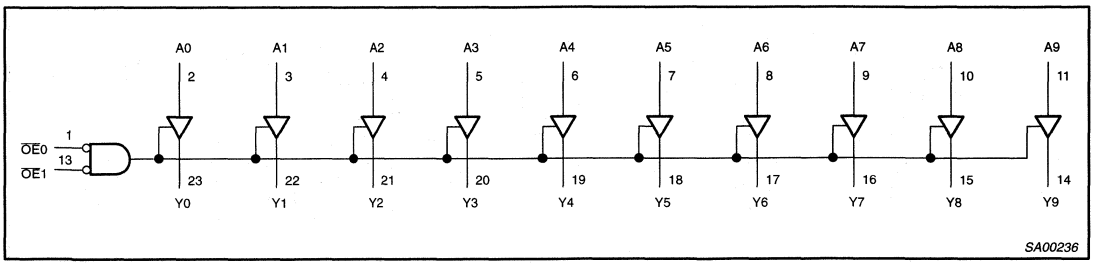


FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$\overline{OE}n$	An	Yn	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output HIgh leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		25	38		38	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.01	50		50	mA
		Outputs 3–State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

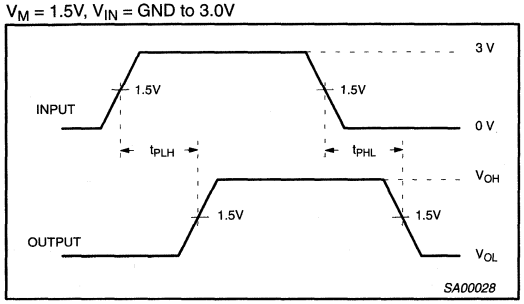
AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

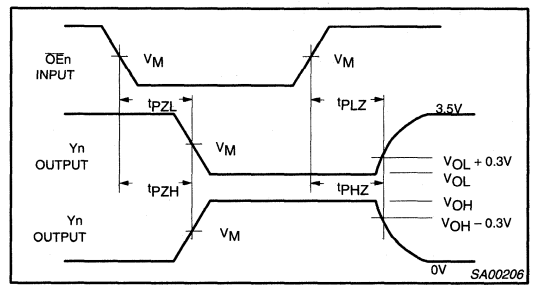
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.1 1.1	3.0 2.9	4.4 4.1	1.1 1.1	4.8 4.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.6 2.6	3.7 4.6	5.1 5.9	1.6 2.6	5.9 6.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.0 2.5	4.8 5.1	6.3 6.6	2.0 2.5	6.8 6.9	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

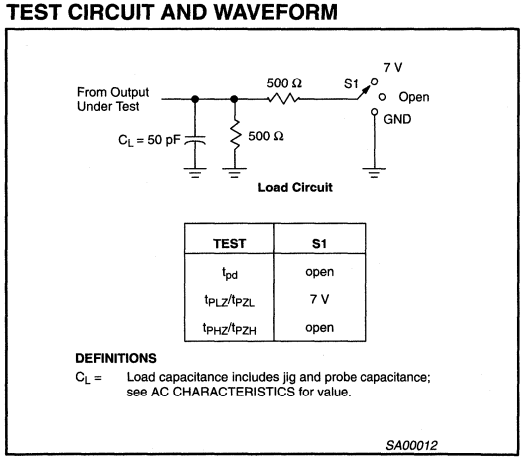


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

Octal transceiver with parity generator/checker (3-State)

74ABT833

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector $\overline{\text{ERROR}}$ output with flag register
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up/down 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT833 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT833 is an octal transceiver with a parity generator/checker and is intended for bus-oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a storage register. If a Low-to-High transition happens at the clock input (CP), the error data is stored in the register and the Open-collector error flag ($\overline{\text{ERROR}}$) will go Low. The error flag register is cleared with a Low pulse on the $\overline{\text{CLEAR}}$ input.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

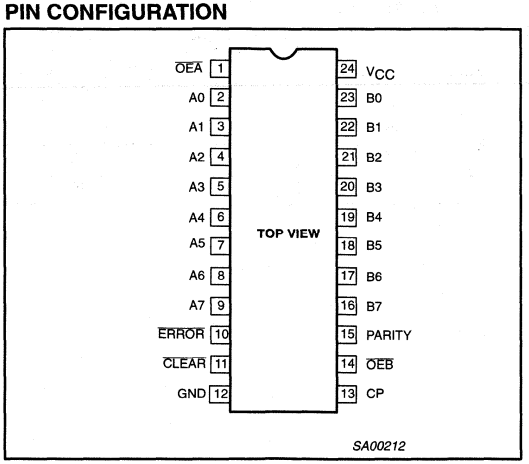
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.4	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	7.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT833 N	74ABT833 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT833 D	74ABT833 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT833 DB	74ABT833 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT833 PW	74ABT833PW DH	SOT355-1

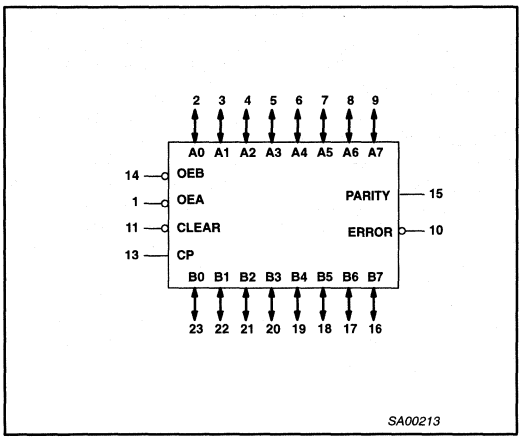
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 – A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3-State inputs/outputs
B0 – B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3-State inputs/outputs
$\overline{\text{OEA}}$	1	Enables the A outputs when Low
$\overline{\text{OEB}}$	14	Enables the B outputs when Low
PARITY	15	Parity output/input
$\overline{\text{ERROR}}$	10	Error output (open collector)
$\overline{\text{CLEAR}}$	11	Clears the error flag register when Low
CP	13	Clock input
GND	12	Ground (0V)
V_{CC}	24	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

MODE	INPUTS				OUTPUTS		
	$\overline{OEB}$	$\overline{OEA}$	An Σ of Highs	Bn + Parity Σ of Highs	An	Bn	PARITY
A data to B bus and generate odd parity output	L	H	Odd Even	(output)	(input)	An	L H
B data to A bus and check for parity error[1]	H	L	(output)	X	Bn	(input)	(input)
A bus and B bus disabled[2]	H	H	X	X	Z	Z	Z
A data to B bus and generate inverted parity output	L	L	Odd Even	(output)	(input)	An	H L

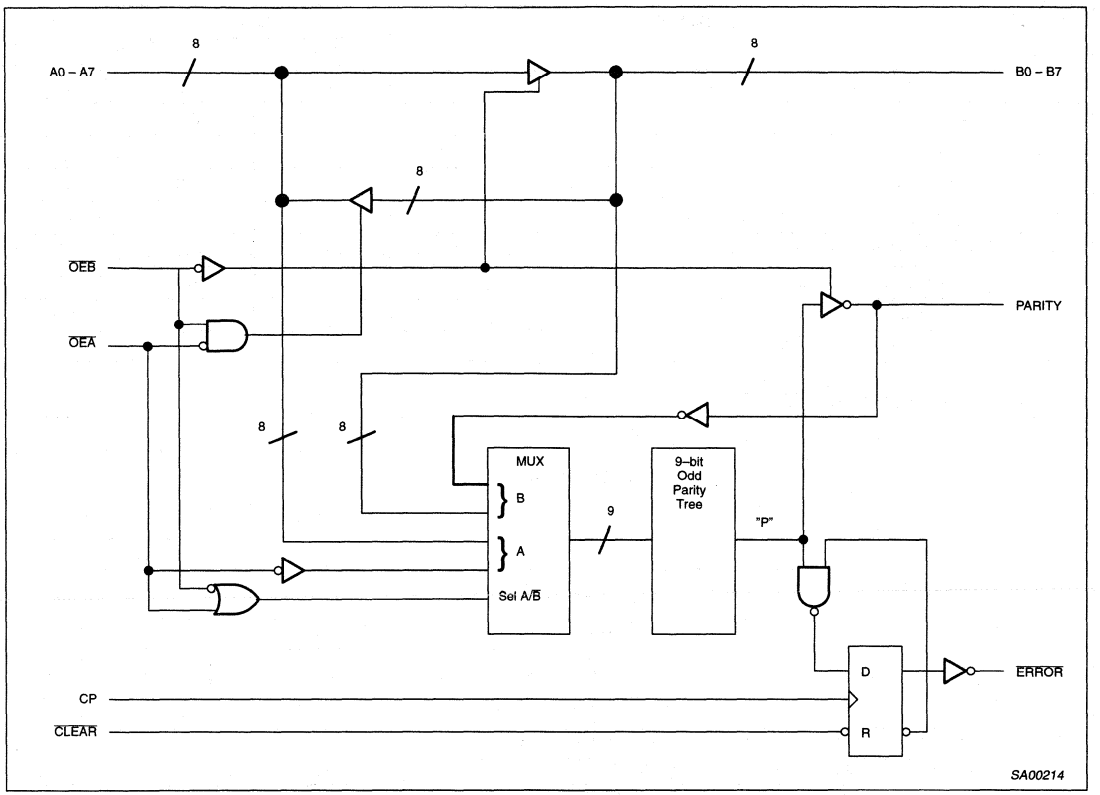
NOTES:
1. Error checking is detailed in the Error Flag Function Table below.
2. When clocked, the error output is Low if the sum of A inputs is even or High if the sum of A inputs is odd.

ERROR FLAG FUNCTION TABLE

MODE	INPUTS			Internal node	Output	
	CLEAR	CP	Bn + Parity Σ of Highs	Point "P"	Pre-state $\overline{ERROR}n-1$	$\overline{ERROR}$ OUTPUT
Sample	H H H	↑ ↑ X	Odd Even X	H L X	H X L	H L L
Hold	H	↥	X	X	X	NC
Clear	L	X	X	X	X	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
NC = No change
Z = High impedance "off" state
↑ = Low-to-High clock transition
↥ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
V_{OH}	High-level output voltage, $\overline{ERROR}$		5.5	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
I_{OH}	High-level output current $\overline{ERROR}$ ONLY		V_{CC} = 5.5V; V_{OH} = 5.5V; V_I = V_{IL} or V_{IH}			20		20	µA
V_{OH}	High-level output voltage All outputs except $\overline{ERROR}$		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V		±5.0	±100		±100	V
$I_{PU}I_{PD}$	Power-up/down 3-State output current[3]		V_{CC} = 2.0V; or V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = Don't care		±5.0	±50		±50	V
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition of up to 100µsec is permitted. The $\overline{ERROR}$ output pin 10 is not included in this spec due to the open collector design.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.2 1.0	3.4 2.6	4.8 4.0	1.2 1.0	5.3 4.5	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	1 2	2.1 2.5	7.4 7.4	9.5 9.7	2.1 2.5	11.2 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEA}$ to PARITY	1 2	2.6 3.1	6.6 6.7	8.5 8.6	2.6 3.1	10.5 10.0	ns
t_{PLH}	Propagation delay $\overline{CLEAR}$ to $\overline{ERROR}$	5	1.0	2.9	4.4	1.0	5.2	ns
t_{PHL}	Propagation delay CP to $\overline{ERROR}$	1	2.5	4.2	5.7	2.5	6.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An or $\overline{OEB}$ to Bn, PARITY	3 4	1.0 2.1	3.2 4.1	5.1 5.8	1.0 2.1	6.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An or $\overline{OEB}$ to Bn, PARITY	3 4	3.1 3.2	5.1 5.6	7.3 7.7	3.1 3.2	7.9 8.1	ns

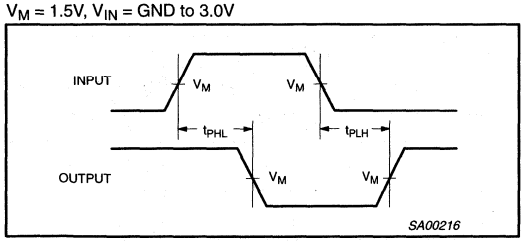
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

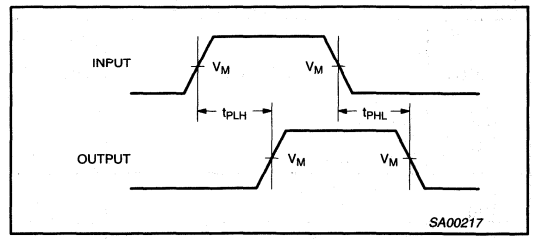
SYMBOL	PARAMETER	WAVEFORMS	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%	
			Min	Typ	Min	
t_s(H) t_s(L)	Setup time, High or Low Bn or PARITY to CP	6	9.8 8.1	6.9 4.0	9.8 8.1	ns
t_h(H) t_h(L)	Hold time, High or Low Bn or PARITY to CP	6	0.0 0.0	−3.7 −6.7	0.0 0.0	ns
t_w(H) t_w(L)	Pulse width, High or Low CP	6	3.0 3.0	1.5 1.0	3.0 3.0	ns
t_w(L)	Pulse width, Low $\overline{CLEAR}$	5	3.0	1.0	3.0	ns
t_{rec}	Recovery time $\overline{CLEAR}$ to CP	5	2.0	−0.3	2.0	ns

AC WAVEFORMS

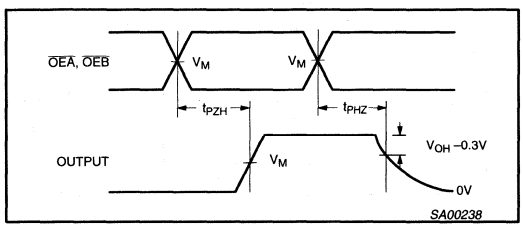
V_M = 1.5V, V_{IN} = GND to 3.0V



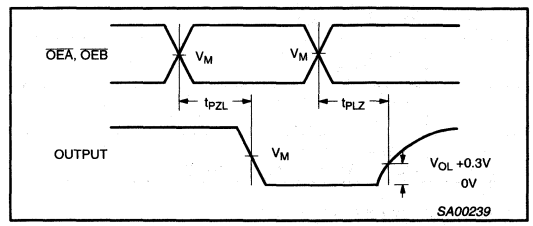
Waveform 1. Propagation Delay For Inverting Output



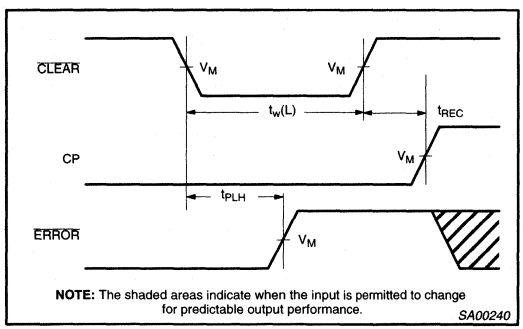
Waveform 2. Propagation Delay For Non-Inverting Output



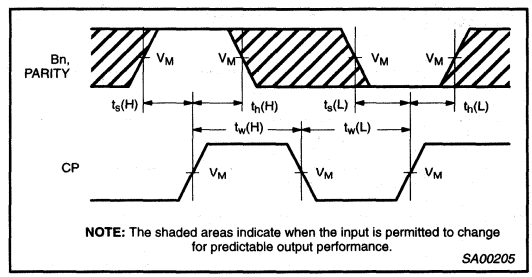
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

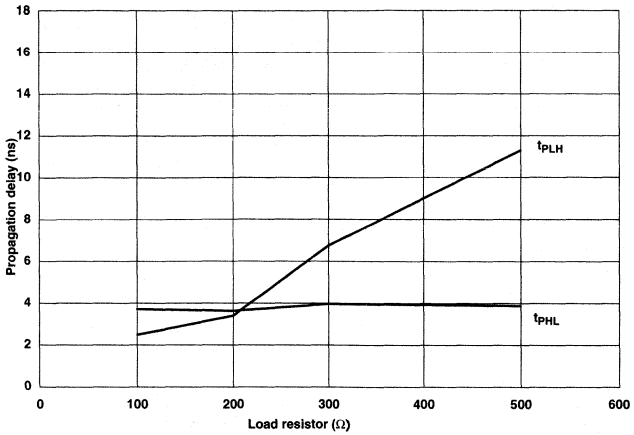


Waveform 5. $\overline{CLEAR}$ Pulse Width, $\overline{CLEAR}$ to $\overline{ERROR}$ Delay and $\overline{CLEAR}$ to Clock Recovery Time



Waveform 6. Data Setup and Hold Times and Clock Pulse Width

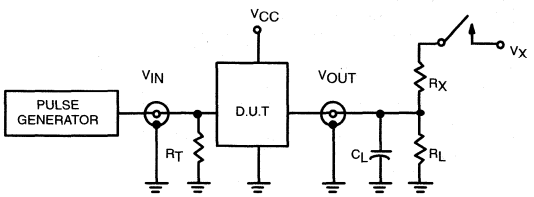
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



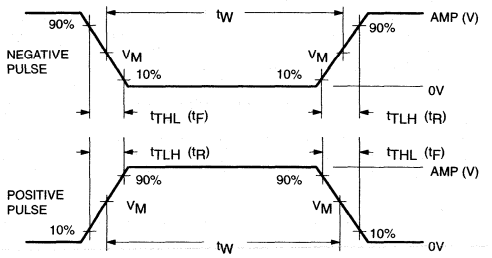
NOTE:
When using Open-Collector parts, the value of the pull–up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} over 300% with only a slight change in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

SA00241

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

LOAD VALUES

OUTPUT	R_X	V_X
$\overline{ERROR}$	100Ω	V_{CC}
All other	500Ω	7.0V

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00242

10-bit bus interface latch (3-State) 74ABT841

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Slim DIP 300 mil package
- Broadside pinout
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT841 Bus interface register is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the High-impedance state.

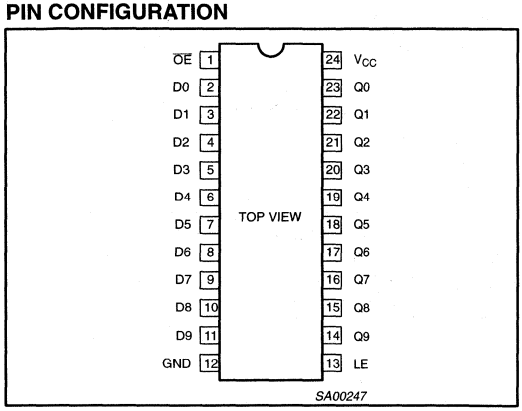
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	4.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT841 N	74ABT841 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT841 D	74ABT841 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT841 DB	74ABT841 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT841 PW	74ABT841PW DH	SOT355-1

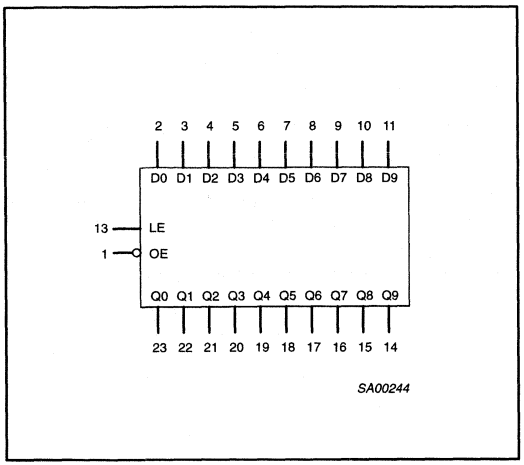
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D0-D9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q0-Q9	Data outputs
13	LE	Latch enable input (active falling edge)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL

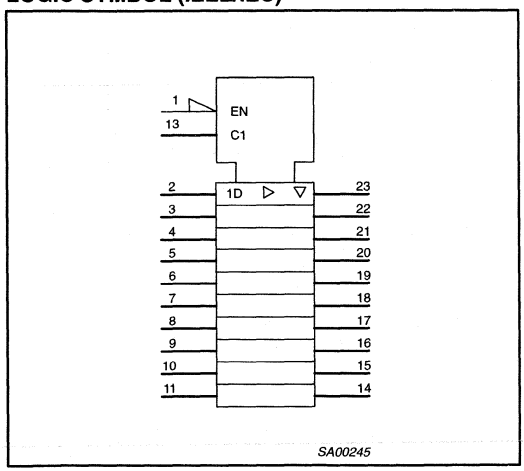


FUNCTION TABLE

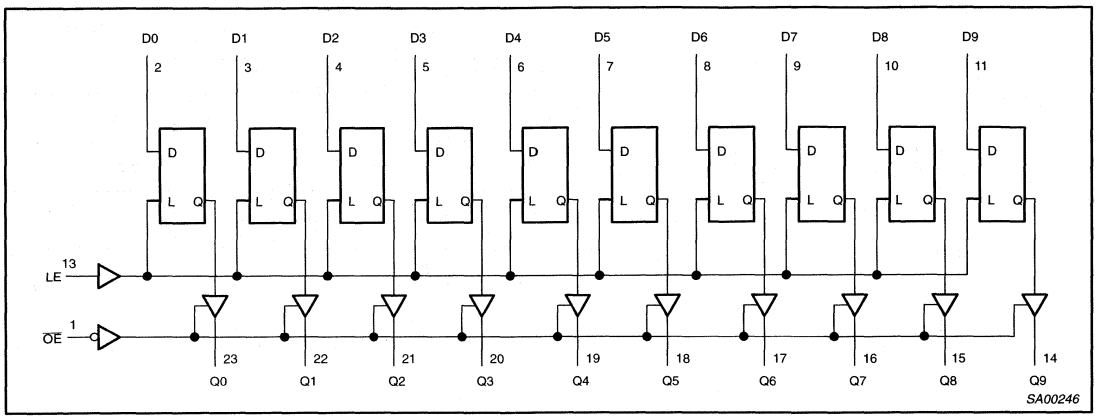
INPUTS			OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	Dn	Q0 – Q9	
L L	H H	L H	L H	Transparent
L L	↓ ↓	l h	L H	Latched
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
↓ = High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current — Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
	Input leakage current — Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-state output current[4]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = V_{CC}		±5.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−100	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		25	38		38	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	2	2.1 2.0	4.1 4.0	5.5 5.5	2.1 2.0	6.2 6.2	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn	1	2.1 2.8	4.1 4.6	5.9 6.2	2.1 2.8	6.5 6.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.0 2.2	3.0 4.1	4.5 5.6	1.0 2.2	5.3 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	2.7 2.8	4.7 4.6	6.2 6.1	2.7 2.8	7.1 6.5	ns

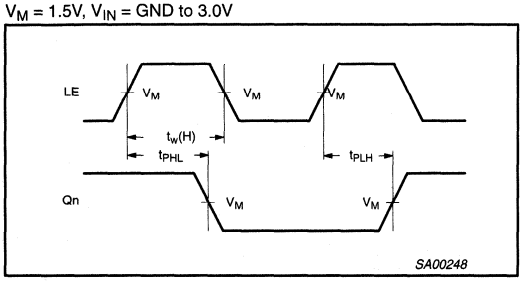
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

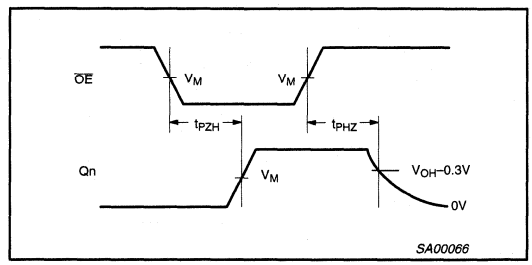
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to LE	3	2.5 1.5	1.0 0.0	2.5 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to LE	3	1.5 1.0	0.2 –0.8	1.5 1.0	ns
$t_w(H)$ $t_w(L)$	LE pulse width High or Low	1	3.3	1.9	3.3	ns

AC WAVEFORMS

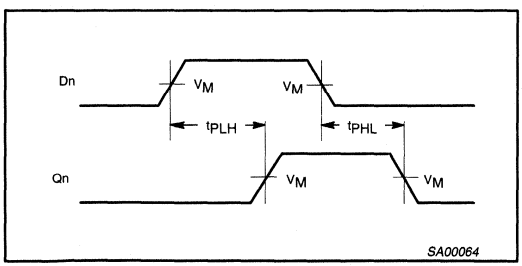
V_M = 1.5V, V_{IN} = GND to 3.0V



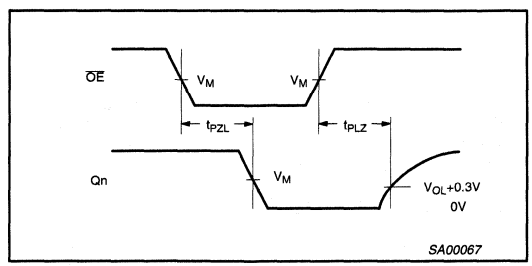
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



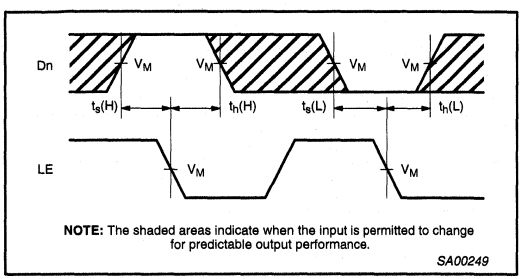
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Propagation Delay for Data to Outputs

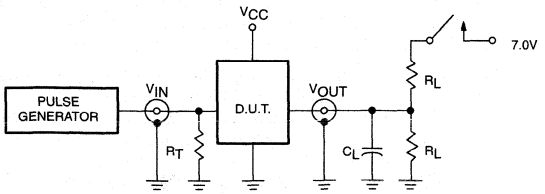


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

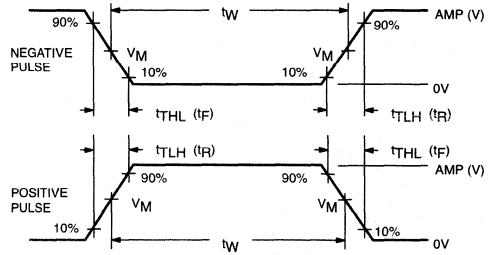


Waveform 3. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

9-bit bus interface latch with set and reset (3-State)

74ABT843

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Slim DIP 300 mil package
- Broadside pinout
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT843 Bus interface latch is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT843 consists of nine D-type latches with 3-State outputs. In addition to the LE and $\overline{OE}$ pins, it has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$.

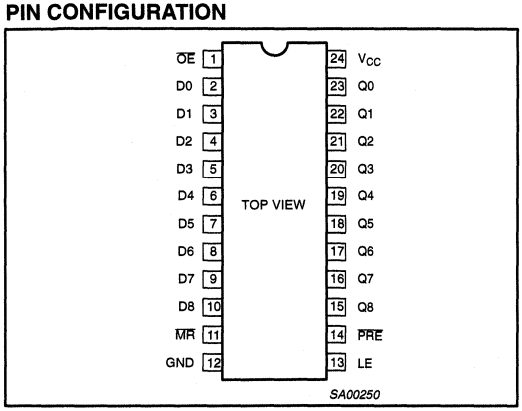
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	5.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT843 N	74ABT843 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT843 D	74ABT843 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT843 DB	74ABT843 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT843 PW	74ABT843PW DH	SOT355-1

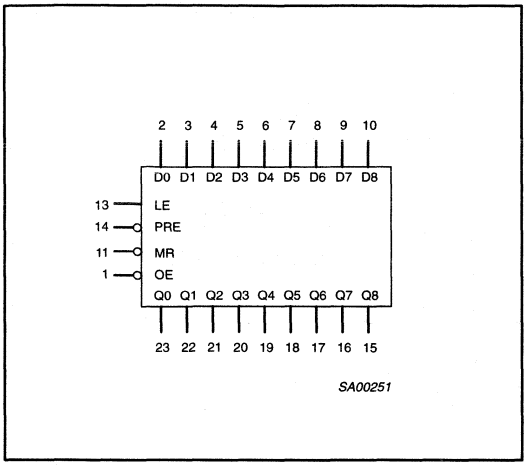
PIN CONFIGURATION



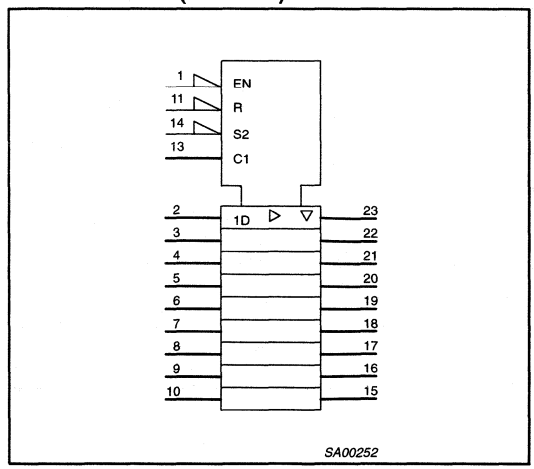
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0-D8	Data inputs
23, 22, 21, 20, 19,18, 17, 16, 15	Q0-Q8	Data outputs
11	$\overline{MR}$	Master reset input (active-Low)
13	LE	Latch enable input (active rising edge)
14	$\overline{PRE}$	Preset input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

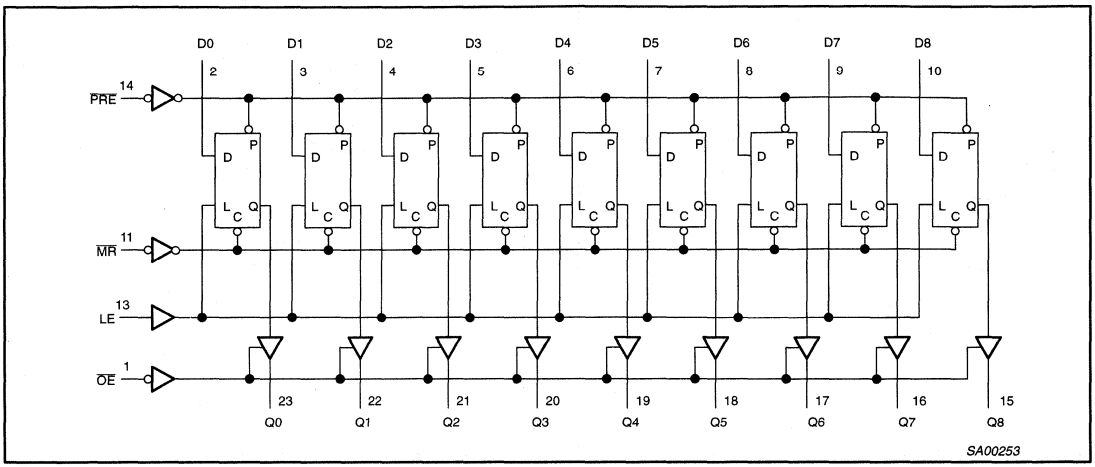


FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L L	H H	H H	H H	L H	L H	Transparent
L L	H H	H H	↓ ↓	l h	L H	Latched
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power–up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = V_{CC} or GND		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3–state output current[4]	V_{CC} = 2.0V; V_O = 0.5V; $V_{\overline{OE}} = V_{CC}$; V_I = GND or V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		25	34		34	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip–flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	1	1.6 2.2	3.6 5.0	5.2 6.3	1.6 2.2	6.0 7.2	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn	2	2.0 2.8	4.1 4.8	5.6 6.3	2.0 2.8	6.5 6.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PRE}$ to Qn	1	2.2 3.0	4.7 5.2	6.2 6.5	2.2 3.0	7.4 7.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Qn	1	2.5 3.1	5.0 5.5	6.3 6.8	2.5 3.1	7.1 8.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to Qn	4 5	1.0 2.0	2.7 4.2	4.2 5.5	1.0 2.0	5.2 6.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to Qn	4 5	2.9 2.2	4.9 5.0	6.2 6.3	2.9 2.2	6.8 6.7	ns

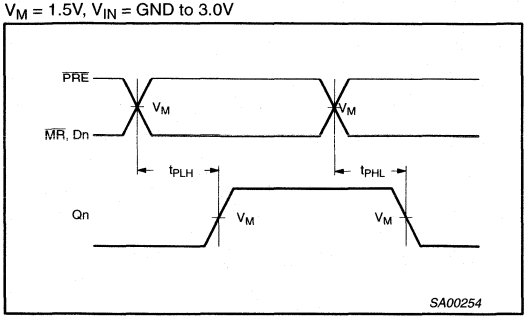
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

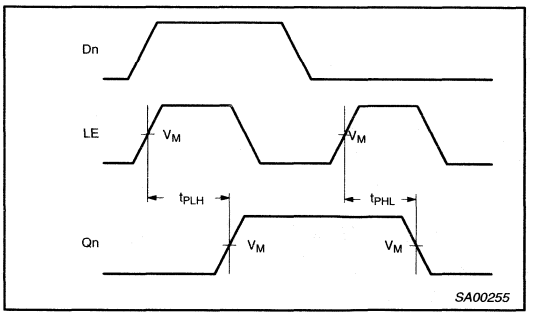
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to LE	3	2.5 3.0	1.1 1.3	2.5 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to LE	3	1.0 1.0	−1.0 −1.0	1.0 1.0	ns
$t_w(H)$	LE pulse width, High	3	3.3	1.8	3.3	ns
$t_w(L)$	$\overline{PRE}$ pulse width, Low	6	4.5	3.0	4.5	ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	6	5.5	4.0	5.5	ns
t_{rec}	$\overline{PRE}$ recovery time	6	2.9	1.6	2.9	ns
t_{rec}	$\overline{MR}$ recovery time	6	3.6	2.0	3.6	ns

AC WAVEFORMS

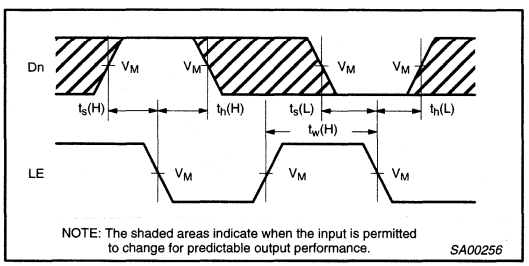
V_M = 1.5V, V_{IN} = GND to 3.0V



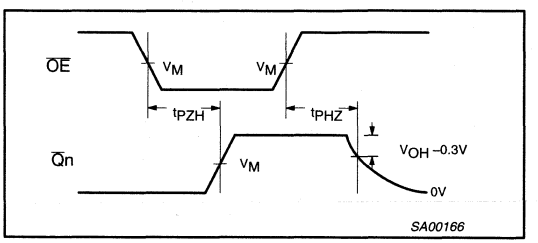
Waveform 1. Propagation Delay, Data to Output, Master Reset to Output, Preset to Output



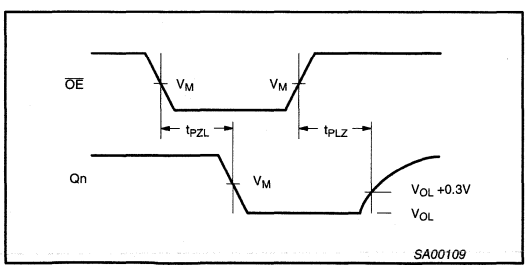
Waveform 2. Propagation Delay, Latch Enable to Output



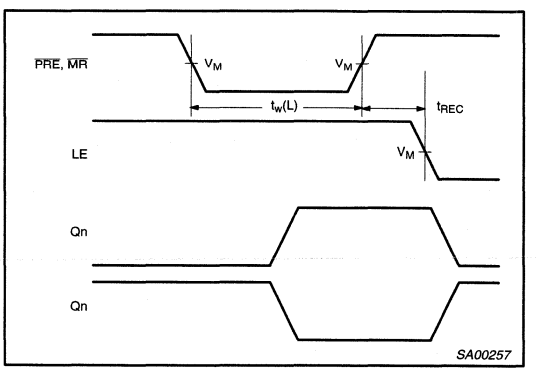
Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

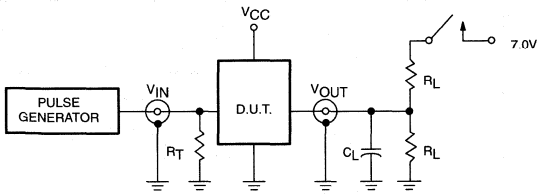


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

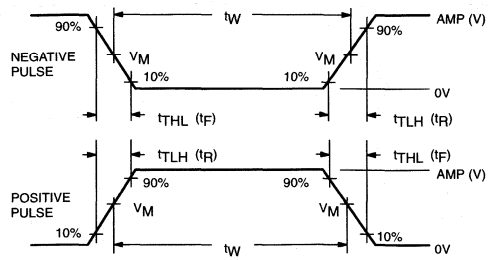


Waveform 6. Master Reset and Preset Pulse Width, Master Reset and Preset to Latch Enable Recovery Time

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SA00012

8-bit bus interface latch with set and reset (3-State)

74ABT845

FEATURES

- High speed parallel latches
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Broadside pinout
- Output capability: +64mA/–32mA
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT845 consists of eight D-type latches with 3-State outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 74ABT845 has two additional $\overline{OE}$ pins, making a total of three Output Enable ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$) pins. The multiple Output enables allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$.

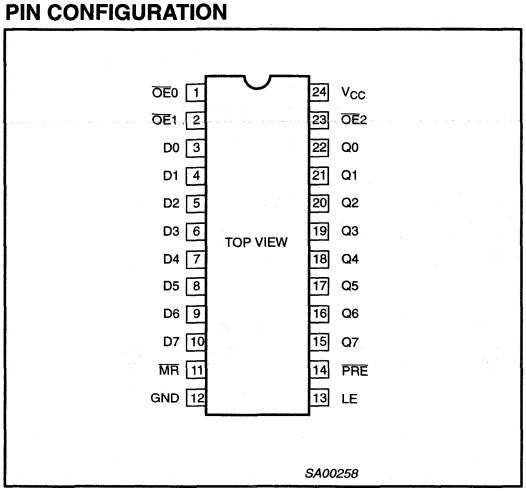
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT845 N	74ABT845 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT845 D	74ABT845 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT845 DB	74ABT845 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT845 PW	74ABT845PW DH	SOT355-1

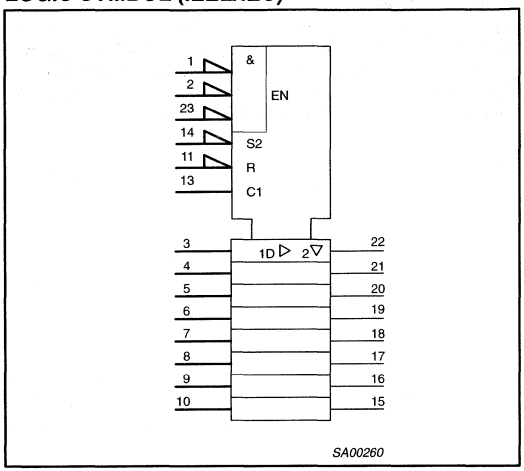
PIN CONFIGURATION



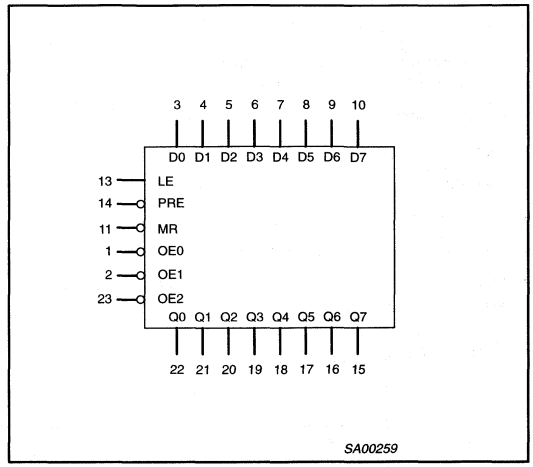
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 23	$\overline{OE}0$ – $\overline{OE}2$	Output enable inputs (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	D0-D7	Data inputs
22, 21, 20, 19,18, 17, 16, 15	Q0-Q7	Data outputs
11	$\overline{MR}$	Master reset input (active-Low)
13	LE	Latch enable input (active-High)
14	$\overline{PRE}$	Preset input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL

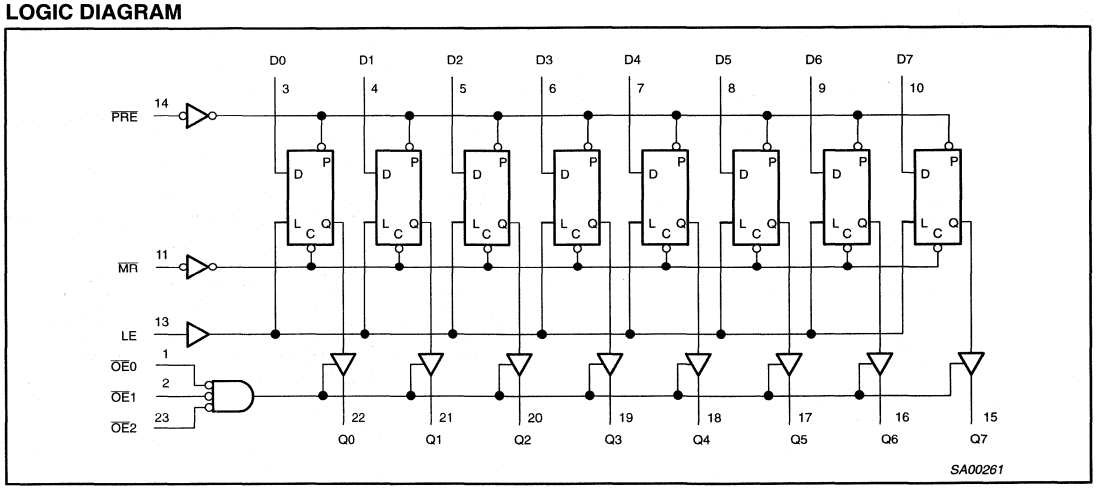


FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$ n	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L L	H H	H H	H H	L H	L H	Transparent
L L	H H	H H	↓ ↓	l h	L H	Latched
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-state output current[4]	V_{CC} = 2.1V; V_O = 0.5V; $V_{\overline{OE}}$ = V_{CC}; V_I = GND or V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−80	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	1	1.0 2.2	3.9 5.4	5.4 6.8	1.0 2.2	6.2 7.8	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn	2	2.0 2.8	5.1 6.4	6.6 7.9	2.0 2.8	7.5 8.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PRE}$ to Qn	1	2.2 3.0	4.9 5.3	6.6 6.8	2.2 3.0	7.8 7.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Qn	1	2.4 3.1	4.9 5.9	6.4 7.3	2.4 3.1	7.3 8.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$n to Qn	4 5	1.0 2.0	3.8 4.7	5.4 6.1	1.0 2.0	6.3 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$n to Qn	4 5	1.9 2.2	4.6 4.7	6.2 6.4	1.9 2.2	7.2 7.0	ns

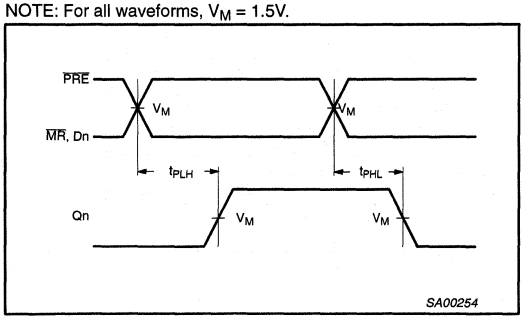
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

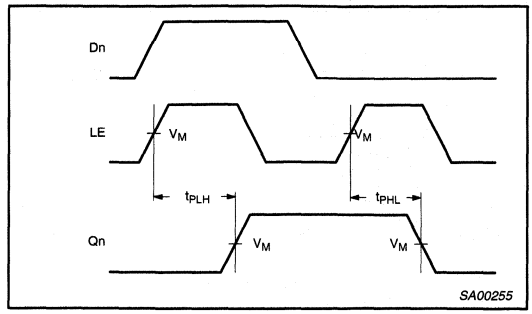
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to LE	3	2.8 3.5	1.0 1.4	2.8 3.5	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to LE	3	1.0 1.0	−1.2 −0.6	1.0 1.0	ns
$t_w(H)$	LE pulse width, High	3	3.0	1.5	3.0	ns
$t_w(L)$	$\overline{PRE}$ pulse width, Low	6	3.5	2.0	3.5	ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	6	2.8	1.3	2.8	ns
t_{rec}	$\overline{PRE}$ recovery time	6	3.0	1.4	3.0	ns
t_{rec}	$\overline{MR}$ recovery time	6	3.4	1.6	3.4	ns

AC WAVEFORMS

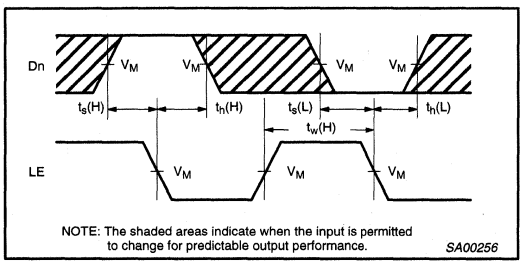
NOTE: For all waveforms, $V_M = 1.5V$.



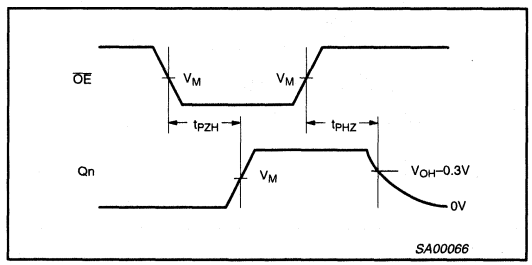
Waveform 1. Propagation Delay, Data to Output, Preset to Output, and Master Reset to Output



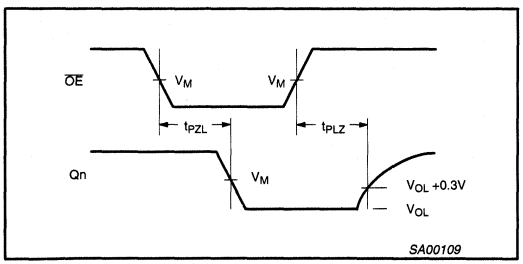
Waveform 2. Propagation Delay, Latch Enable to Output



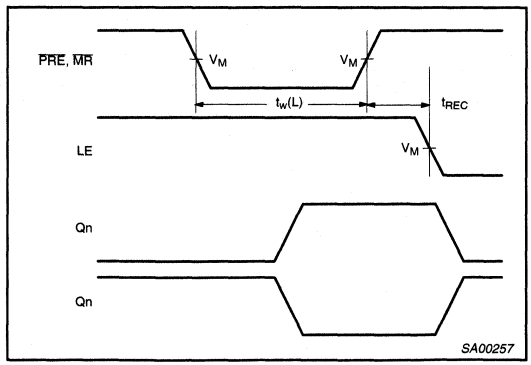
Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

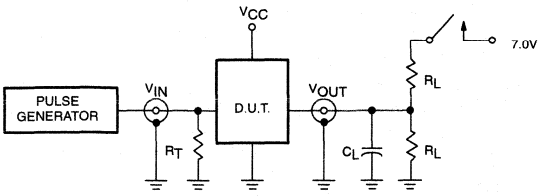


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

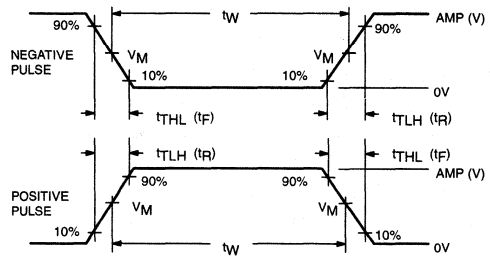


Waveform 6. Master Reset and Preset Pulse Width and Master Reset and Preset to Latch Enable Recovery Time

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

8-bit transceiver with 9-bit parity checker/generator and flag latch (3-State)

74ABT853

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector $\overline{\text{ERROR}}$ output
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT853 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT853 is an octal transceiver with a parity generator/checker and is intended for bus–oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a latch. The error data can then be passed, stored, cleared, or sampled depending on the $\overline{\text{ENABLE}}$ and $\overline{\text{CLEAR}}$ control signals.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

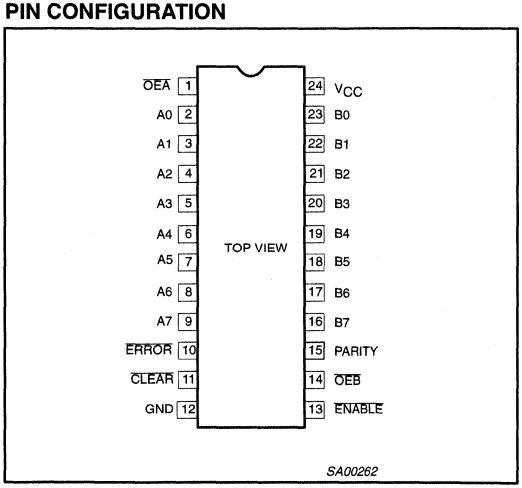
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.4	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	7.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

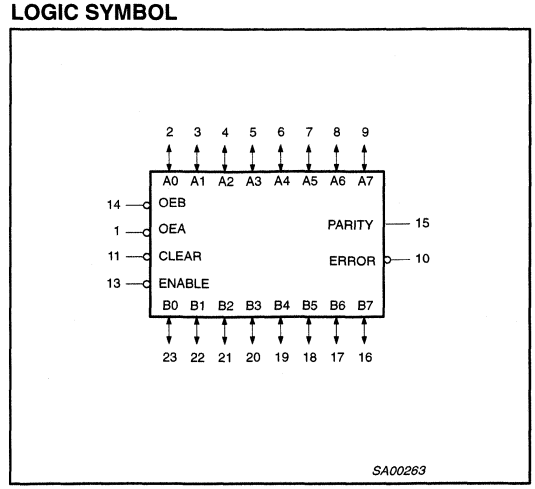
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT853 N	74ABT853 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT853 D	74ABT853 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT853 DB	74ABT853 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT853 PW	74ABT853PW DH	SOT355-1

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 – A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3–State inputs/outputs
B0 – B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3–State inputs/outputs
$\overline{OEA}$	1	Enables the A outputs when Low
$\overline{OEB}$	14	Enables the B outputs when Low
PARITY	15	Parity output/input
$\overline{ERROR}$	10	Error output (open collector)
$\overline{CLEAR}$	11	Clears the error flag register when Low
$\overline{ENABLE}$	13	Enable input (active-Low)
GND	12	Ground (0V)
V_{CC}	24	Positive supply voltage

FUNCTION TABLE

MODE	INPUTS				OUTPUTS		
	$\overline{OEB}$	$\overline{OEA}$	An Σ OF HIGHS	Bn + PARITY Σ OF HIGHS	An	Bn	PARITY
A data to B bus and generate odd parity output	L	H	Odd Even	(output)	(input)	An	L H
B data to A bus and check for parity error[1]	H	L	(output)	X	Bn	(input)	(input)
A bus and B bus disabled[2]	H	H	X	X	Z	Z	Z
A data to B bus and generate inverted parity output	L	L	Odd Even	(output)	(input)	An	H L

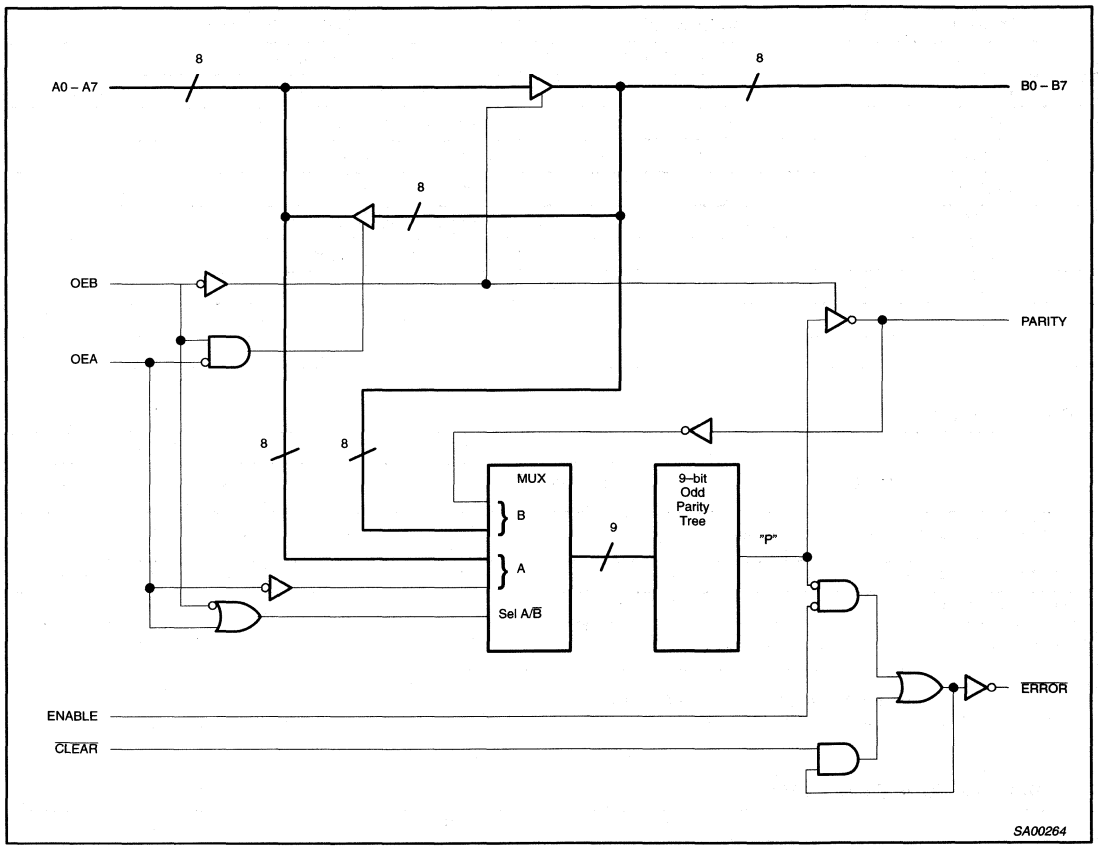
NOTES:
1. Error checking is detailed in the Error Flag Function Table below.
2. When $\overline{ENABLE}$ is Low, $\overline{ERROR}$ is Low if the sum of A inputs is even or $\overline{ERROR}$ is High if the sum of A inputs is odd.

ERROR FLAG FUNCTION TABLE

MODE	INPUTS			INTERNAL NODE	OUTPUT	
	$\overline{ENABLE}$	$\overline{CLEAR}$	Bn + PARITY Σ OF HIGHS	POINT "P"	PRE–STATE $\overline{ERROR}$n–1	$\overline{ERROR}$ OUTPUT
Pass	L	L	Odd Even	H L	X	H L
Sample	L	H	Odd Even X	H L X	H X L	H L L
Clear	H	L	X	X	X	H
Store	H	H	X	X	L H	L H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage All outputs except $\overline{ERROR}$		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		25	38		38	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.01	50		50	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted. The $\overline{ERROR}$ output pin 10 is not included in this spec due to the open collector design.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±10%		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	4	1.2 1.0	3.4 2.6	4.8 4.0	1.2 1.0	5.3 4.5	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	1, 4	2.1 2.5	7.4 7.4	9.5 9.7	2.1 2.5	11.2 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEA}$ to PARITY	1, 4	1.8 2.3	6.6 6.7	8.5 8.6	1.8 2.3	10.5 10.0	ns
t_{PLH}	Propagation delay $\overline{CLEAR}$ to $\overline{ERROR}$	3	1.0	3.6	5.5	1.0	6.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{ENABLE}$ to $\overline{ERROR}$	4	1.8 1.8	3.8 4.5	5.1 5.8	1.8 1.8	6.0 6.6	ns
t_{PLH} t_{PHL}	Propagation delay Bn or PARITY to $\overline{ERROR}$	1, 4	2.0 3.0	7.9 9.0	10.1 11.5	2.0 3.0	11.7 12.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An or $\overline{OEB}$ to Bn, PARITY	2, 5	1.0 2.1	3.2 4.1	5.1 5.8	1.0 2.1	6.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An or $\overline{OEB}$ to Bn, PARITY	2, 5	3.1 3.2	5.1 5.6	7.3 7.2	3.1 3.2	7.9 8.1	ns

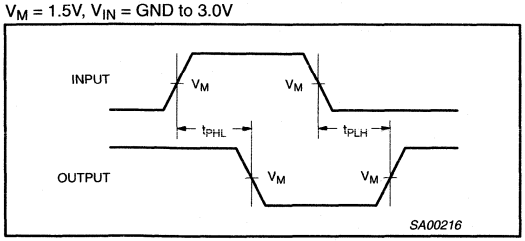
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

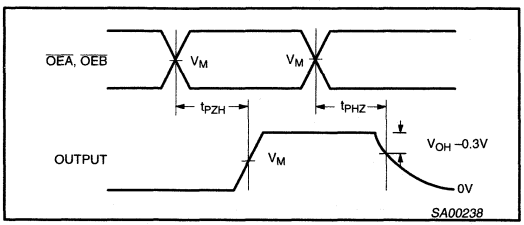
SYMBOL	PARAMETER	WAVEFORMS	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±10%	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time, High or Low Bn or PARITY to $\overline{ENABLE}$	6	8.5 8.5	6.5 3.6	8.5 8.5	ns
t_h(H) t_h(L)	Hold time, High or Low Bn or PARITY to $\overline{ENABLE}$	6	0.0 0.0	–3.4 –6.3	0.0 0.0	ns
t_s(H)	Setup time, High $\overline{CLEAR}$ to $\overline{ENABLE}$	6	2.0	–1.6	2.0	ns
t_h(L)	Hold time, Low $\overline{CLEAR}$ to $\overline{ENABLE}$	6	3.0	1.8	3.0	ns
t_w(L)	Pulse width, Low $\overline{CLEAR}$	3	3.5	1.0	3.5	ns
t_w(L)	Pulse width, Low $\overline{ENABLE}$	6	4.0	2.5	4.0	ns

AC WAVEFORMS

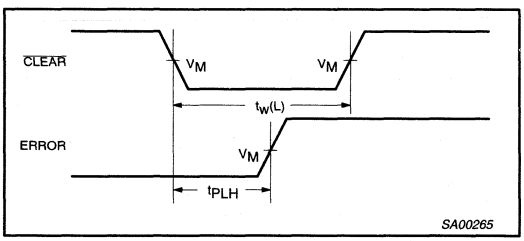
V_M = 1.5V, V_{IN} = GND to 3.0V



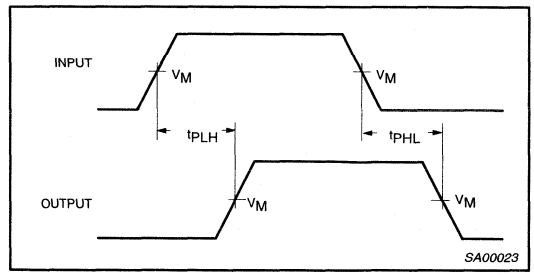
Waveform 1. Propagation Delay For Inverting Output



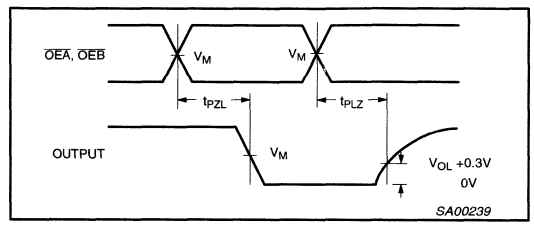
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



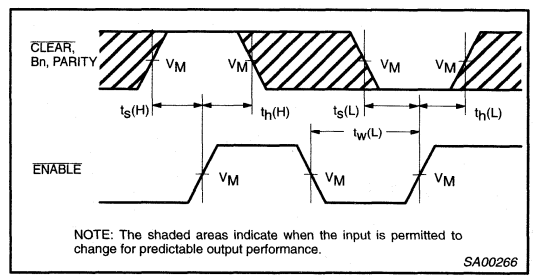
Waveform 3. $\overline{\text{CLEAR}}$ Pulse Width and $\overline{\text{CLEAR}}$ to $\overline{\text{ERROR}}$ Delay



Waveform 4. Propagation Delay For Non-Inverting Output

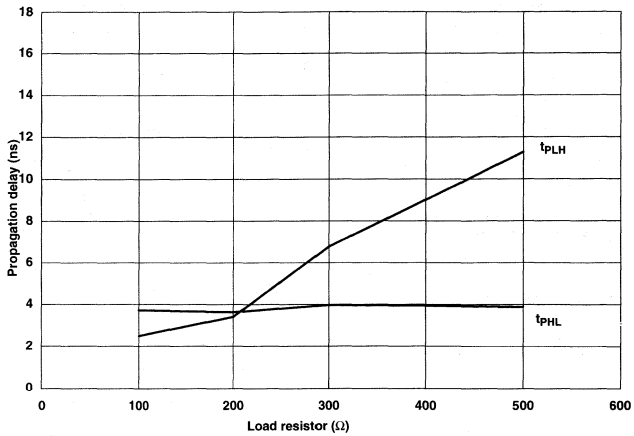


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 6. Data Setup and Hold Times and $\overline{\text{ENABLE}}$ Pulse Width

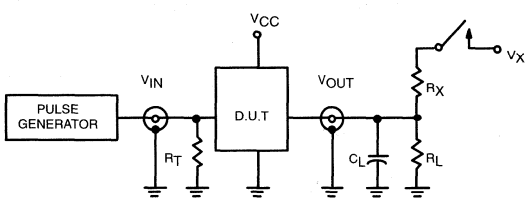
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



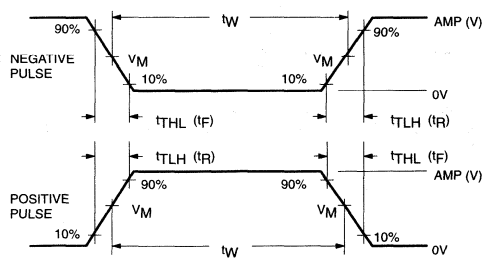
NOTE:
When using Open-Collector parts, the value of the pull–up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} over 300% with only a slight change in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

SA00241

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

LOAD VALUES

OUTPUT	R_X	V_X
$\overline{ERROR}$	100Ω	V_{CC}
All other	500Ω	7.0V

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00242

10-bit bus transceiver (3-State) 74ABT861

FEATURES

- Provides high performance bus interface buffering for wide data/address paths or buses carrying parity
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT861 bus transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity.

The 74ABT861 10-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

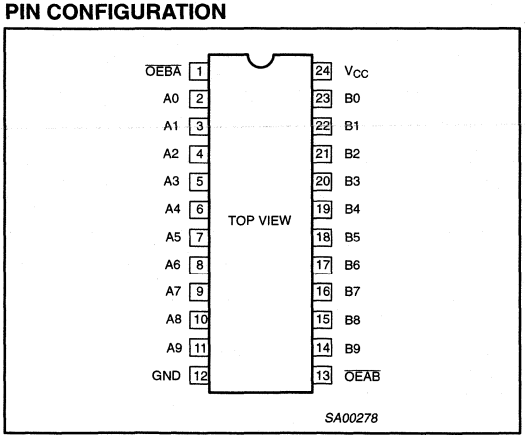
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT861 N	74ABT861 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT861 D	74ABT861 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT861 DB	74ABT861 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT861 PW	74ABT861PW DH	SOT355-1

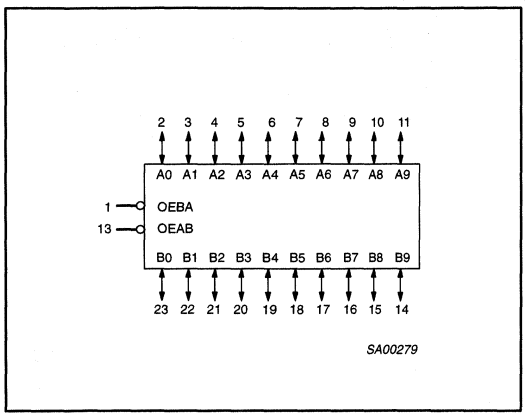
PIN CONFIGURATION



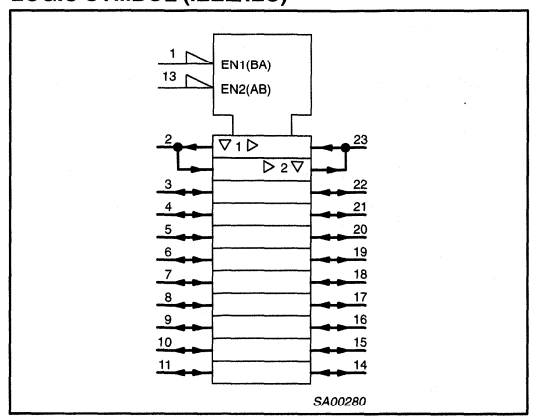
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
13	$\overline{OEAB}$	A side to B side output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A0-A9	Data inputs/outputs (A side)
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	B0-B9	Data inputs/outputs (B side)
1	$\overline{OEBA}$	B side to A side output enable input (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

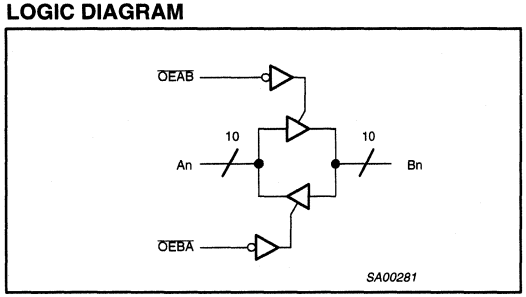
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODE
$\overline{OEAB}$	$\overline{OEBA}$	
L	H	A data to B bus
H	L	B data to A bus
H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low–level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5.0	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power–up/down 3-State output current[3]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = V_{CC}		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		25	38		38	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.01	50		50	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

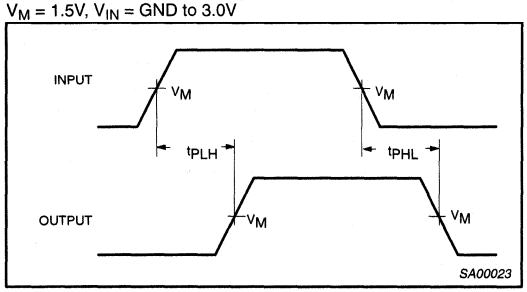
AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

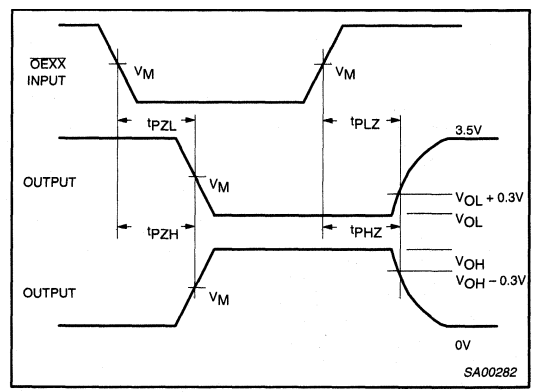
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.1 1.0	3.4 3.2	4.9 4.9	1.1 1.0	5.2 5.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.2 2.4	3.5 4.6	5.0 6.0	1.2 2.4	5.9 6.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	3.1 3.7	5.3 5.3	6.5 6.6	3.1 3.7	7.5 7.1	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

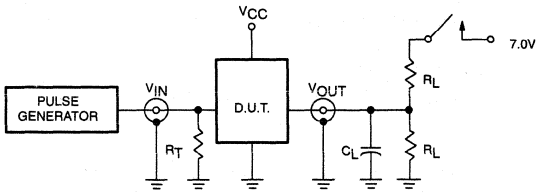


Waveform 1. Input to Output Propagation Delays

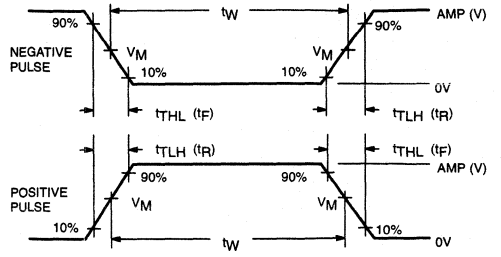


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

9-bit bus transceiver (3-State) 74ABT863

FEATURES

- Provides high performance bus interface buffering for wide data/address paths or buses carrying parity
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT863 bus transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity.

The 74ABT863 9-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

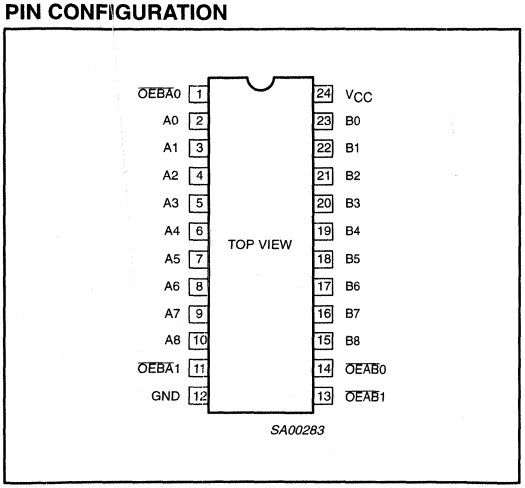
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	110	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT863 N	74ABT863 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT863 D	74ABT863 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT863 DB	74ABT863 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT863 PW	74ABT863PW DH	SOT355-1

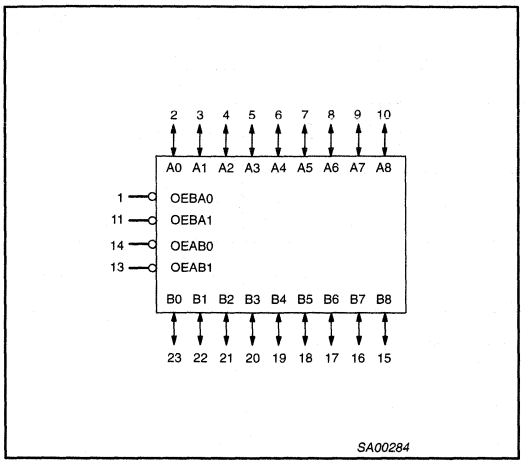
PIN CONFIGURATION



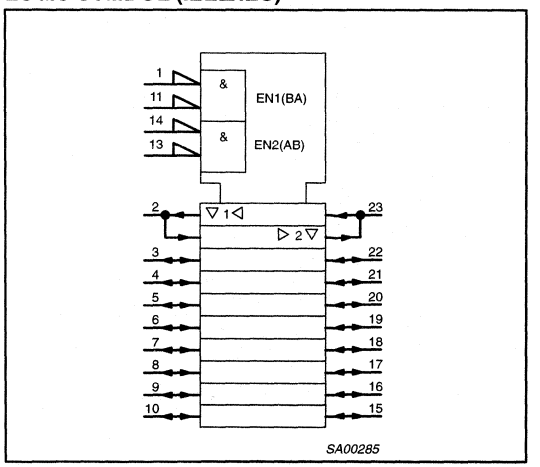
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 13	$\overline{OEAB}$0, $\overline{OEAB}$1	Output enable inputs (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	A0-A8	Data inputs/outputs (A side)
23, 22, 21, 20, 19, 18, 17, 16, 15	B0-B8	Data inputs/outputs (B side)
1, 11	$\overline{OEBA}$0, $\overline{OEBA}$1	Output enable inputs (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

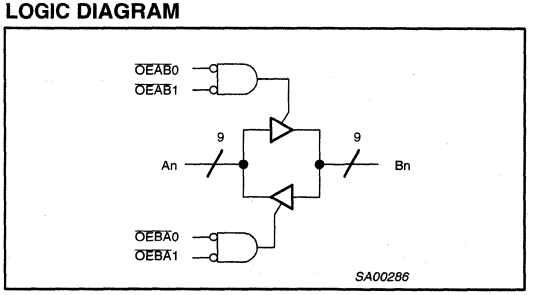


FUNCTION TABLE

INPUTS				OPERATING MODE
$\overline{OEAB0}$	$\overline{OEAB1}$	$\overline{OEBA0}$	$\overline{OEBA1}$	
L L	L L	H X	X H	A data to B bus A data to B bus
H X	X H	L L	L L	B data to A bus B data to A bus
H	H	H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.2		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.7		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.3		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]		V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; = V_{OE}= Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–63	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		25	38		38	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		110	250		250	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

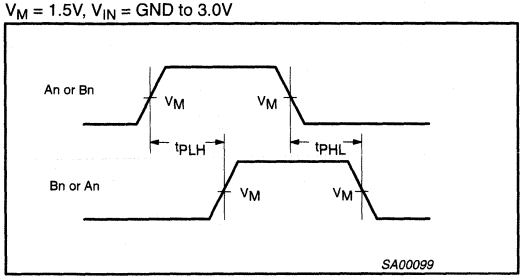
AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

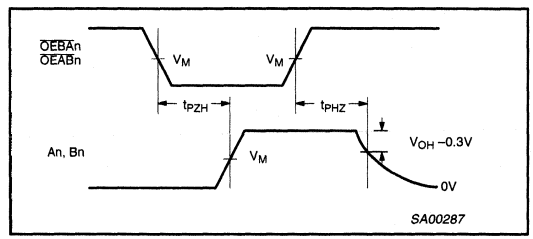
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A0–7 to B0–7 or Bn to An	1	1.3	3.3	4.8	1.3	5.3	ns
	A8 to B8		1.3	4.5	5.9	2.5	6.3	
t_{PHL}	An to Bn or Bn to An		1.2	2.8	4.6	1.2	5.2	
t_{PZH}	Output enable time $\overline{OEBA}$n to An or $\overline{OEAB}$n to B0–7	2	1.3	4.3	5.5	1.3	6.5	ns
	$\overline{OEAB}$n to B8		1.3	4.9	6.4	2.4	7.5	
t_{PZL}	$\overline{OEBA}$n to An or $\overline{OEAB}$n to Bn	3	2.2	5.2	6.3	2.2	7.3	
t_{PHZ}	Output disable time	2	3.0	5.0	6.3	3.0	7.1	ns
t_{PLZ}	from High and Low level	3	2.5	4.8	6.3	2.5	6.8	

AC WAVEFORMS

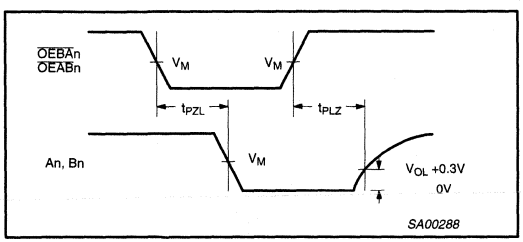
V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Propagation Delay for Data to Outputs

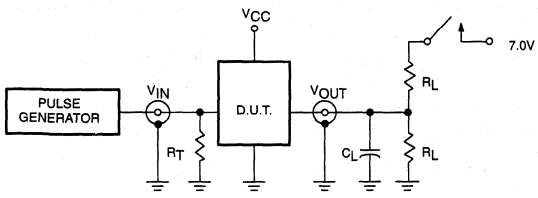


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

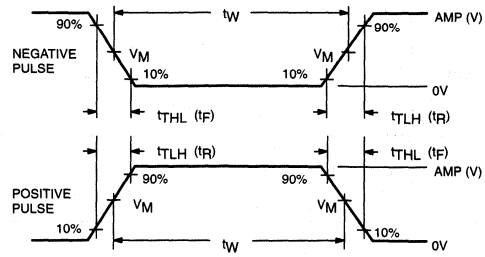


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899

FEATURES

- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/$\overline{\text{EVEN}}$ parity
- Continuously checks parity of both A bus and B bus latches as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data
- Output capability: +64 mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT899 is a 9-bit to 9-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the $\overline{\text{SEL}}$ input.

Parity error checking of the A and B bus latches is continuously provided with $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$, even with both buses in 3-State.

The 74ABT899 features independent latch enables for the A and B bus latches, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION

The 74ABT899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEA and LEB are High and the Mode Select ($\overline{\text{SEL}}$) is Low, the parity generated from A0-A7 and B0-B7 can be checked and monitored by $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$. (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is High. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ and can be used as an interrupt to signal a data/parity bit error to the CPU.

Latched input, Generate/Feed-through parity, Check A (and B) bus parity:
Independent latch enables (LEA and LEB) allow other permutations of:

- Transparent latch / 1 bus latched / both buses latched
- Feed-through parity / generate parity
- Check in bus parity / check out bus parity / check in and out bus parity

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.9	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{\text{ERRA}}$	C_L = 50pF; V_{CC} = 5V	6.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

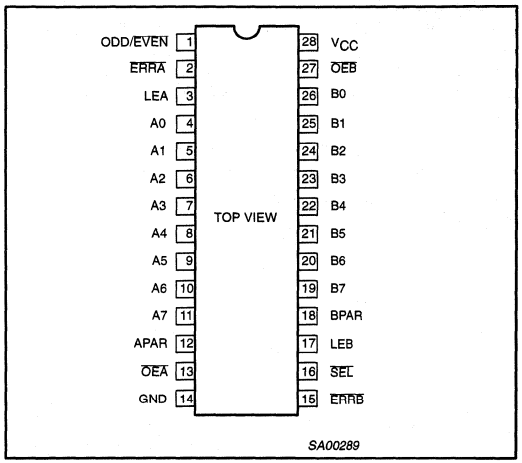
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
28-Pin Plastic PLCC	–40°C to +85°C	74ABT899 A	74ABT899 A	SOT261-3
28-Pin Plastic SOP	–40°C to +85°C	74ABT899 D	74ABT899 D	SOT136-1
28-Pin Plastic SSOP	–40°C to +85°C	74ABT899 DB	74ABT899 DB	SOT341-1

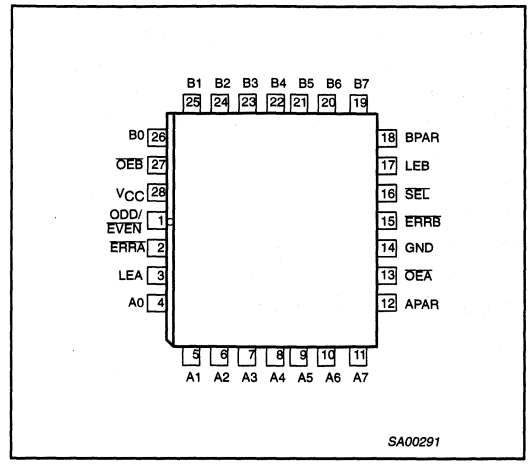
9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899

PIN CONFIGURATION



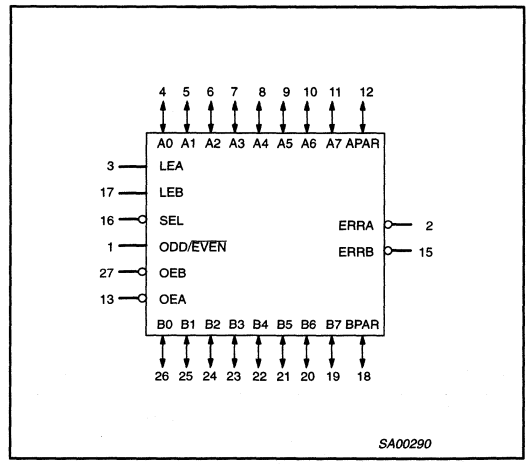
PLCC PIN CONFIGURATION



PIN DESCRIPTION

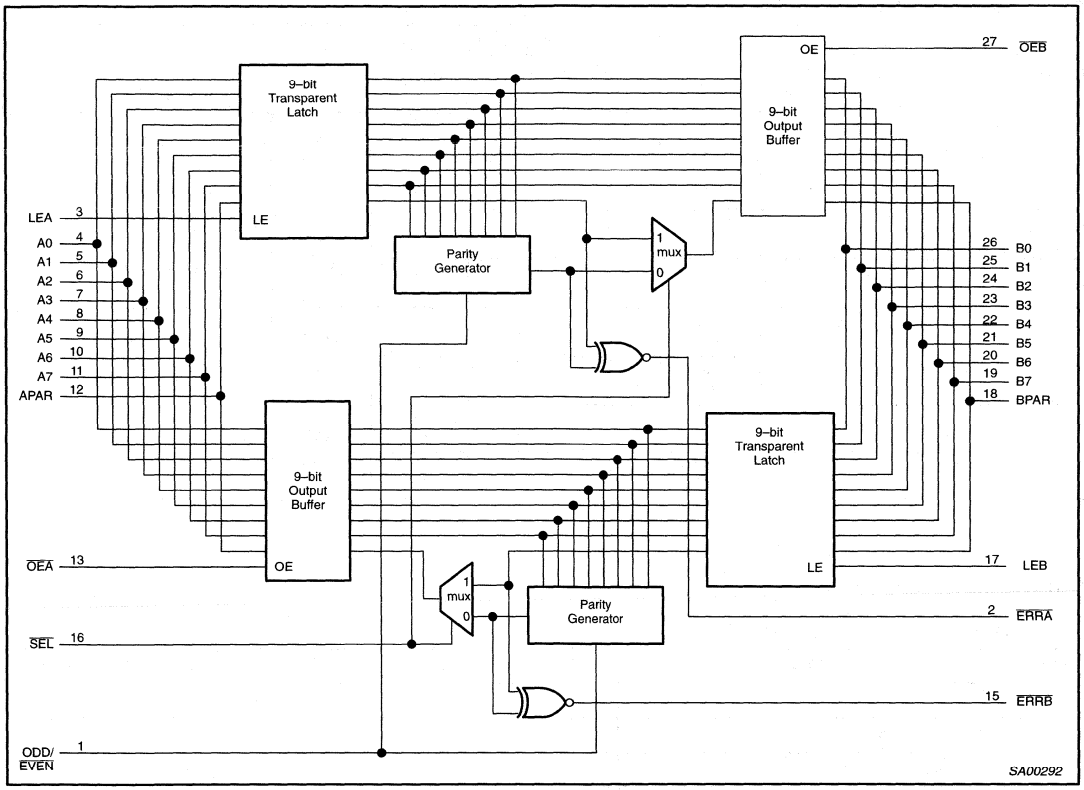
SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 - A7	4, 5, 6, 7, 8, 9, 10, 11	Latched A bus 3-State inputs/outputs
B0 - B7	19, 20, 21, 22, 23, 24, 25, 26	Latched B bus 3-State inputs/outputs
APAR	12	A bus parity 3-State input
BPAR	18	B bus parity 3-State input
ODD/EVEN	1	Parity select input (Low for EVEN parity)
$\overline{OEA}$, $\overline{OEB}$	13, 27	Output enable inputs (gate A to B, B to A)
$\overline{SEL}$	16	Mode select input (Low for generate)
LEA, LEB	3, 17	Latch enable inputs (transparent High)
$\overline{ERRA}$, $\overline{ERRB}$	2, 15	Error signal outputs (active-Low)
GND	14	Ground (0V)
V_{CC}	28	Positive supply voltage

LOGIC SYMBOL



9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)

74ABT899



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OEB}$	$\overline{OEA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	3-State A bus and B bus (input A & B simultaneously)
H	L	L	L	H	B → A, transparent B latch, generate parity from B0 - B7, check B bus parity
H	L	L	H	H	B → A, transparent A & B latch, generate parity from B0 - B7, check A & B bus parity
H	L	L	X	L	B → A, B bus latched, generate parity from latched B0 - B7 data, check B bus parity
H	L	H	X	H	B → A, transparent B latch, parity feed-through, check B bus parity
H	L	H	H	H	B → A, transparent A & B latch, parity feed-through, check A & B bus parity
L	H	L	H	X	A → B, transparent A latch, generate parity from A0 - A7, check A bus parity
L	H	L	H	H	A → B, transparent A & B latch, generate parity from A0 - A7, check A & B bus parity
L	H	L	L	X	A → B, A bus latched, generate parity from latched A0 - A7 data, check A bus parity
L	H	H	H	L	A → B, transparent A latch, parity feed-through, check A bus parity
L	H	H	H	H	A → B, transparent A & B latch, parity feed-through, check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

PARITY AND ERROR FUNCTION TABLE

INPUTS				OUTPUTS			PARITY MODES	
$\overline{SEL}$	ODD/$\overline{EVEN}$	xPAR (A or B)	Σ of High Inputs	xPAR (B or A)	$\overline{ERRt}$	$\overline{ERRr}$*		
H	H	H	Even Odd	H H	H L	H L	Odd Mode	Feed-through/check parity
H	H	L	Even Odd	L L	L H	L H		
H	L	H	Even Odd	H H	L H	L H	Even Mode	
H	L	L	Even Odd	L L	H L	H L		
L	H	H	Even Odd	H L	H L	H H	Odd Mode	Generate parity
L	H	L	Even Odd	H L	L H	H H		
L	L	H	Even Odd	L H	L H	H H	Even Mode	
L	L	L	Even Odd	L H	H L	H H		

H = High voltage level
L = Low voltage level
t = Transmit–if the data path is from A→B then $\overline{ERRt}$ is $\overline{ERRA}$
r = Receive–if the data path is from A→B then $\overline{ERRr}$ is $\overline{ERRB}$
* Blocked if latch is not transparent

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 1505C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		28	34		34	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	3.2 2.7	4.5 4.1	1.0 1.0	4.9 4.6	ns
t_{PLH} t_{PHL}	Propagation delay An to BPAR or Bn to APAR	2	3.0 2.5	6.0 6.4	7.5 7.9	3.0 2.5	9.0 8.8	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{ERRA}$ or Bn to $\overline{ERRB}$	3	2.8 2.8	6.0 6.7	8.0 8.5	2.8 2.8	9.1 9.3	ns
t_{PLH} t_{PHL}	Propagation delay APAR to BPAR or BPAR to APAR	1	2.0 1.3	4.0 3.2	5.2 4.4	2.0 1.3	5.7 5.0	ns
t_{PLH} t_{PHL}	Propagation delay APAR to $\overline{ERRA}$ or BPAR to $\overline{ERRB}$	6	1.5 1.5	4.2 4.0	5.4 5.4	1.5 1.5	6.0 6.1	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to APAR or BPAR	5	2.6 2.5	5.5 5.3	6.8 6.7	2.6 2.5	8.1 7.8	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$ or $\overline{ERRB}$	4	2.3 2.6	5.4 5.7	6.8 7.2	2.3 2.6	7.9 8.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to APAR or BPAR	8	1.3 1.4	4.1 4.1	5.2 5.3	1.3 1.4	6.0 5.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to $\overline{ERRA}$ or $\overline{ERRB}$	8	3.7 5.1	6.8 8.3	8.3 9.7	3.7 5.1	9.8 11.0	ns
t_{PLH} t_{PHL}	Propagation delay LEA to Bn or LEB to An	9	1.0 1.0	3.2 3.1	4.4 4.5	1.0 1.0	4.9 5.0	ns
t_{PLH} t_{PHL}	Propagation delay LEA to BPAR or LEB to APAR	9	2.0 1.7	6.8 6.3	8.3 7.9	2.0 1.7	9.7 9.0	ns
t_{PLH} t_{PHL}	Propagation delay LEA to $\overline{ERRA}$ or LEB to $\overline{ERRB}$	7	2.0 2.0	6.3 7.1	8.3 9.2	2.0 2.0	9.6 10.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	11, 12	1.0 1.0	3.0 3.4	4.3 4.8	1.0 1.0	5.1 5.4	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	11, 12	1.0 0.5	3.4 3.0	4.7 4.2	1.0 0.5	5.5 4.7	ns

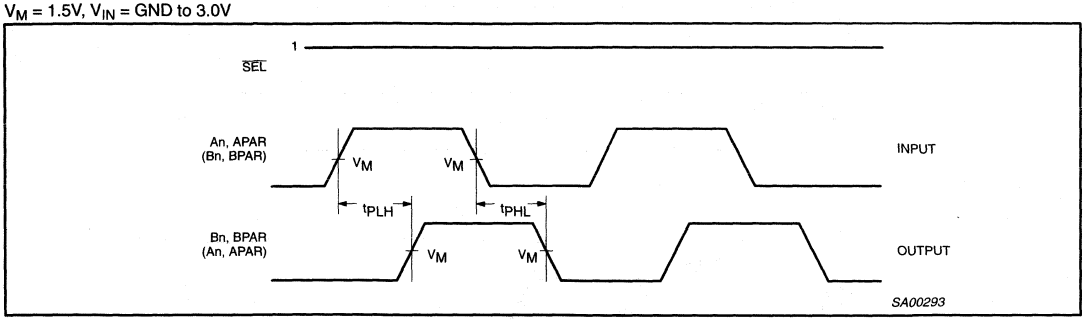
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

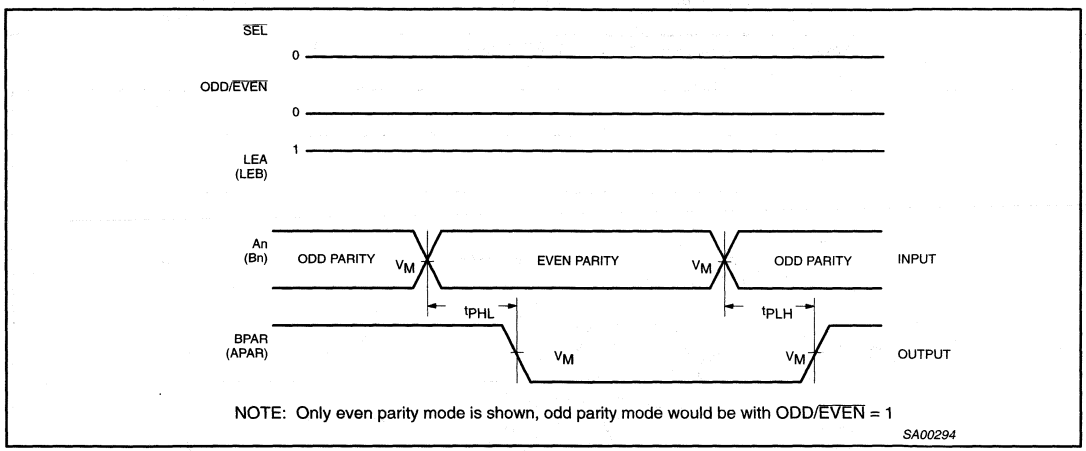
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	2.0 1.5	0.4 0.0		2.0 1.5		ns
t_h(H) t_h(L)	Hold time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	1.5 1.0	0.0 −0.2		1.5 1.0		ns
t_w(H)	Pulse width, High LEA or LEB	10	3.0	1.9		3.0		ns

AC WAVEFORMS

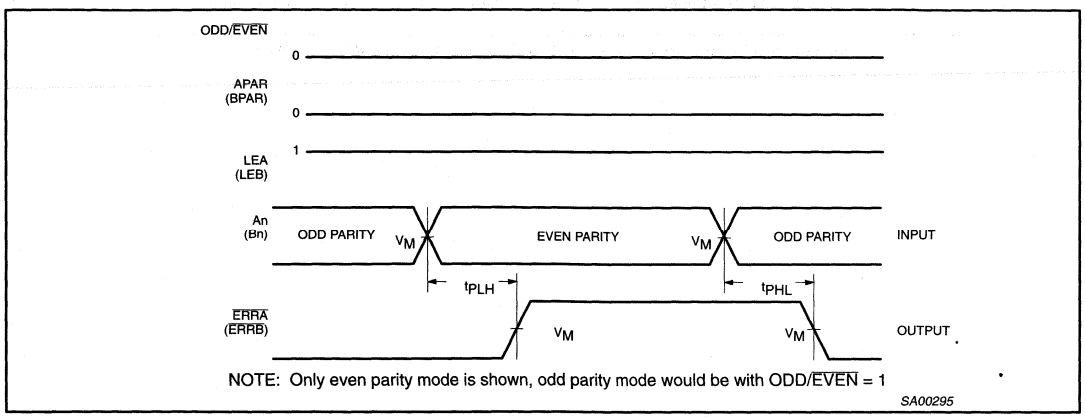
V_M = 1.5V, V_{IN} = GND to 3.0V



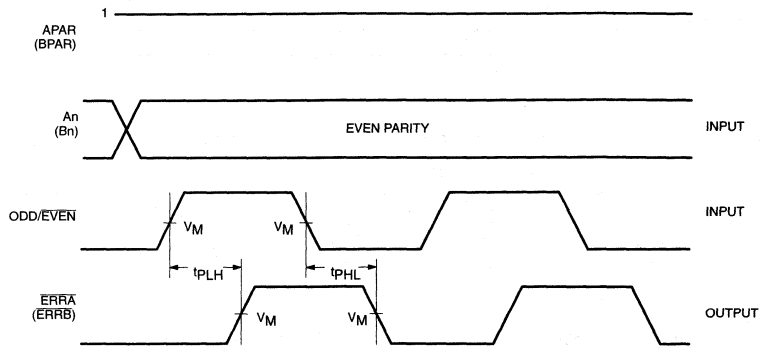
Waveform 1. Propagation Delay, An to Bn, Bn to An, APAR to BPAR, BPAR to APAR



Waveform 2. Propagation Delay, An to BPAR or Bn to APAR



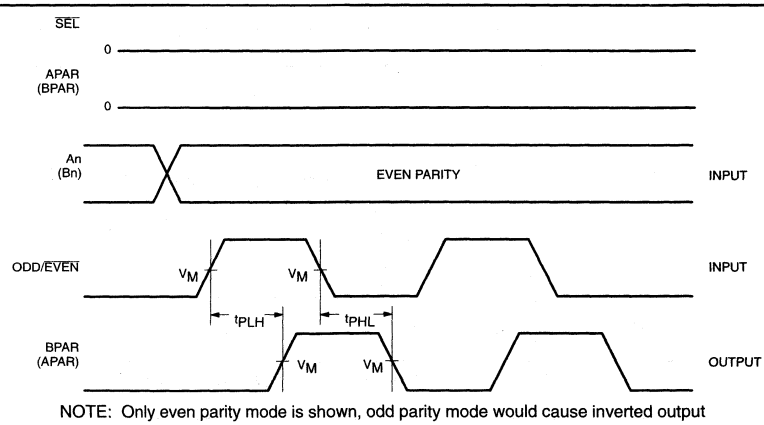
Waveform 3. Propagation Delay, An to ERRA or Bn to ERRB



NOTE: Only even parity mode is shown, odd parity mode would cause inverted output

SA00296

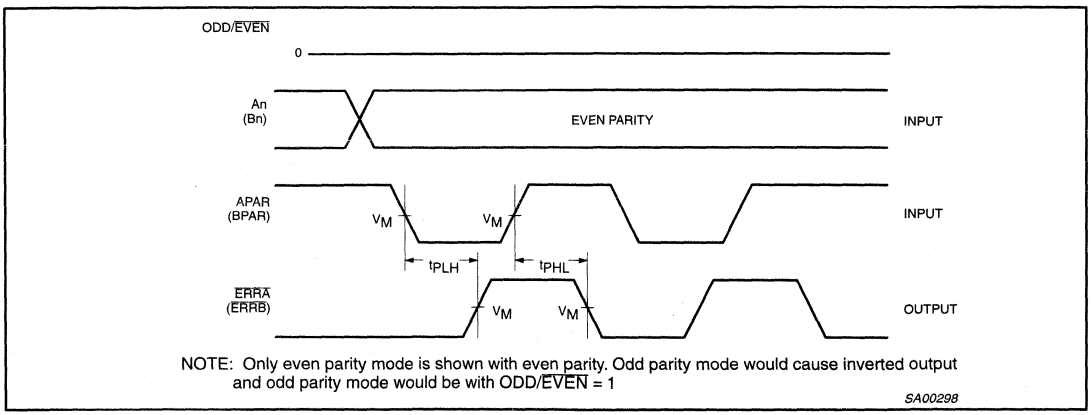
Waveform 4. Propagation Delay, ODD/EVEN to ERRA or ODD/EVEN to ERRB



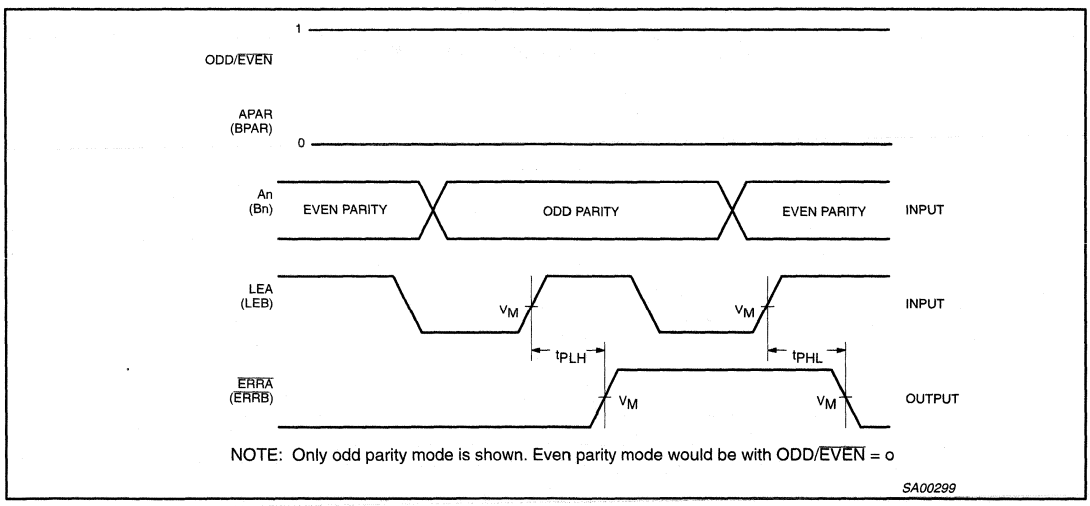
NOTE: Only even parity mode is shown, odd parity mode would cause inverted output

SA00297

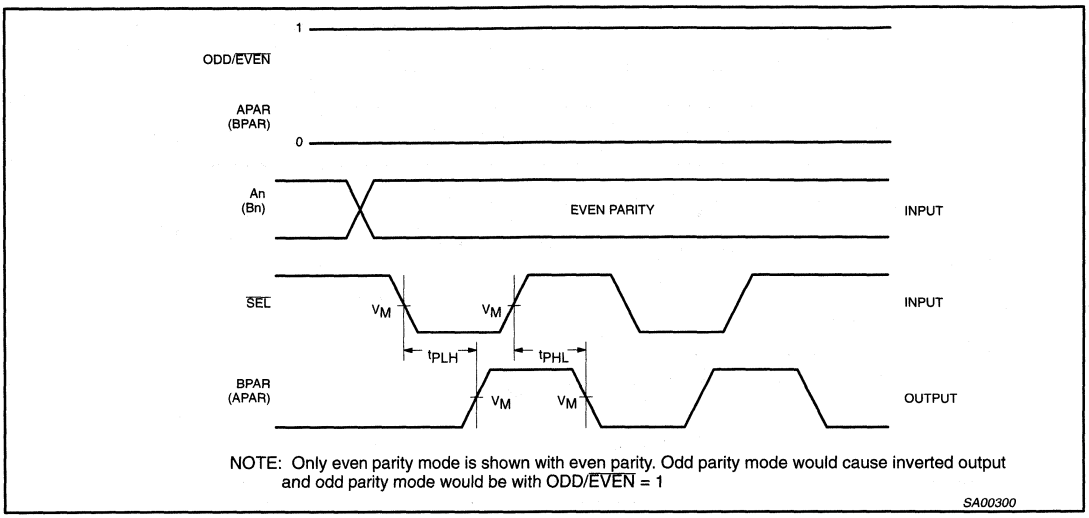
Waveform 5. Propagation Delay, ODD/EVEN to APAR or ODD/EVEN to BPAR



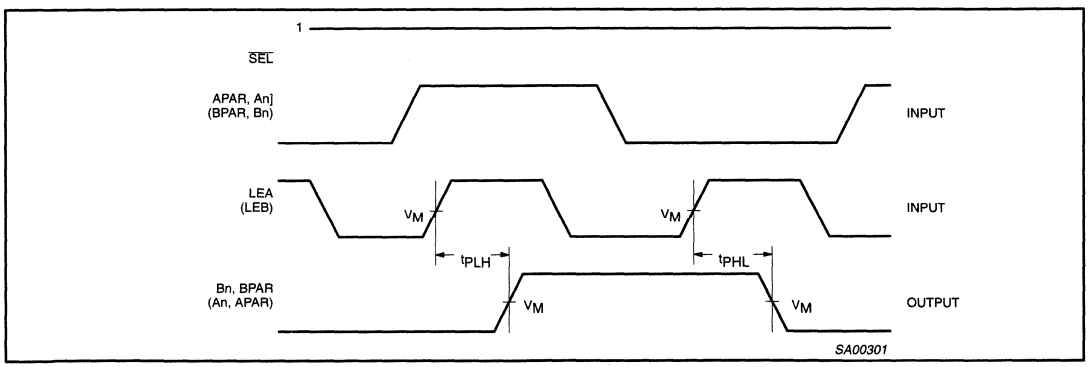
Waveform 6. Propagation Delay, APAR to ERRA or BPAR to ERRB



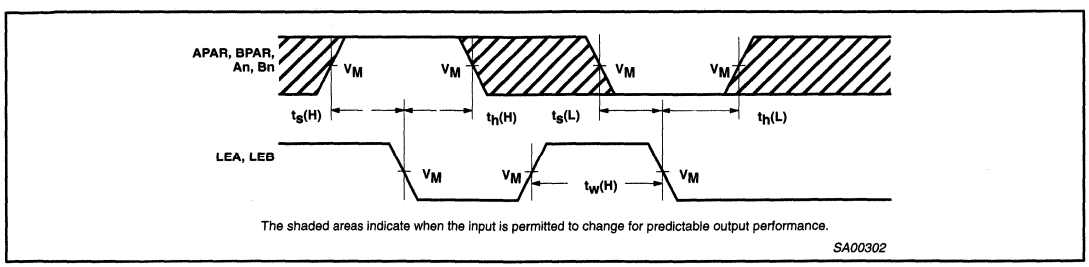
Waveform 7. Propagation Delay, LEA to ERRA or LEB to ERRB



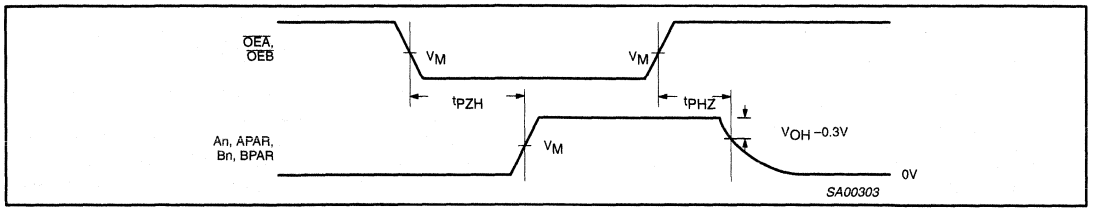
Waveform 8. Propagation Delay, $\overline{SEL}$ to BPAR or $\overline{SEL}$ to APAR



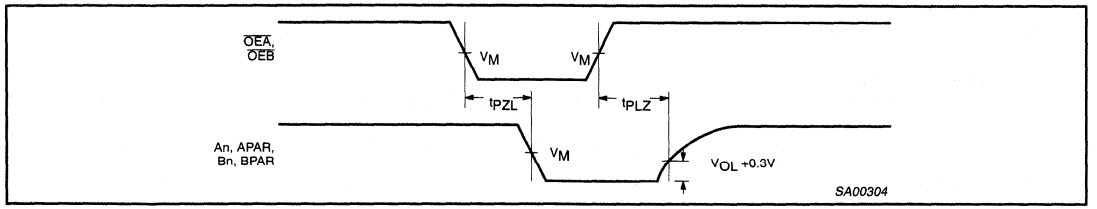
Waveform 9. Propagation Delay, LEA to BPAR or LEB to APAR, LEA to Bn or LEB to An



Waveform 10. Data Setup and Hold Times, Pulse Width High

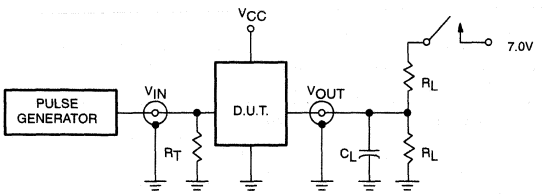


Waveform 11. 3-State Output Enable Time to High Level and Output Disable Time from High Level

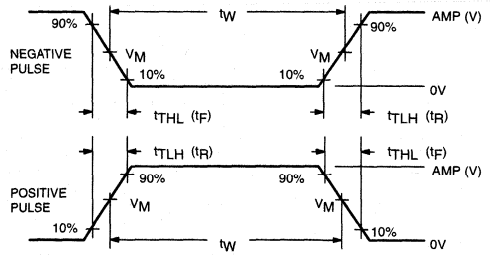


Waveform 12. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Octal registered transceiver (3-State) 74ABT2952

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT2952 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

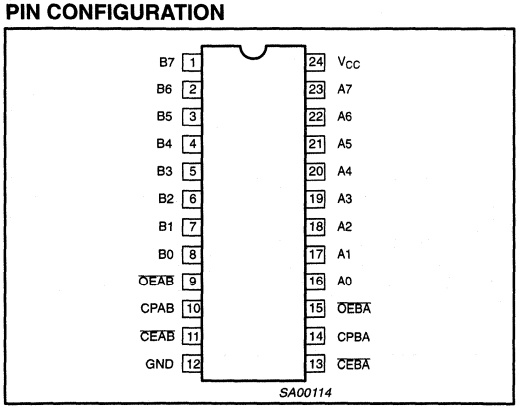
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50pF; V_{CC} = 5V	5.7	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	110	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT2952 N	74ABT2952 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT2952 D	74ABT2952 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT2952 DB	74ABT2952 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT2952 PW	7ABT2952PW DH	SOT355-1

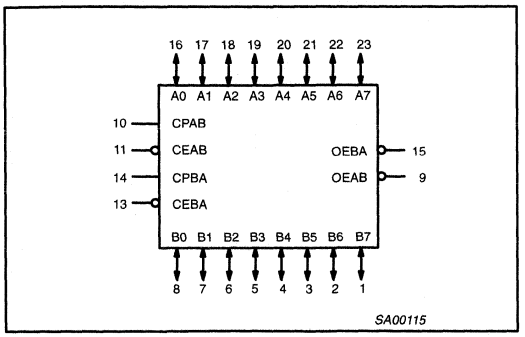
PIN CONFIGURATION



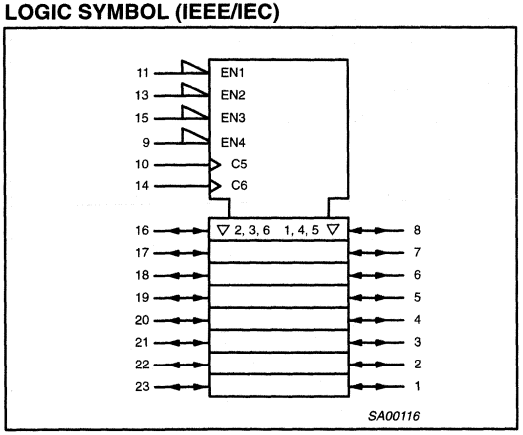
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
1, 2, 3, 4, 5, 6, 7, 8	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Output enable inputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low–to–High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OEXX}$			
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

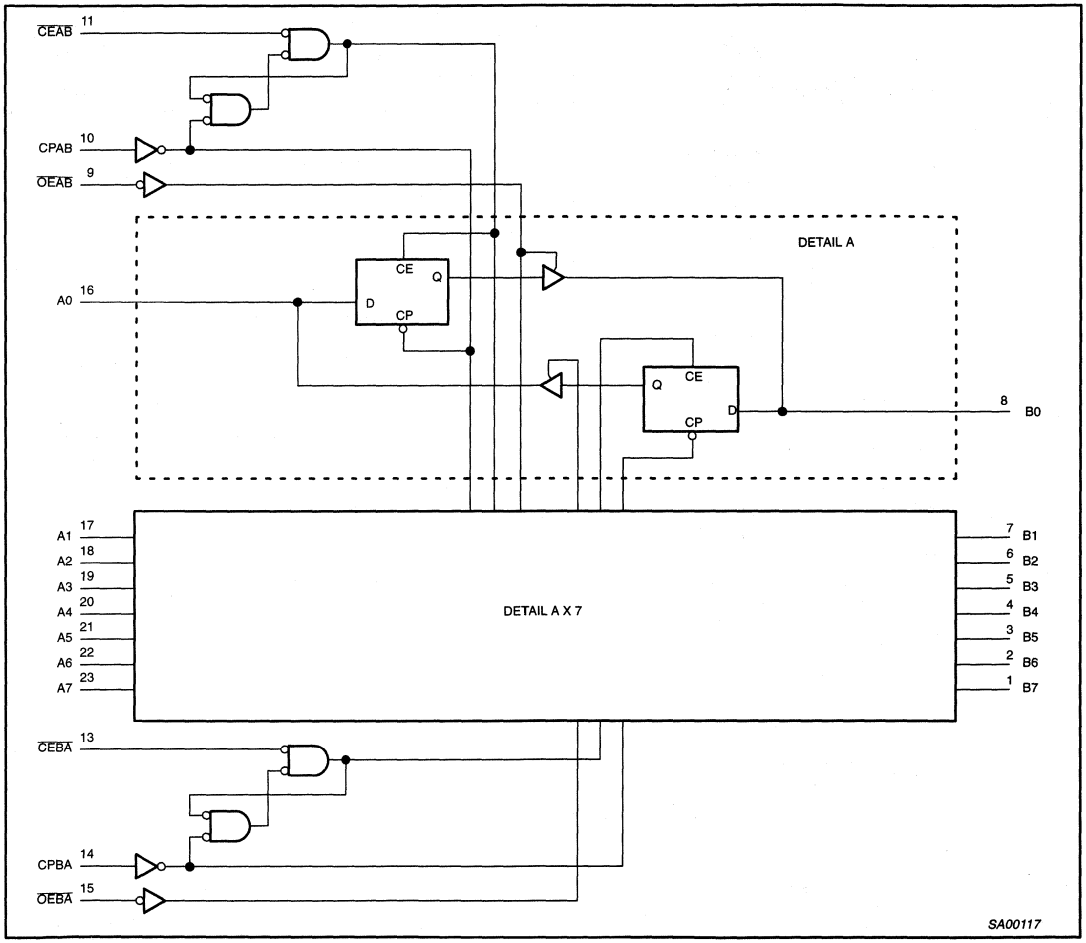
H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O = 4.5V; V_I = 0.0V or 5.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

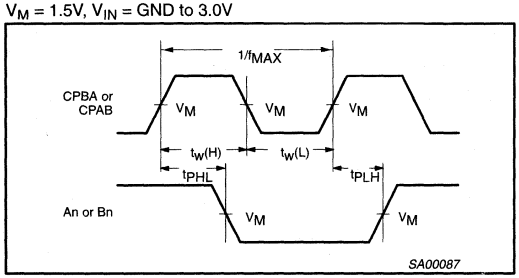
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	150	250		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	1	2.0 2.5	3.2 3.8	6.6 7.2	2.0 2.5	7.6 8.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	3 4	1.0 2.2	3.2 4.4	4.8 6.2	1.0 2.2	5.8 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	3 4	2.0 1.5	3.6 2.8	7.6 7.1	2.0 1.5	8.1 7.6	ns

AC SETUP REQUIREMENTS

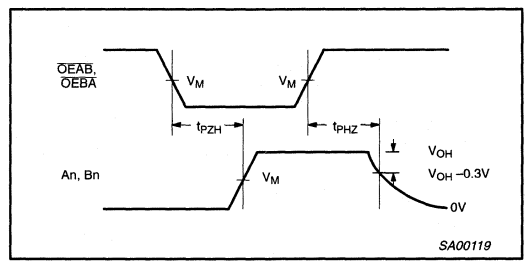
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_S(H)$ $t_s(L)$	Setup time An to CPAB or Bn to CPBA	2	4.5 3.5	2.2 1.6	4.5 3.5	ns
$t_h(H)$ $t_h(L)$	Hold time An to CPAB or Bn to CPBA	2	0.0 0.0	–0.8 –1.4	0.0 0.0	ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	2	4.0 3.0	0.8 0.8	4.0 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	2	0.0 0.0	–0.7 –0.7	0.0 0.0	ns
$t_w(H)$ $t_w(L)$	CPAB or CPBA pulse width, High or Low	1	3.0 3.5	0.8 0.9	3.0 3.5	ns

AC WAVEFORMS

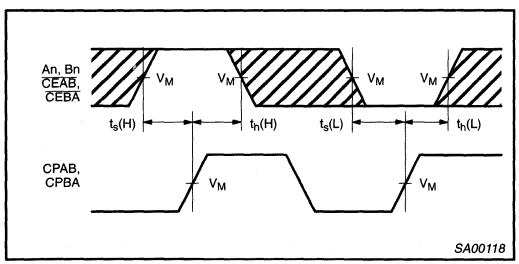
V_M = 1.5V, V_{IN} = GND to 3.0V



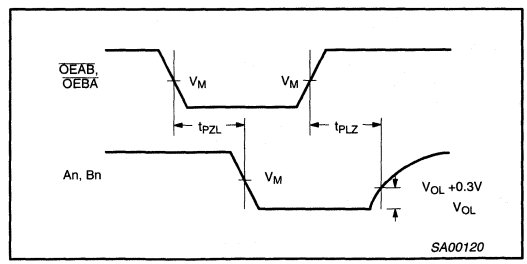
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

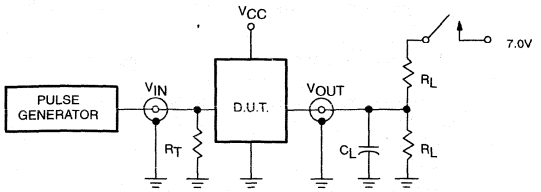


Waveform 2. Data Setup and Hold Times

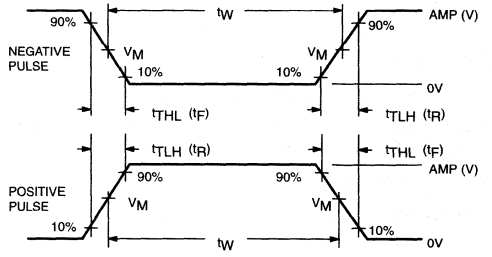


Waveform 4. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SA00012

Octal registered transceiver, inverting (3-State) 74ABT2953

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset

DESCRIPTION

The 74ABT2953 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT2953 device is an 8-bit registered inverting transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

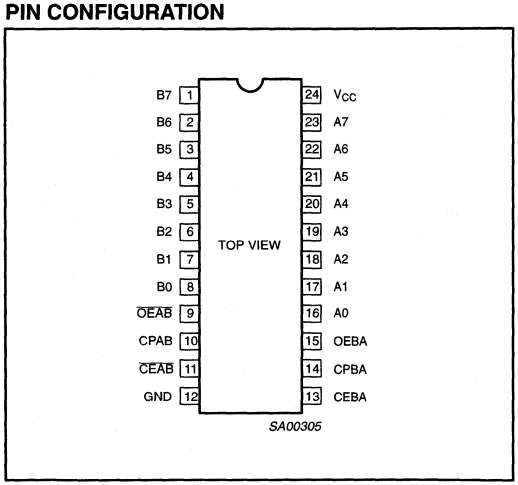
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to $\overline{An}$ or CPAB to $\overline{Bn}$	C_L = 50pF; V_{CC} = 5V	5.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT9253 N	74ABT2953 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT2953 D	74ABT2953 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT2953 DB	74ABT2953 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT2953 PW	7ABT2953PW DH	SOT355-1

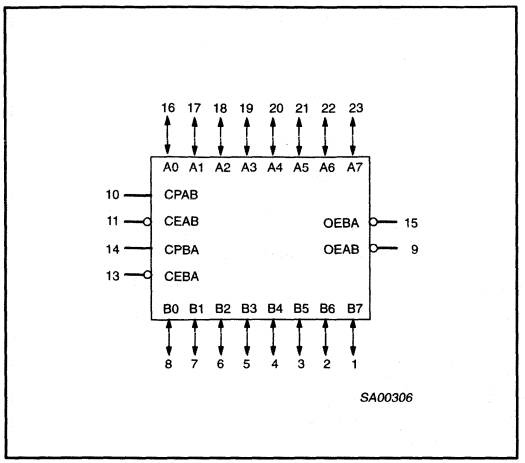
PIN CONFIGURATION



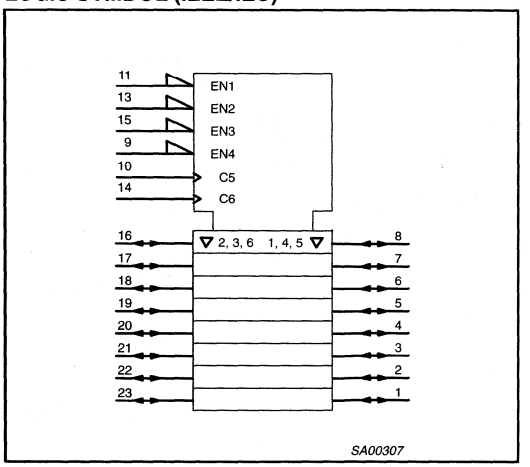
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
1, 2, 3, 4, 5, 6, 7, 8	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Output enable inputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL	OPERATING
An or Bn	CPXX	$\overline{CEXX}$	Q	MODE
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	An or Bn	OPERATING
$\overline{OEXX}$	Q	OUTPUTS	MODE
H	X	Z	Disable outputs
L L	L H	H L	Enable outputs

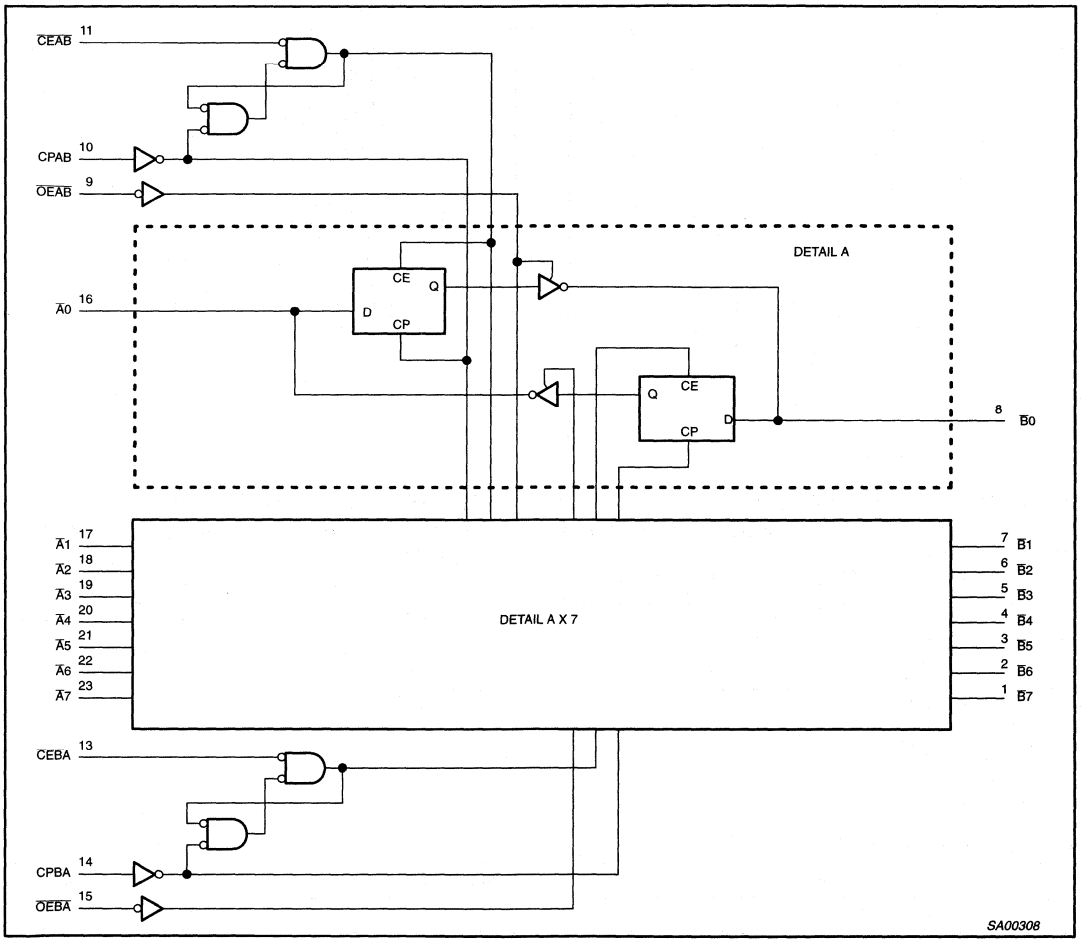
H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.2		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.7		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.3		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–65	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		110	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		110	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

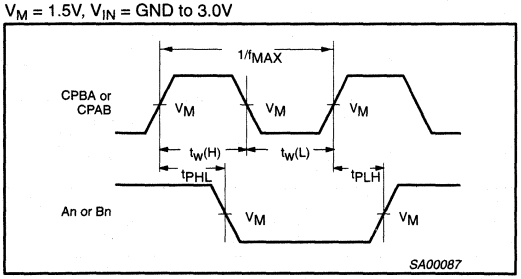
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	1	2.0 2.5	5.1 5.7	6.6 7.2	2.0 2.5	7.6 8.2	ns
t_{PZH} t_{PZL}	Output enable time OEBA to An, OEAB to Bn	3 4	1.0 2.2	4.0 5.3	4.8 6.2	1.0 2.2	5.8 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time OEBA to An, OEAB to Bn	3 4	2.0 1.5	6.1 5.6	7.6 7.1	2.0 1.5	8.1 7.6	ns

AC SETUP REQUIREMENTS

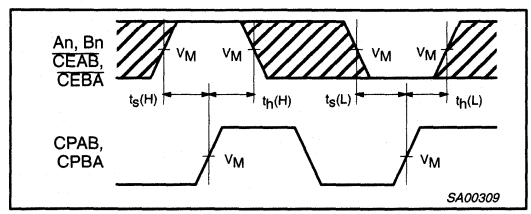
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_S(H)$ $t_s(L)$	Setup time An to CPAB or Bn to CPBA	2	4.0 3.0	2.5 1.1	4.0 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time An to CPAB or Bn to CPBA	2	0.0 0.0	−1.0 −2.0	0.0 0.0	ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	2	3.5 2.5	2.0 0.9	3.5 2.5	ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	2	0.0 0.0	−0.5 −1.0	0.0 0.0	ns
$t_w(H)$ $t_w(L)$	CPAB or CPBA pulse width, High or Low	1	3.0 3.5	2.0 1.1	3.0 3.5	ns

AC WAVEFORMS

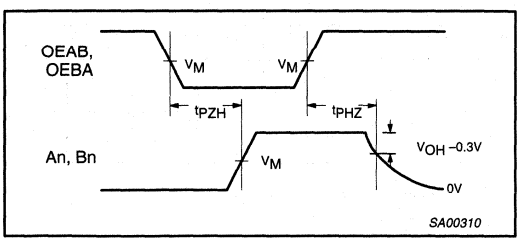
V_M = 1.5V, V_{IN} = GND to 3.0V



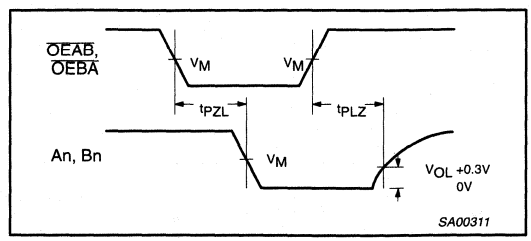
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

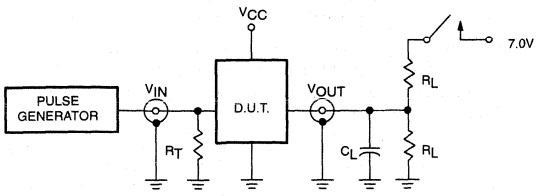


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

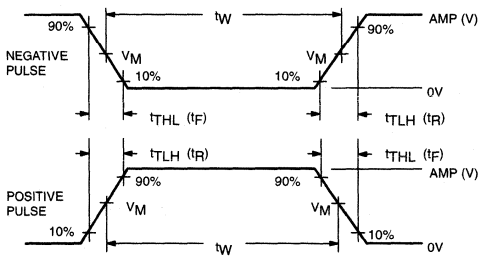


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

Synchronizing dual D-type flip-flop with metastable immune characteristics

74ABT5074

FEATURES

- Metastable immune characteristics
- Pin compatible with 74F74 and 74F5074
- Typical f_{MAX} = 200MHz
- Output skew guaranteed less than 2.0ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- Output capability: +20mA/–15mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT5074 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ($\overline{S}$Dn) and reset ($\overline{R}$Dn) are asynchronous active low inputs and operate independently of the clock (CPn) input. Data must be stable just one setup time prior to the low-to-high transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output.

The 74ABT5074 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74ABT5074 are:

$$\tau \cong 94\text{ps and } T_0 \cong 1.3 \times 10^7 \text{ sec}$$

where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

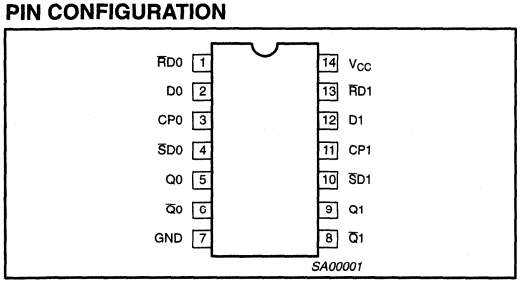
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Qn}$	C_L = 50pF; V_{CC} = 5V	2.8 2.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} =5.5V	2	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	–40°C to +85°C	74ABT5074 N	74ABT5074 N	SOT27-1
14-Pin plastic SO	–40°C to +85°C	74ABT5074 D	74ABT5074 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT5074 DB	74ABT5074 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT5074 PW	7ABT5074PW DH	SOT402-1

PIN CONFIGURATION



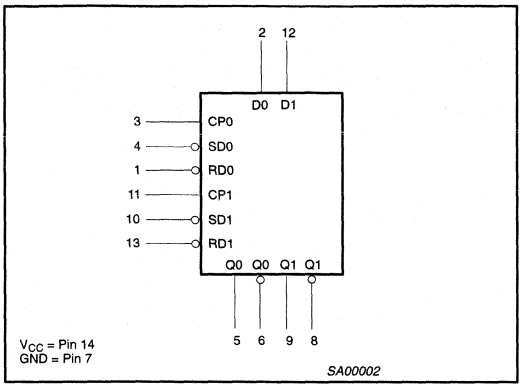
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 12	D0, D1	Data inputs
3, 11	CP0, CP1	Clock inputs (active rising edge)
4, 10	$\overline{S}$D0, $\overline{S}$D1	Set inputs (active-Low)
1, 13	$\overline{R}$D0, $\overline{R}$D1	Reset inputs (active-Low)
5, 9	Q0, Q1	Data outputs (active-Low), non-inverting
6, 8	$\overline{Q}$0, $\overline{Q}$1	Data outputs (active-Low), inverting
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

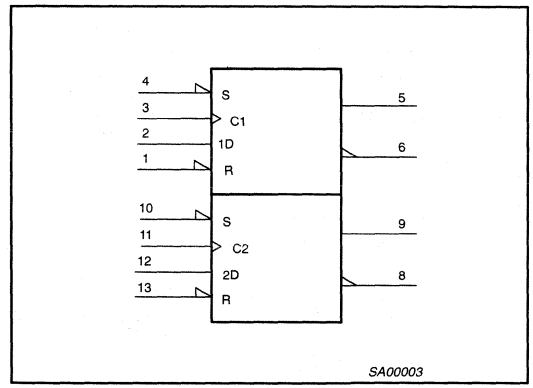
Synchronizing dual D-type flip-flop with metastable immune characteristics

74ABT5074

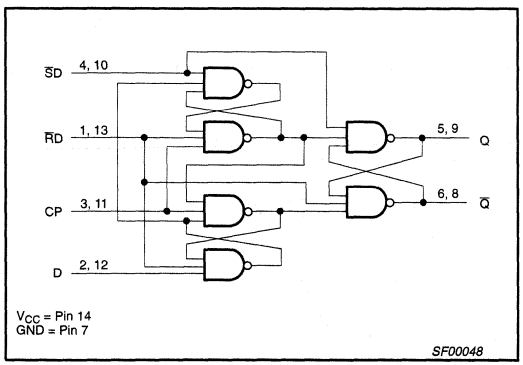
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	L	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↥	X	NC	NC	Hold

NOTES:

H = High voltage level
h = High voltage level one setup time prior to low-to-high clock transition
L = Low voltage level
l = Low voltage level one setup time prior to low-to-high clock transition
NC= No change from the previous setup
X = Don't care
↑ = Low-to-high clock transition
↥ = Not low-to-high clock transition
* = This setup is unstable and will change when either set or reset return to the high level

METASTABLE IMMUNE CHARACTERISTICS

Philips Semiconductors uses the term 'metastable immune' to describe characteristics of some of the products in its family. By running two independent signal generators (see Figure 1) at nearly the same frequency (in this case 10MHz clock and 10.02MHz data) the device-under-test can often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

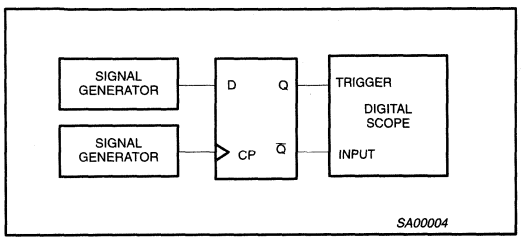


Figure 1. Test Setup

After determining the T_0 and τ of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74ABT5074 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74ABT5074 7 nanoseconds after the clock edge. He simply plugs his number into the following equation:

$$MTBF = e^{(t'/\tau)} / T_O * f_C * f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' > h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Figure 2 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.69×10^{10} seconds or about 535 years.

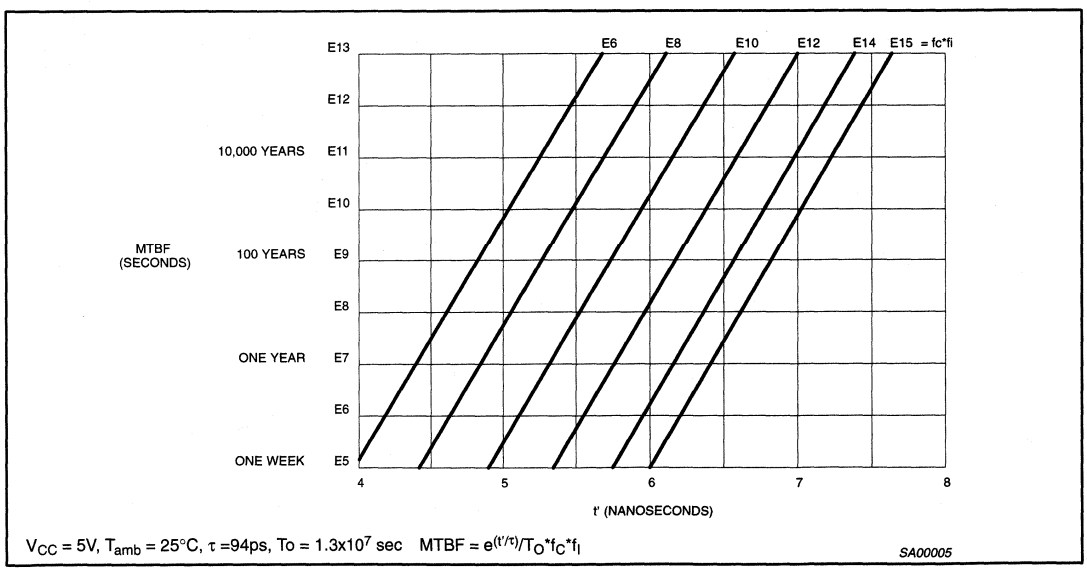


Figure 2. Mean Time Between Failures (MTBF) versus t'

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

V_{CC}	T_{amb} = –40°C		T_{amb} = 25°C		T_{amb} = 85°C	
	τ	T_0	τ	T_0	τ	T_0
5.5V	84ps	1.0×10^6 sec	93ps	3.8×10^6 sec	89ps	1.5×10^9 sec
5.0V	84ps	2.7×10^8 sec	94ps	1.3×10^7 sec	106ps	2.2×10^6 sec
4.5V	89ps	1.0×10^9 sec	103ps	2.1×10^7 sec	115ps	4.4×10^6 sec

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	40	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–75	–180	–50	–180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	1	180	250		150		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	1	1.0 1.0	2.8 2.4	3.9 3.5	1.0 1.0	4.5 3.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$Dn to Qn or $\overline{Q}$n	2	1.0 1.0	3.5 3.1	4.6 4.2	1.0 1.0	5.5 4.7	ns
$t_{sk(o)}$	Output skew[1, 2] CPn to Qn to $\overline{Q}$n	4			1.5		2.0	ns

NOTES:
1. I t_{PN} actual - t_{PM} actual I for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).

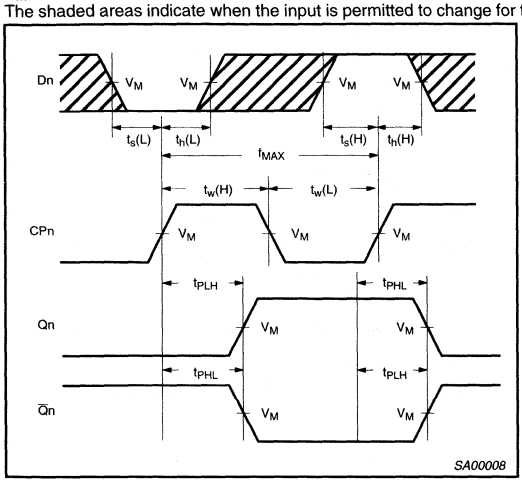
AC SETUP REQUIREMENTS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

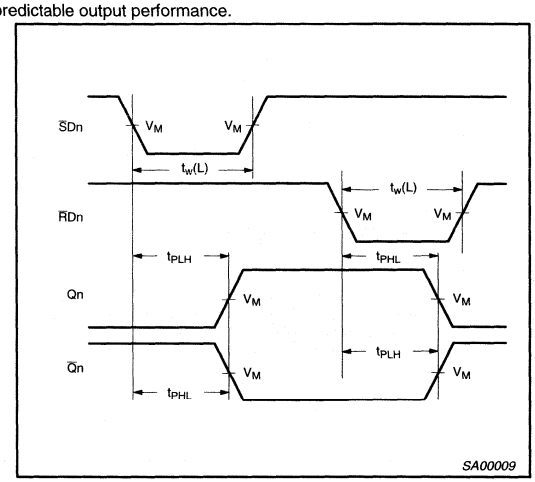
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C V_{CC} = +5.0V		T_{amb} = –40 to +85°C V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time, High or Low Dn to CPn	1	2.5 2.5	1.5 1.5	2.5 2.5	ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CPn	1	0 0	–1.4 –1.4	0 0	ns
t_w (H) t_w (L)	CPn pulse width, high or low	1	1.5 2.4	0.6 1.8	1.5 2.9	ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn pulse width, low	2	2.0	1.3	2.2	ns
t_{rec}	Recovery time $\overline{S}$Dn or $\overline{R}$Dn to CPn	3	2.4	1.3	2.8	ns

AC WAVEFORMS

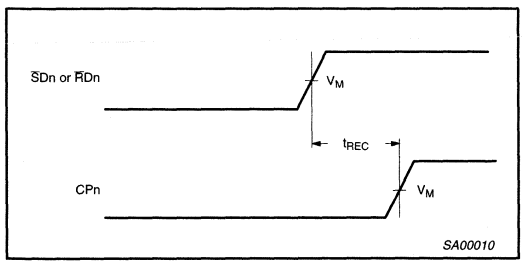
V_M = 1.5V, V_{IN} = GND to 3.0V
The shaded areas indicate when the input is permitted to change for the predictable output performance.



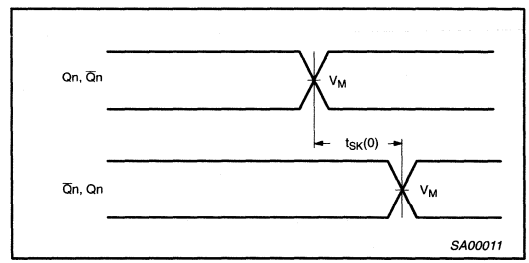
Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Time, and Clock Width



Waveform 2. Propagation Delay for Set and Reset to Output, Set and Reset Pulse Width

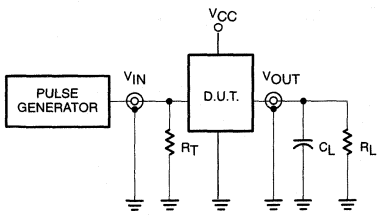


Waveform 3. Recovery Time for Set or Reset to Output

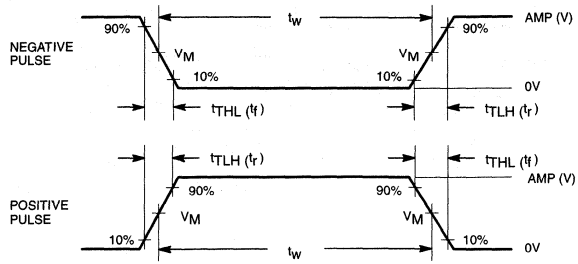


Waveform 4. Output Skew

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	amplitude	rep. rate	t_w	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00058

16-bit inverting buffer/driver (3-State)

74ABT16240A
74ABTH16240A

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16240A incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16240A is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed and high output drive.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

Two options are available, 74ABT16240A which does not have the bus hold feature and 74ABTH16240A which incorporates the bus hold feature.

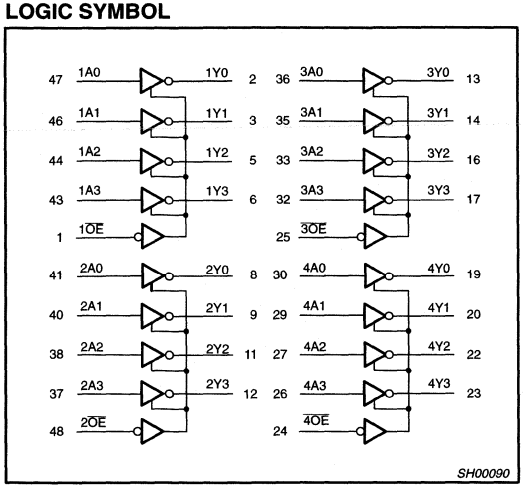
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} =	2.0 1.8	ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16240A DL	BT16240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16240A DGG	BT16240A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16240A DL	BH16240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16240A DGG	BH16240A DGG	SOT362-1

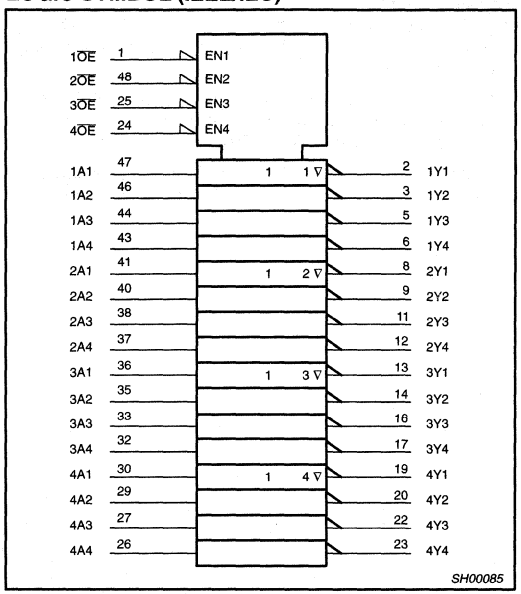
LOGIC SYMBOL



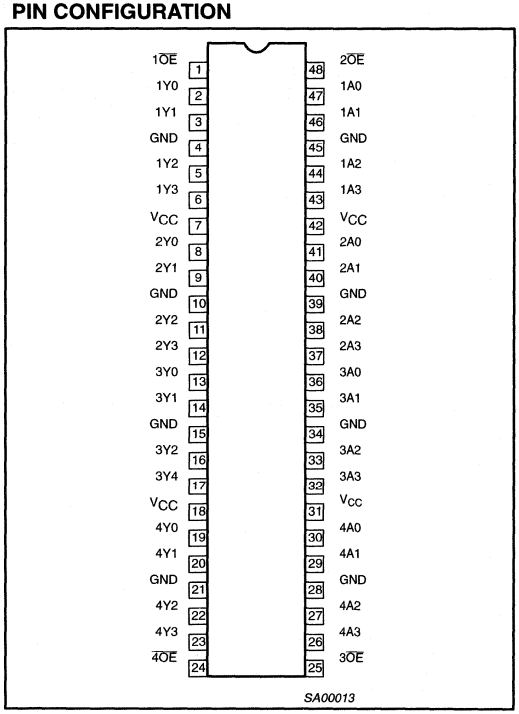
16-bit inverting buffer/driver (3-State)

74ABT16240A
74ABTH16240A

LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0-1$\overline{Y}$3 2$\overline{Y}$0-2$\overline{Y}$3 3$\overline{Y}$0-3$\overline{Y}$3 4$\overline{Y}$0-4$\overline{Y}$3	Data outputs
1, 48, 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Outputs
n$\overline{OE}$	nAx	n$\overline{Y}$x
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH16240A	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0			–2	–3		–5	µA
I_{HOLD}	Bus Hold current A inputs[4] 74ABTH168240A	V_{CC} = 4.5V; V_I = 0.8V		50			50		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1.0		1.0	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1.0		1.0	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16240A	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			10	200		200	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16240A	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			0.2	1.0		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This is the bus hold overdrive current required to force the input to the opposite logic state.

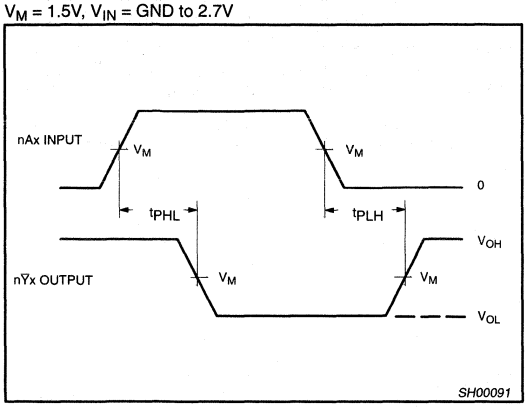
AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

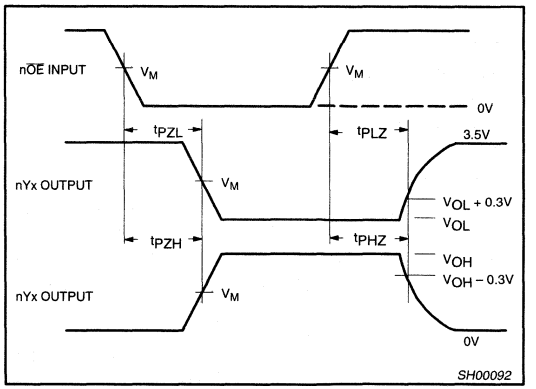
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1.0 1.0	2.0 1.5	3.0 3.0	1.0 1.0	3.7 3.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.2 1.2	2.4 2.3	3.3 3.2	1.2 1.0	4.2 4.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.3 1.3	2.7 2.5	4.1 3.6	1.6 1.4	4.7 4.1	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

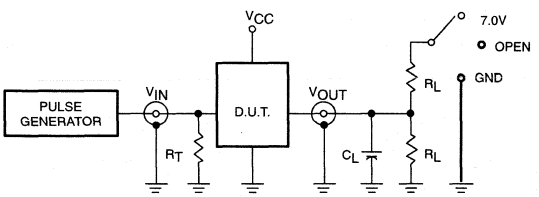


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

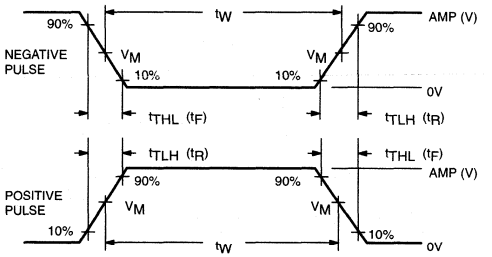


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	7V
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00093

16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

74ABT162240
74ABTH162240

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-32mA
- TTL input and output switching levels
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH162240 incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT162240 is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

Two options are available, 74ABT162240 which does not have the bus hold feature and 74ABTH162240 which incorporates the bus hold feature.

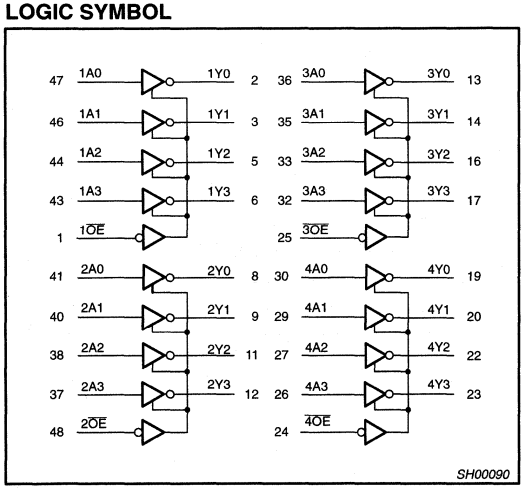
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} =	2.7 2.6	ns
C_{IN}	Input capacitance $n\overline{OE}$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT162240 DL	BT162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT162240 DGG	BT162240 DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH162240 DL	BH162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH162240 DGG	BH162240 DGG	SOT362-1

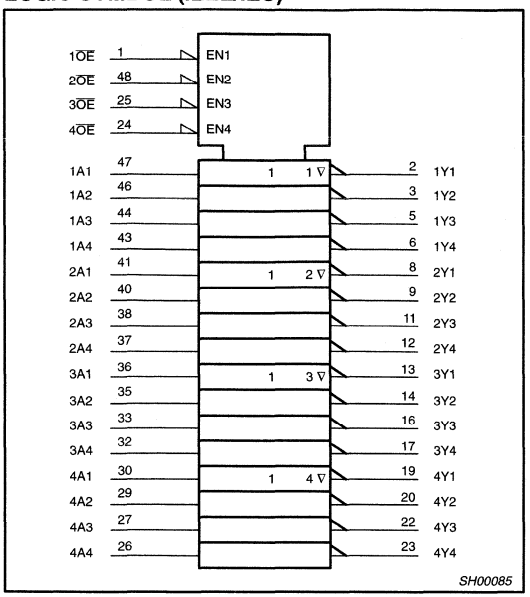
LOGIC SYMBOL



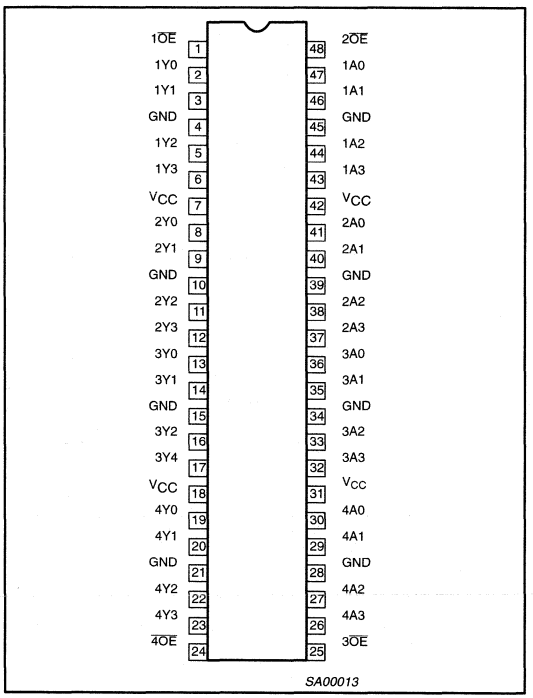
16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

74ABT162240
74ABTH162240

LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION

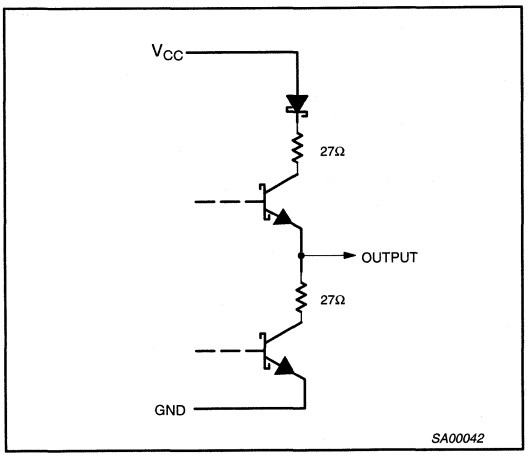


FUNCTION TABLE

Inputs		Outputs
$n\overline{OE}$	nAx	$n\overline{Y}x$
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

SCHEMATIC OF Y OUTPUTS



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	$1\overline{Y}0$-$1\overline{Y}3$ $2\overline{Y}0$-$2\overline{Y}3$ $3\overline{Y}0$-$3\overline{Y}3$ $4\overline{Y}0$-$4\overline{Y}3$	Data outputs
1, 48, 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		12	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 8mA; V_I = V_{IL} or V_{IH}				0.65		0.65	V
		V_{CC} = 4.5V; I_{OL} = 12mA; V_I = V_{IL} or V_{IH}				0.80		0.80	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH162240	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0			−2	−3		−5	µA
I_{HOLD}	Bus Hold current A inputs[3] 74ABTH162240	V_{CC} = 4.5V; V_I = 0.8V		50			50		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			−1.0	−10		−10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−70	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1.0		1.0	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1.0		1.0	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT162240	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			10	200		200	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH162240	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			0.2	1.0		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This is the bus hold overdrive current required to force the input to the opposite logic state.

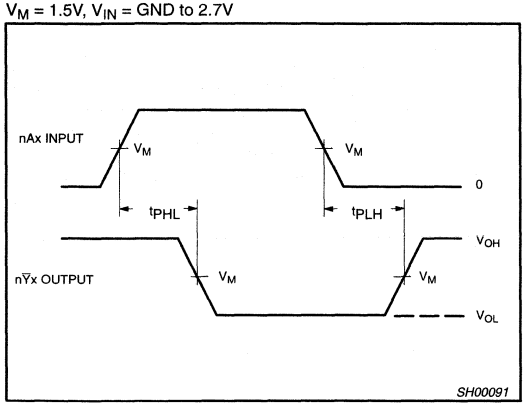
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

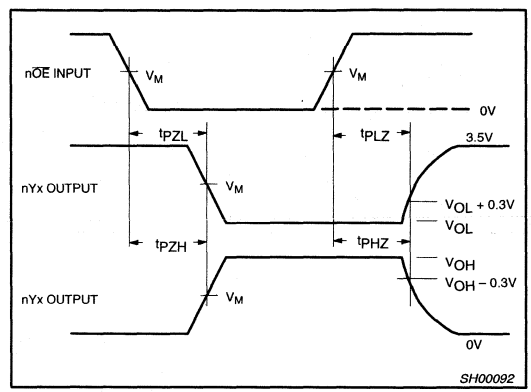
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{amb} = +25°C$ $V_{CC} = +5.0V$			$T_{amb} = -40°C$ to $+85°C$ $V_{CC} = +5.0V \pm 0.5V$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1.0 1.0	2.7 2.6	3.8 3.2	1.0 1.0	4.2 3.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.2 1.0	2.3 2.9	3.2 3.8	1.2 1.0	4.0 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.6 1.4	3.0 2.8	4.1 3.8	1.6 1.4	4.7 4.0	ns

AC WAVEFORMS

$V_M = 1.5$V, V_{IN} = GND to 2.7V

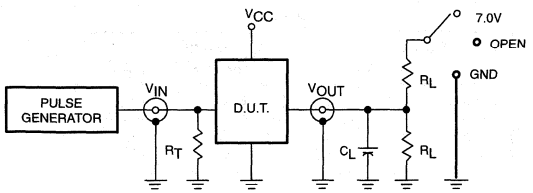


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

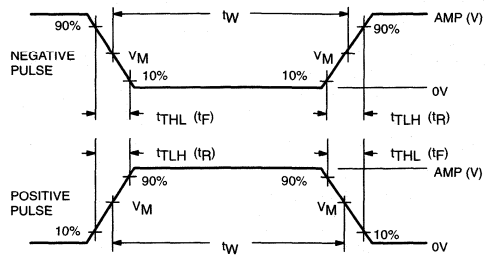


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	7V
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00093

16-bit buffer/driver (3-State)

74ABT16241A
74ABTH16241A

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16241A incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16241A is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed and high output drive.

This device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, 2OE, 3OE, $4\overline{OE}$), each controlling four of the 3-State outputs.

Two options are available, 74ABT16241A which does not have the bus hold feature and 74ABTH16241A which incorporates the bus hold feature.

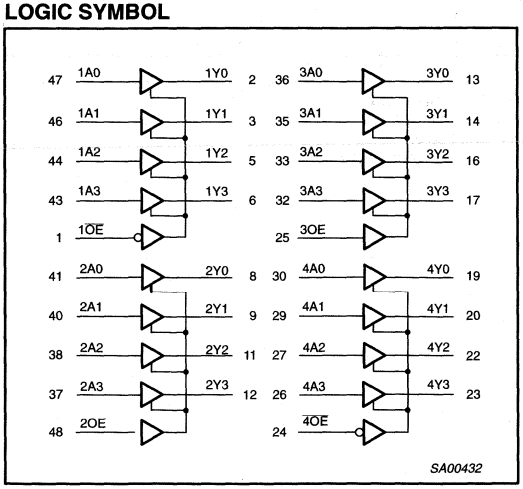
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nȲx	C_L = 50pF; V_{CC} =	1.8 1.6	ns
C_{IN}	Input capacitance $n\overline{OE}$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

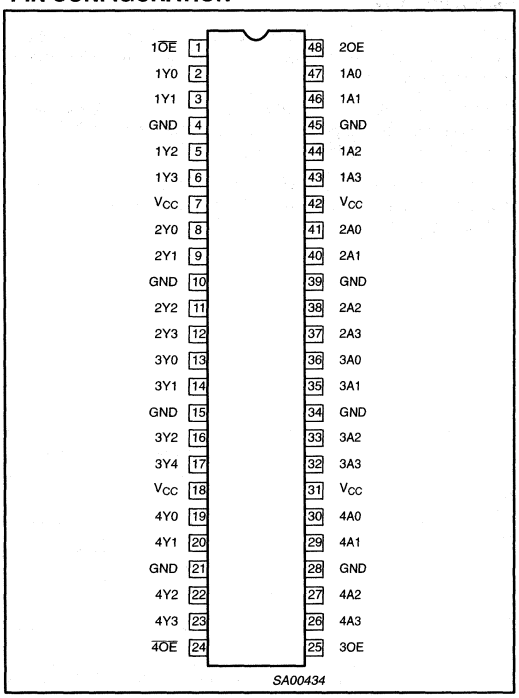
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16241A DL	BT16241A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16241A DGG	BT16241A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16241A DL	BH16241A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16241A DGG	BH16241A DGG	SOT362-1

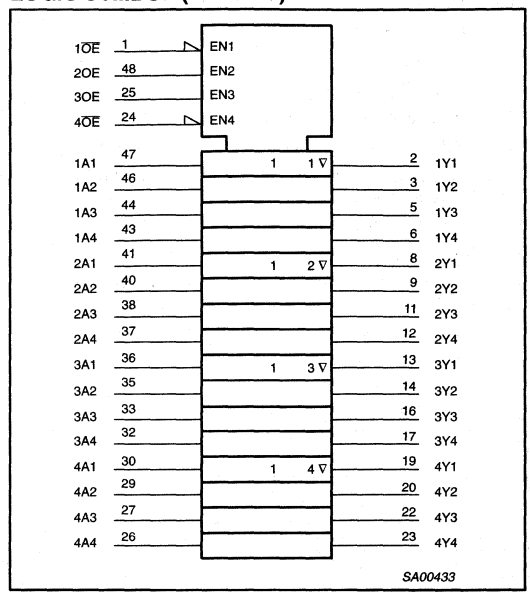
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Y0-1Y3 2Y0-2Y3 3Y0-3Y3 4Y0-4Y3	Data outputs
1, 48, 25, 24	$1\overline{OE}$, 2OE, 3OE, $4\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Outputs
$1\overline{OE}$, $4\overline{OE}$	1An, 4An	1Yn, 4Yn
L	L	L
L	H	H
H	X	Z
2OE, 3OE	2An, 3An	2Yn, 3Yn
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH16241A	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0			–2	–3		–5	µA
I_{HOLD}	Bus Hold current A inputs[4] 74ABTH16241A	V_{CC} = 4.5V; V_I = 0.8V		75			75		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1.0		1.0	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1.0		1.0	mA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			10	200		200	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This is the bus hold overdrive current required to force the input to the opposite logic state.

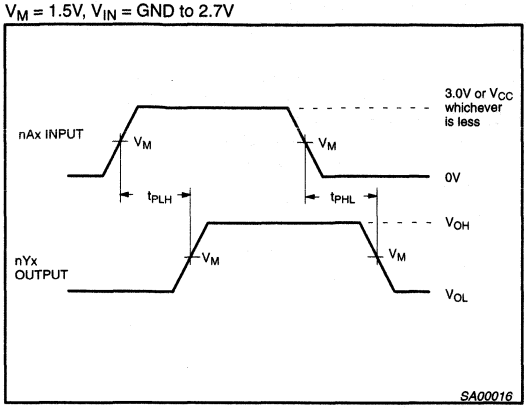
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

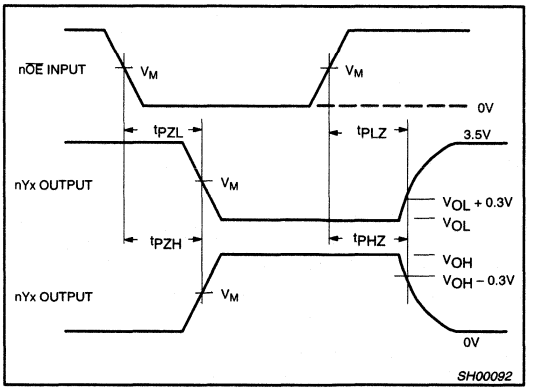
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1.0 1.0	1.8 1.6	2.6 2.4	1.0 1.0	3.1 2.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.4 2.6	3.4 4.6	1.0 1.0	3.9 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.3 1.3	3.0 2.4	4.3 3.6	1.0 1.0	5.3 4.2	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

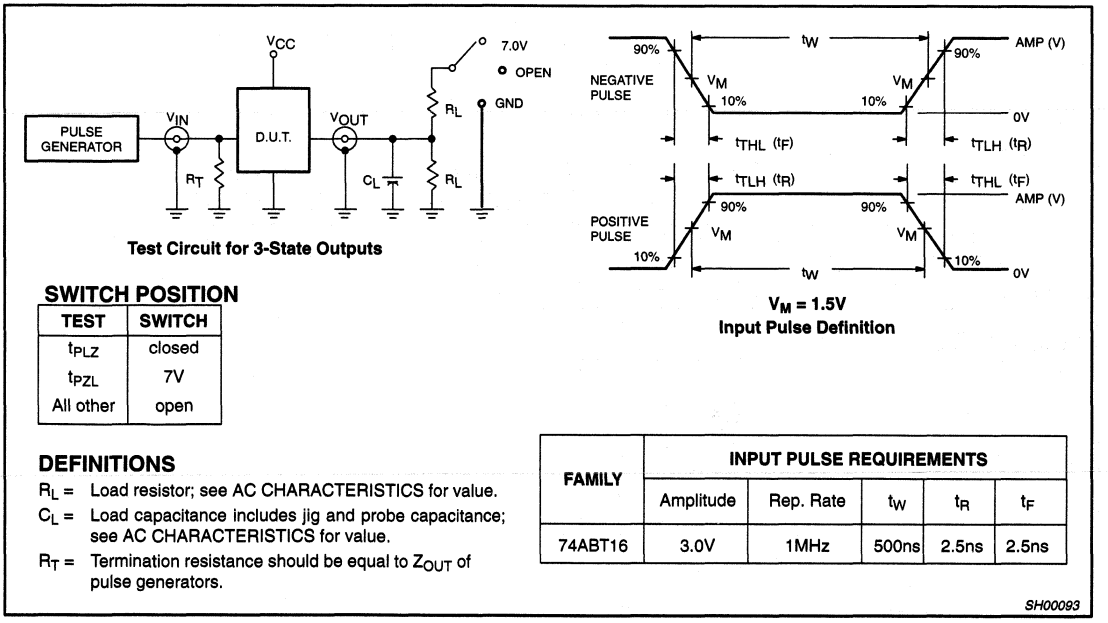


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	7V
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00093

16-bit buffer/line driver (3-State)

74ABT16244A
74ABTH16244A

FEATURES

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- 3-State buffers
- Output capability: +64 mA/–32mA
- Live insertion/extraction permitted
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- 74ABTH16244A incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT16244A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16244A device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.
Two options are available, 74ABT16244A which does not have the bus hold feature and 74ABTH16244A which incorporates the bus hold feature.

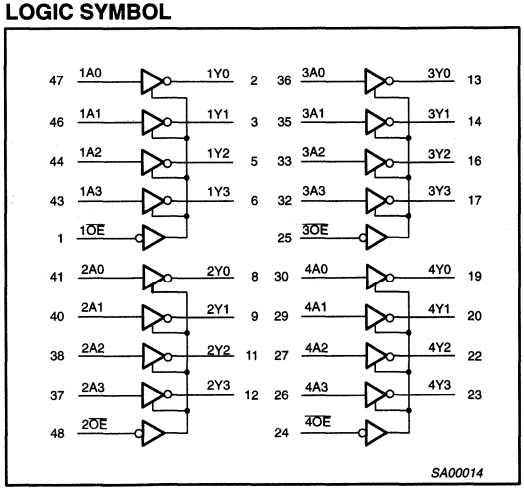
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	1.7 2.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	450	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	10	mA

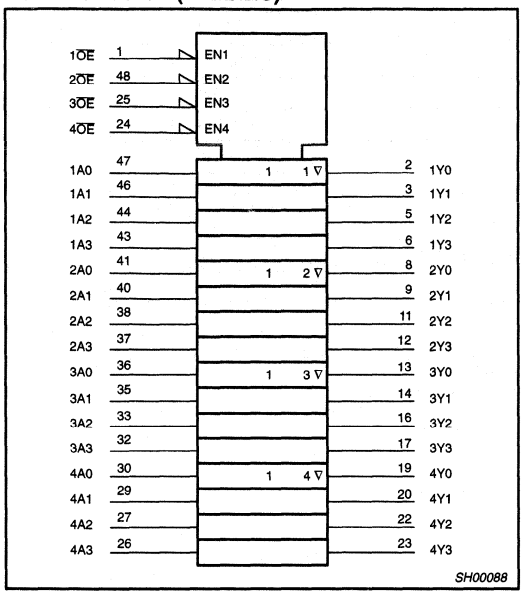
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16244A DL	BT16244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16244A DGG	BT16244A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABH16244A DL	BH16244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABH16244A DGG	BH16244A DGG	SOT362-1

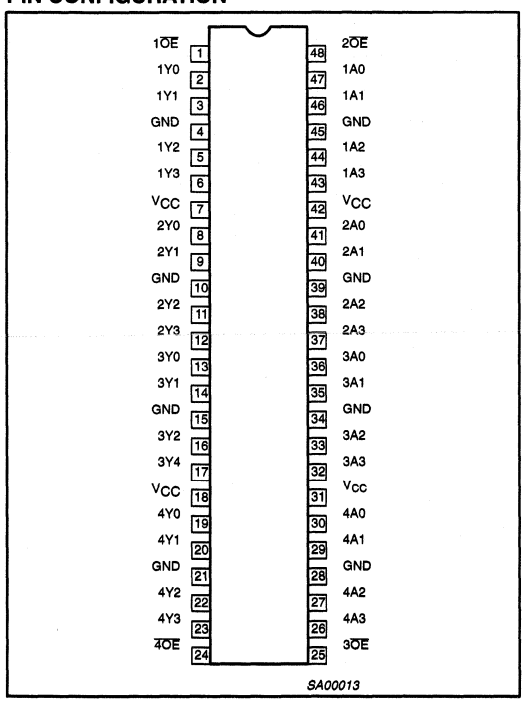
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 – 1Y3, 2Y0 – 2Y3, 3Y0 – 3Y3, 4Y0 – 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH16244A	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data Pins		0.01	1		1	
		V_{CC} = 5.5V; V_I = 0			−2	−3		−5	
I_{HOLD}	Bus Hold current A inputs[4] 74ABTH16244A	V_{CC} = 4.5V; V_I = 0.8V		50			50		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}			0.1	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}			−0.1	−10		−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−100	−180	−50	−180	mA
I_{CCH}	Quiescent supply current[3]	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.45	1.0		1.0	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			10	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.45	1.0		1.0	µA
ΔI_{CC}	Additional supply current per input pin[2, 3]	Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			100	250		250	µA
		Outputs disabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			100	250		250	
		Control pins, outputs disabled, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			100	250		250	

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This data sheet limit may vary among suppliers.
4. This is the bus hold overdrive current required to force the input to the opposite logic state.

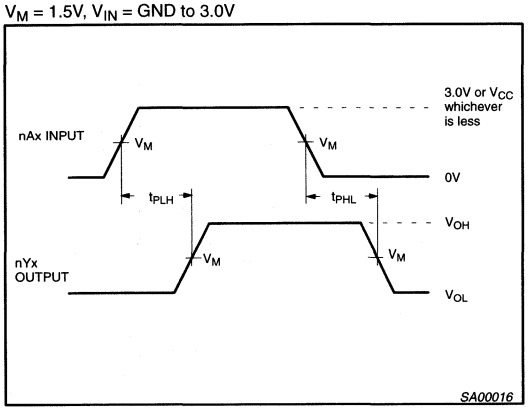
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

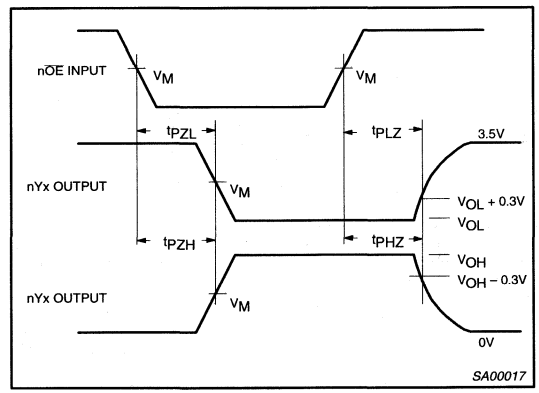
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.1 1.3	1.7 2.1	2.6 2.9	1.1 1.3	2.8 3.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.6 2.3	2.7 3.5	3.7 4.0	1.6 2.3	4.5 4.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.0 1.6	3.0 2.4	4.0 3.2	2.0 1.6	4.6 4.1	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

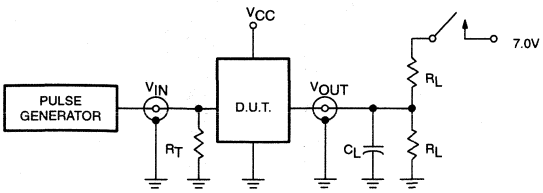


Waveform 1. Input (An) to Output (Yn) Propagation Delays

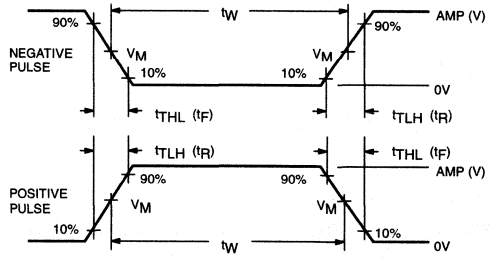


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

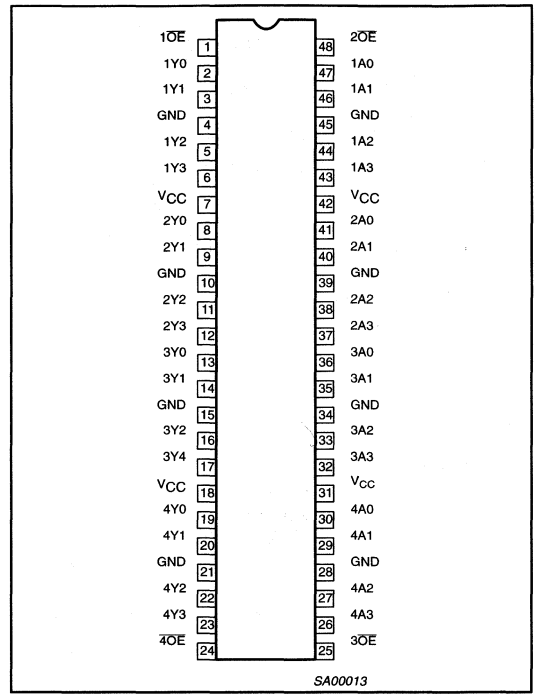
16-bit buffer/line driver with 30Ω series termination resistors (3-State)

74ABT162244
74ABTH162244

FEATURES

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- 3-State buffers
- Output capability: +12 mA/–32mA
- Live insertion/extraction permitted
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Same part as 74ABT16244-1
- 74ABTH162244 incorporates bus hold data inputs which eliminate the need for external pull–up resistors to hold unused inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

PIN CONFIGURATION



DESCRIPTION

The 74ABT162244 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT162244 device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

The 74ABT162244 is designed with 30Ω series resistance in both the upper and lower output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

The 74ABT162244 is the same as the 74ABT16244-1. The part number has been changed to reflect industry standards.

Two options are available, 74ABT162244 which does not have the bus hold feature and the 74ABTH162244 which incorporates the bus hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	1.8 3.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs Low; V_{CC} = 5.5V	10	mA

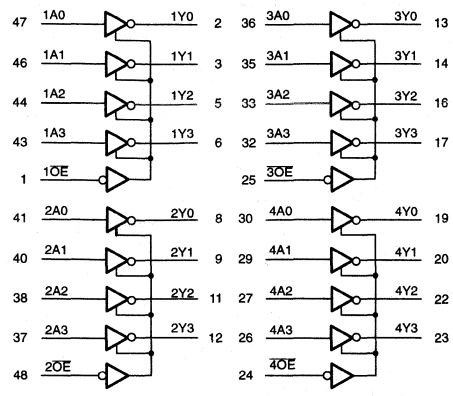
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT162244 DL	BT162244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT162244 DGG	BT162244 DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH162244 DL	BH162244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH162244 DGG	BH162244 DGG	SOT362-1

16-bit buffer/line driver with 30Ω series termination resistors (3-State)

74ABT162244
74ABTH162244

LOGIC SYMBOL

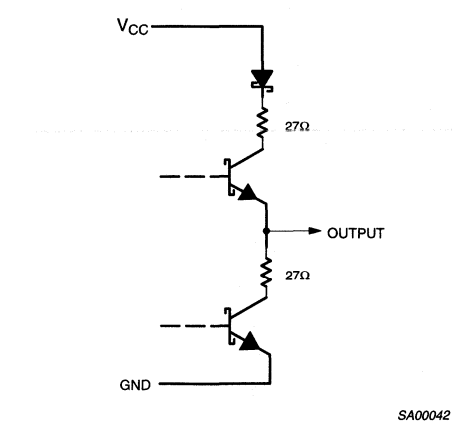


FUNCTION TABLE

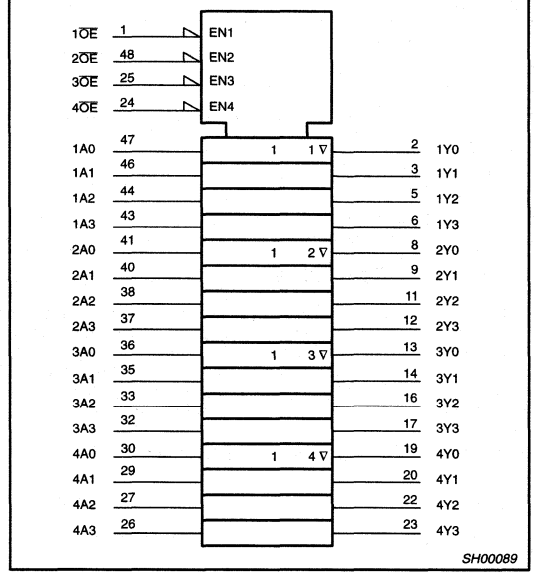
INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

SCHEMATIC OF Y OUTPUTS



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 – 1Y3, 2Y0 – 2Y3, 3Y0 – 3Y3, 4Y0 – 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage[3]	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 8mA; V_I = V_{IL} or V_{IH}				0.65		0.65	V
		V_{CC} = 4.5V; I_{OL} = 12mA; V_I = V_{IL} or V_{IH}				0.80		0.80	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH162244	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1.0		±1.0	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1.0		1.0	µA
		V_{CC} = 5.5V; V_I = 0			−2.0	−3.0		−5.0	µA
I_{HOLD}	Bus Hold Current A Inputs[4] 74ABTH162244	V_{CC} = 4.5V; V_I = 0.8V		50			50		µA
		V_{CC} = 5.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}			0.1	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}			−0.1	−10		−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−100	−180	−50	−180	mA
I_{CCH}	Quiescent supply current[3]	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.50	1.0		1.0	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			10	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.50	1.0		1.0	mA
ΔI_{CC}	Additional supply current per input pin[2, 3]	Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			100	250		250	µA
		Outputs disabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			100	250		250	µA
		Control pins, outputs disabled, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			100	250		250	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This data sheet limit may vary among suppliers.
4. This is the bus hold overdrive current required to force the input to the opposite logic state.

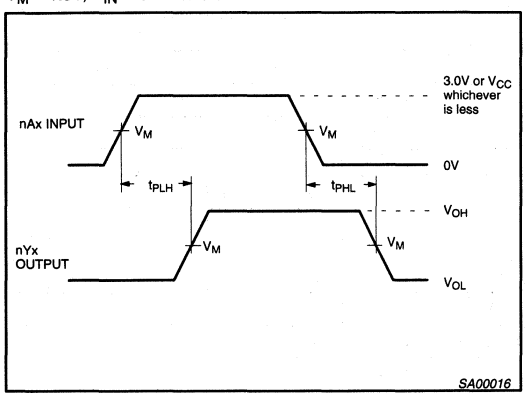
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

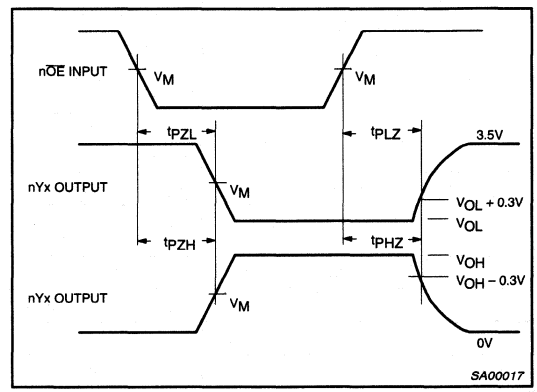
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.6	1.8 3.2	2.4 4.0	1.0 1.6	2.7 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.2 2.6	2.7 5.0	3.5 6.2	1.2 2.6	4.3 7.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.3	3.0 2.6	3.8 3.3	1.5 1.3	4.5 4.6	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

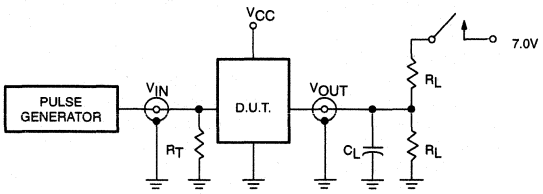


Waveform 1. Input (An) to Output (Yn) Propagation Delays

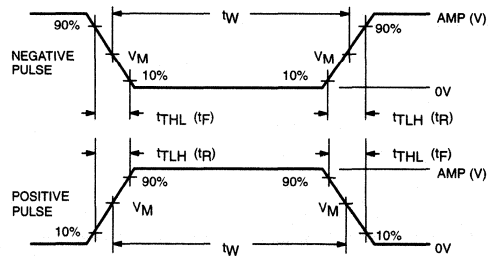


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

16-bit bus transceiver (3-State)

74ABT16245B
74ABTH16245B

FEATURES

- 16-bit bidirectional bus interface
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64 mA/–32mA
- Latch–up protection exceeds 500mA per JEDEC Std 17
- Live insertion/extraction permitted
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200V per Machine Model
- 74ABTH16245B incorporates bus hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT16245B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16245B device is a dual octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable ($1\overline{OE}$, $2\overline{OE}$) inputs for easy cascading and two Direction (1DIR, 2DIR) inputs for direction control.

Two options are available, 74ABT16245B which does not have the bus hold feature and the 74ABTH16245B which incorporates the bus hold feature.

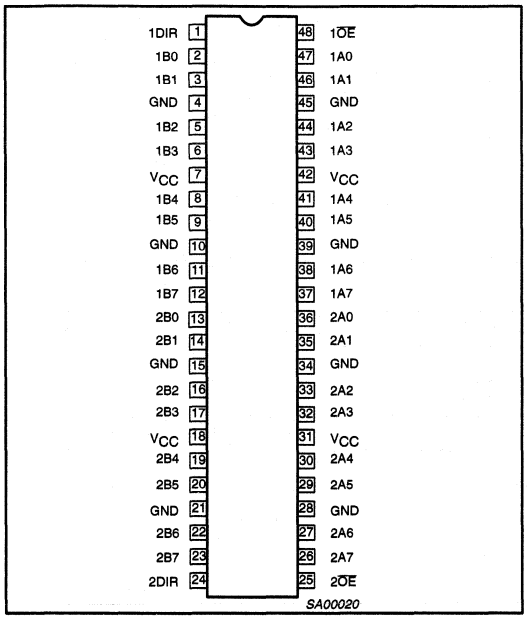
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 5V	2.0 2.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =5.5V	500	µA
I_{CCL}		Output Low; V_{CC} =5.5V	10	mA

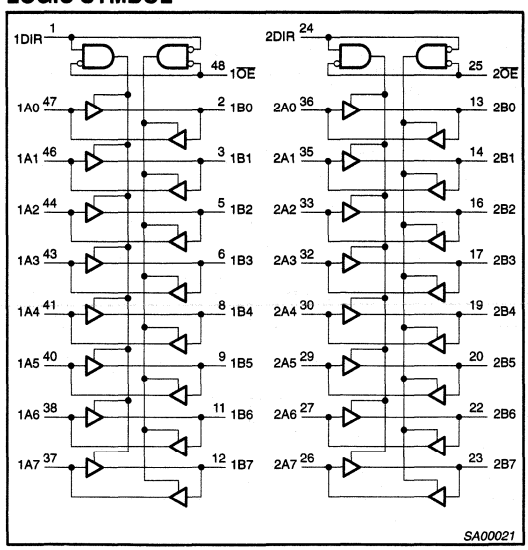
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16245B DL	BT16245B DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16245B DGG	BT16245B DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16245B DL	BH16245B DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16245B DGG	BH16245B DGG	SOT362-1

PIN CONFIGURATION



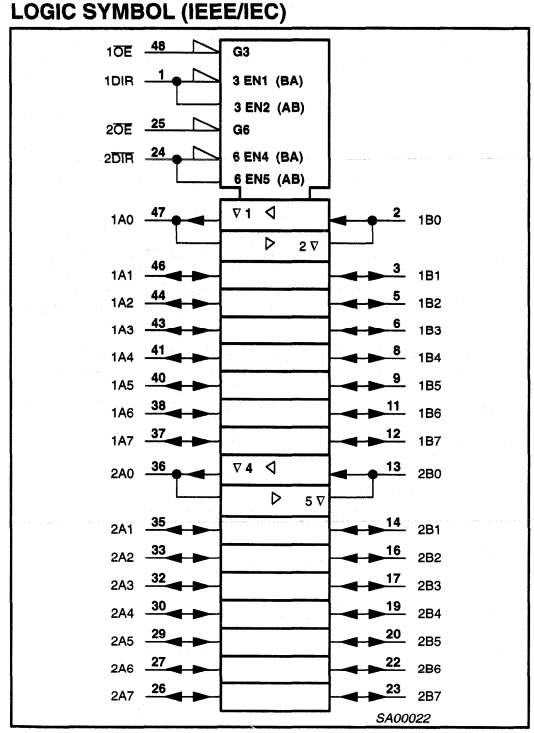
LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1DIR, 2DIR	1, 24	Direction control inputs (Active-High)
1A0 – 1A7, 2A0 – 2A7	47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	Data inputs/outputs (A side)
1B0 – 1B7 2B0 – 2B7	2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	Data inputs/outputs (B side)
$1\overline{OE}$, $2\overline{OE}$	48, 25	Output enables
GND	4, 10, 15, 21 28, 34, 39, 45	Ground (0V)
V_{CC}	7, 18, 31, 42	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" scale

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V; Control pins		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus hold current A and B inputs 74ABTH16245B	V_{CC} = 4.5V; V_I = 0.8V	50			50		µA
		V_{CC} = 5.5V; V_I = 2.0V	–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V	±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH}+I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		0.1	10		10	µA
$I_{IL}+I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		0.1	10		10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–92	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.30	0.70		0.70	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		10	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.30	0.70		0.70	mA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		400	700		700	µA
		Outputs disabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		100	250		250	µA
		Control pins, outputs disabled, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		400	700		700	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This is the bus hold overdrive current required to force the input to the opposite logic state.

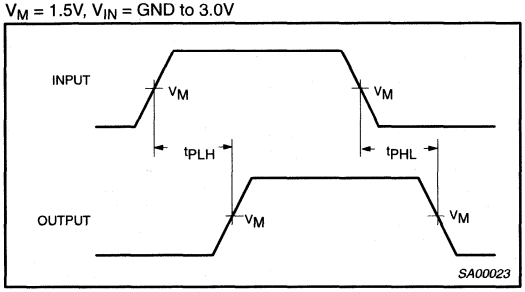
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

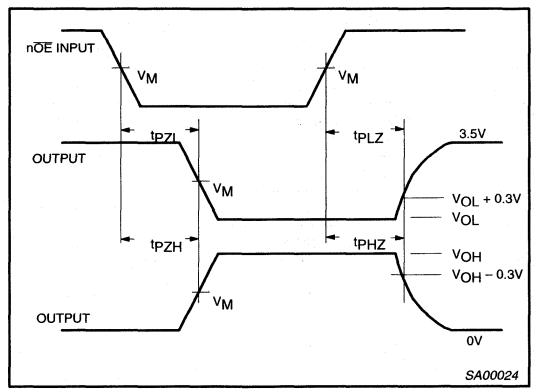
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.0 1.0	2.0 2.3	3.2 3.5	1.0 1.0	3.5 4.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.7	3.1 4.0	4.4 5.2	1.0 1.7	5.1 6.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.7 1.5	3.5 3.2	4.9 4.4	1.7 1.5	5.4 5.0	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

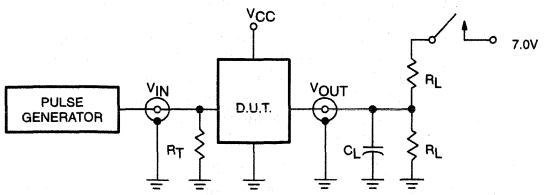


Waveform 1. Input to Output Propagation Delays

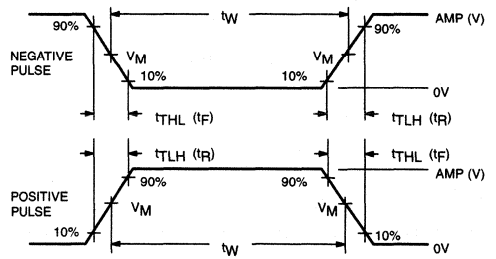


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

16-bit bus transceiver with 30Ω series termination resistors (3-State)

74ABT162245A
74ABTH162245A

FEATURES

- 16-bit bidirectional bus interface
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +12mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same part as 74ABT16245A-1
- 74ABTH162245A incorporates bus hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT162245A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT162245A device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable ($1\overline{OE}$, $2\overline{OE}$) inputs for easy cascading and two Direction (1DIR, 2DIR) inputs for direction control.

The 74ABT162245A is designed with 30 ohm series resistance in both the upper and lower output structures on both A and B ports. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receiver/transmitters.

The 74ABT162245A is the same as the 74ABT16245A-1. The part number has been changed to reflect industry standards

Two options are available, 74ABT162245A which does not have the bus hold feature and the 74ABTH162245A which incorporates the bus hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 5V	2.0 3.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O pin capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	300	nA
I_{CCL}		Outputs Low; V_{CC} = 5.5V	10	mA

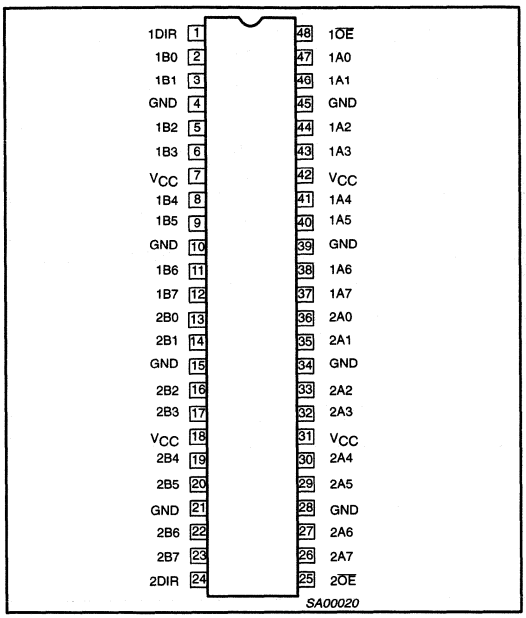
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT162245A DL	BT162245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT162245A DGG	BT162245A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH162245A DL	BH162245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH162245A DGG	BH162245A DGG	SOT362-1

16-bit bus transceiver with 30Ω series termination resistors (3-State)

74ABT162245A
74ABTH162245A

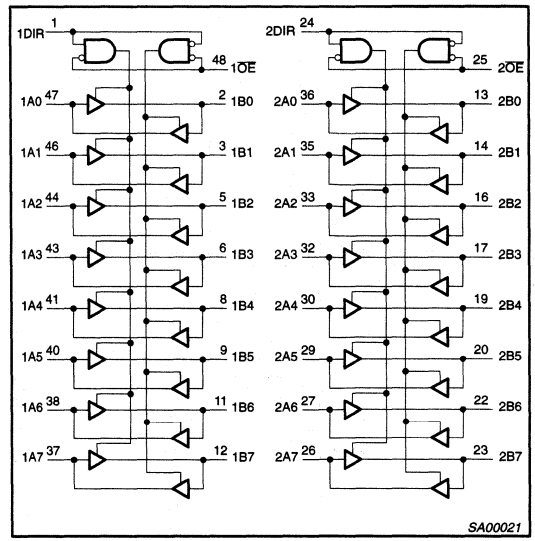
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1DIR, 2DIR	1, 24	Direction control inputs (Active-High)
1A0 – 1A7, 2A0 – 2A7	47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	Data inputs/outputs (A side)
1B0 – 1B7 2B0 – 2B7	2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	Data inputs/outputs (B side)
$1\overline{OE}$, $2\overline{OE}$	48, 25	Output enables
GND	4, 10, 15, 21 28, 34, 39, 45	Ground (0V)
V_{CC}	7, 18, 31, 42	Positive supply voltage

LOGIC SYMBOL

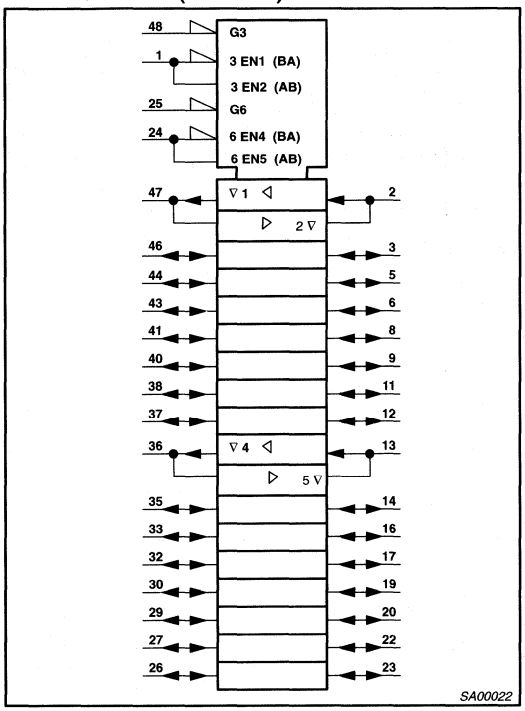


FUNCTION TABLE

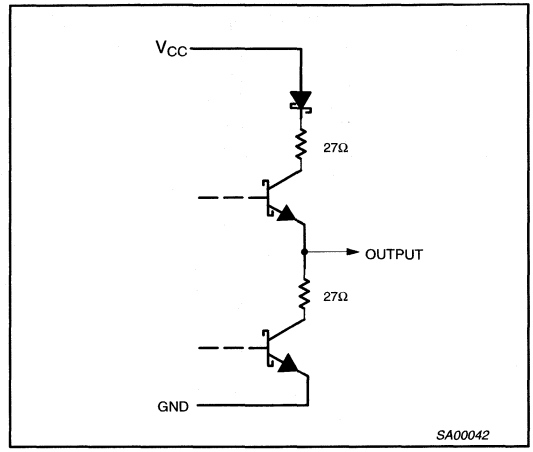
INPUTS		INPUTS/OUTPUTS	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = D0n't care
Z = High impedance "off" state

LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 8mA; V_I = V_{IL} or V_{IH}		0.46	0.65		0.65	V
	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 12mA; V_I = V_{IL} or V_{IH}		0.50	0.80		0.80	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V (Control pins)		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus hold current A and B inputs[4] 74ABTH162245A	V_{CC} = 4.5V; V_I = 0.8V	50			50		µA
		V_{CC} = 5.5V; V_I = 2.0V	−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V	±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH}+I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		0.5	10		10	µA
$I_{IL}+I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		−0.5	−10		−10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−92	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.3	0.70		0.70	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		10	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.3	0.70		0.70	mA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		400	700		700	µA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V 74ABT162245A		1.0	50		50	µA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V 74ABTH162245A		100	250		250	µA
		Control pins, outputs disabled, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		400	700		700	µA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5 ±10% a transition time of up to 100 µsec is permitted.
4. This is the bus hold overdrive current required to force the input to the opposite logic state.

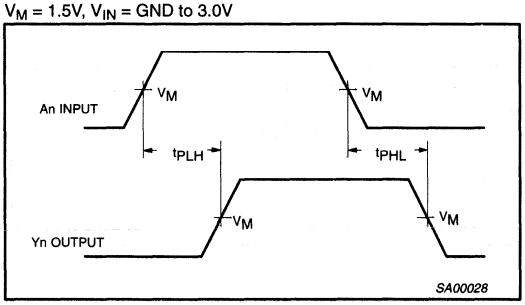
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

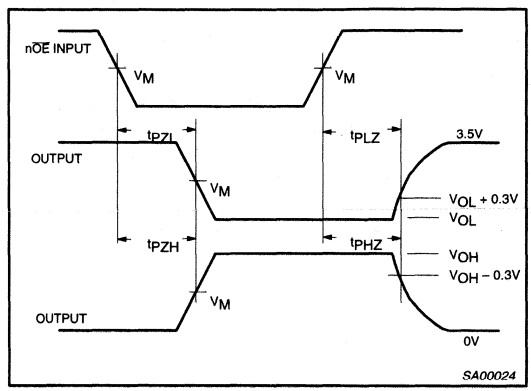
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.0 1.5	2.0 3.0	3.3 4.5	1.0 1.5	3.5 4.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 2.0	3.1 5.0	4.3 6.1	1.5 2.0	5.0 7.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.7 1.5	3.5 3.2	4.8 4.5	1.7 1.5	5.4 4.9	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

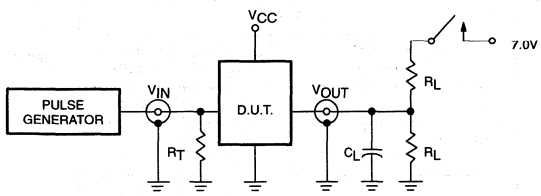


Waveform 1. Input to Output Propagation Delays

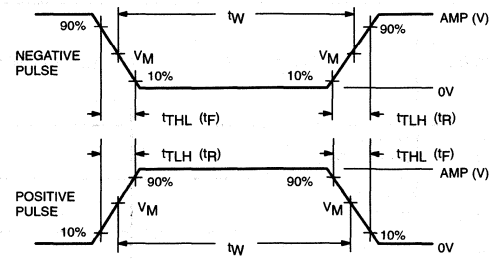


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

12-bit to 24-bit multiplexed D-type latches (3-State)

74ABT16260
74ABTH16260

FEATURES

- ESD protection exceeds 2000V per Mil-Std-883C, Method 3015; exceeds 200V using machine model (C = 200pF, R = 0).
- Latch-up performance exceeds 500mA per JEDEC Standard JESD-17.
- Distributed V_{CC} and GND pin configuration minimizes high-speed switching noise.
- Flow-through architecture optimizes PCB layout.
- High-drive outputs (–32mA I_{OH}, 64mA I_{OL}).
- 74ABTH16260 incorporates bus-hold inputs which eliminate the need for external pull-up resistors.
- Package options:
  - 56-pin plastic Shrink Small-Outline Package (SSOP)
  - 56-pin plastic Thin Shrink Small-Outline Package (TSSOP)

DESCRIPTION

The 74ABT16260/74ABTH16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is alto useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch enable input is high, the latch is transparent. When the latch enable input goes low, the data present at the inputs is latched and remains latched until the latch enable input is returned high.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The 74ABTH incorporates the bus hold feature. The 74ABT does not include bus hold feature. Both parts are available in 56-pin SSOP and TSSOP.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx nBx to nAx	C_L = 50 pF	2.8 2.5	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_{I/O}$ = 0 V or 5.0 V	6	pF
I_{CCZ}	Total supply current	Outputs disabled	100	µA

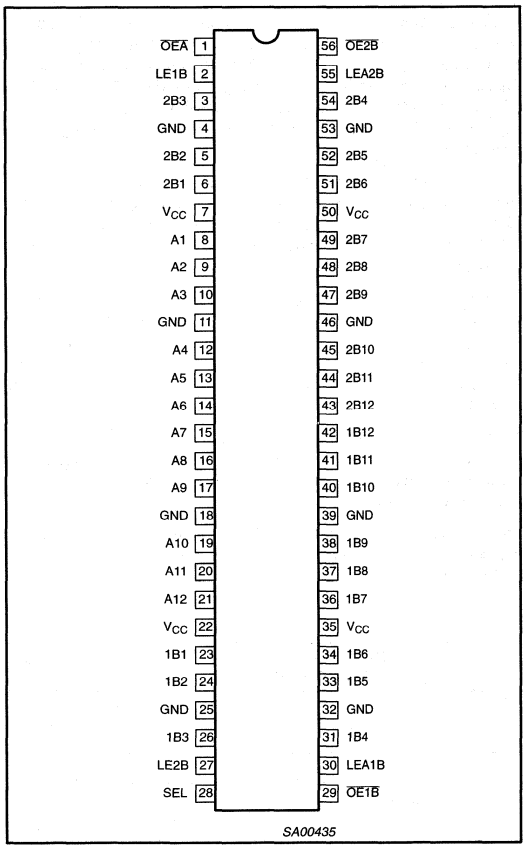
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16260 DL	BT16260 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16260 DGG	BT16260 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16260 DL	BH16260 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16260 DGG	BH16260 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21	An	Data inputs/outputs (A)
23, 24, 26, 31, 33, 34, 36, 37, 38, 40, 41, 42	1Bn	Data inputs/outputs (B1)
6, 5, 3, 54, 52, 51, 49, 48, 47, 45, 44, 43	2Bn	Data inputs/outputs (B2)
1, 29, 56	$\overline{OEA}$, $\overline{OE1B}$, $\overline{OE2B}$	Output enable input (active low)
2, 27, 30, 55	LE1B, LE2B, LEA1B, LEA2B	Latch enable inputs

PIN CONFIGURATION



SA00435

FUNCTION TABLES

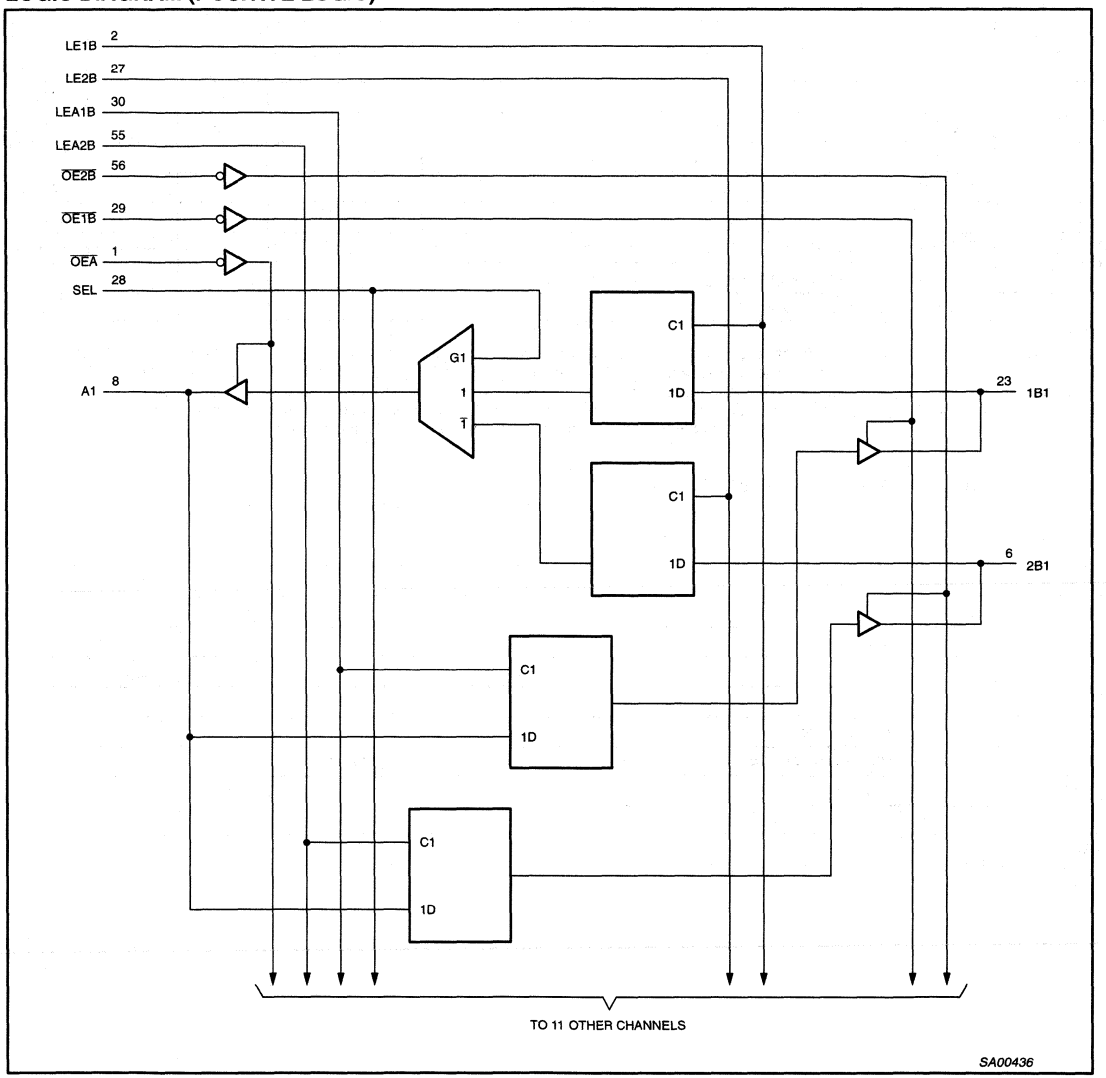
B to A ($\overline{OEB}$ = H)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A0
X	X	X	X	X	H	Z

A to B ($\overline{OEA}$ = H)

INPUTS					OUTPUT	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B0
L	H	L	L	L	L	2B0
H	L	H	L	L	1B0	H
L	L	H	L	L	1B0	L
X	L	L	L	L	1B0	2B0
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise specified)[1]

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range	see Note 2	–0.5	7	V
V_O	Voltage range applied to any output in the high state or power-off state		–0.5	5.5	V
I_O	Current into any output in the low state			128	mA
I_{IK}	Input clamp current	$V_I < 0$		–18	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
	Maximum power dissipation at T_{amb} = 55°C (in still air)	see Note 3		1.4	W
T_{stg}	Storage temperature range		–65	+150	°C

NOTES:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER		LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		μs/V
T_{amb}	Operating free-air temperature		–40	+85	°C

NOTE:

1. Unused or floating inputs must be held high or low.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.8	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC} or GND	Data pins			±3		±5	µA
I_{HOLD}	Bus Hold current	V_{CC} = 4.5V; V_I = 0.8V	A or B ports	75			75		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500			±500		
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = V_{CC}			±60	±200		±200	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			−1.0	−10		−10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}				50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−100	−225	−50	−225	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.2	1.5		1.5	mA
		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	
		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.1	1.0		1.0	
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			0.1	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
3. This is the bus hold minimum overdrive current required to force the input to the opposite logic state.

AC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		V_{CC} = 5V, T_{amb} = 25°C			T_{amb} = –40°C to +85°C		UNIT
	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.8	4.8	1	5.6	ns
t_{PHL}			1	2.5	5	1	5.9	ns
t_{PLH}	$\overline{LE}$	A or B	1.1	3.2	4.9	1.1	5.8	ns
t_{PHL}			1.1	3.2	4.9	1.1	5.3	ns
t_{PLH}	SEL (B1)	A	1.3	3.2	4.6	1.3	5.3	ns
	SEL (B2)	A	1.1	2.8	4.9	1.1	6	ns
t_{PHL}	SEL (B1)	A	1.5	3.0	4.4	1.5	4.4	ns
	SEL (B2)	A	1.6	2.6	5.1	1.6	5.9	ns
t_{PZH}	$\overline{OE}$	A or B	1	2.9	4.7	1	5.7	ns
t_{PZL}			1.6	2.2	5.1	1.6	5.8	ns
t_{PHZ}	$\overline{OE}$	A or B	2.2	4.1	5.4	2.2	6.4	ns
t_{PLZ}			1.3	3.2	4.4	1.3	4.8	ns

AC SETUP CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	V_{CC} = 5V, T_{amb} = 25°C		T_{amb} = –40°C to +85°C		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5		1.5		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		1		ns

AC WAVEFORMS

V_M = 1.5V for all waveforms

The outputs are measured one at a time with one transition per measurement.

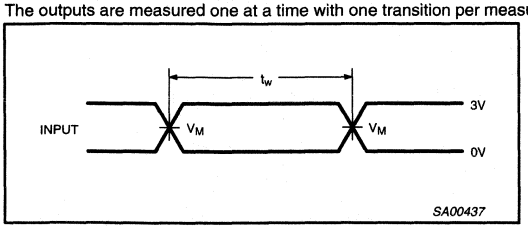


Figure 1. Pulse duration

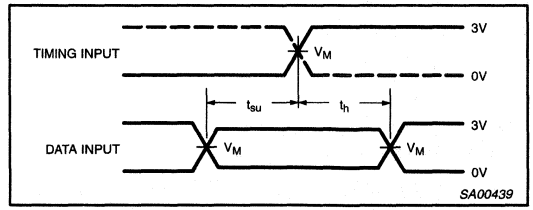
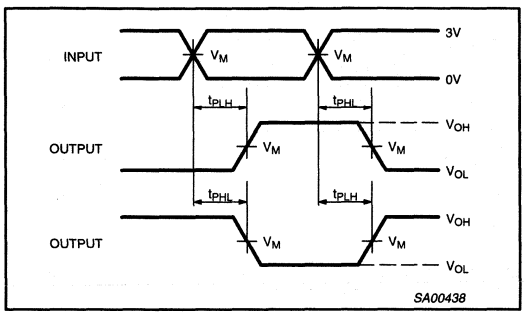
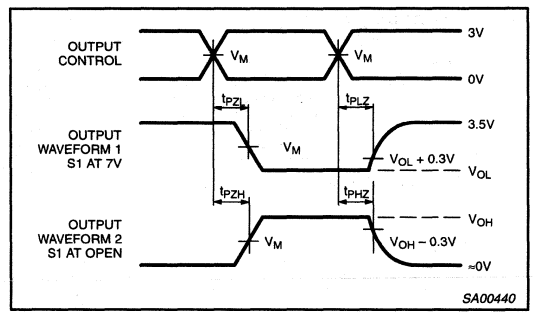


Figure 3. Setup and hold times



All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r ≤ 2.5ns, t_f ≤ 2.5ns.

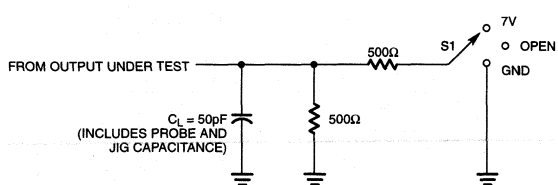
Figure 2. Propagation delay times; inverting and non-inverting outputs



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 4. Enable and disable times; low- and high-level enabling

TEST LOAD CIRCUIT



Load Circuit for Outputs

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7V
t_{PHZ}/t_{PZH}	Open

SA00441

Figure 5. Test load circuit

16-bit D-type flip-flop

74ABT16273
74ABTH16273

FEATURES

- 16-bit D-type edge triggered flip-flops
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Live insertion/extraction permitted
- Power-up reset
- 74ABTH16273 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16273 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This part is a 16-bit edge triggered D-type flip-flop with non-inverting high drive outputs. This device can be used as two 8-bit flip-flops or one 16-bit flip-flop. When the clock (CP) goes High, the data on the D inputs is stored and the Q outputs display the stored data.

This device also features a master reset ($\overline{MR}$) that resets all flip-flops to the Low state when $\overline{MR}$ is set to the Low state.

Two options are available, 74ABT16273 which does not have the bus-hold feature and 74ABTH16273 which incorporates the bus-hold feature.

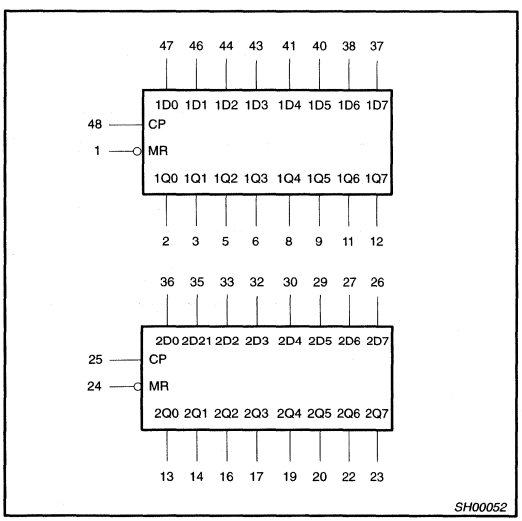
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5.0V	2.5 2.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
I_{CCH}	Quiescent supply current	Outputs High; V_{CC} = 5.5V	200	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16273 DL	BT16273 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16273 DGG	BT16273 DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16273 DL	BH16273 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16273 DGG	BH16273 DGG	SOT362-1

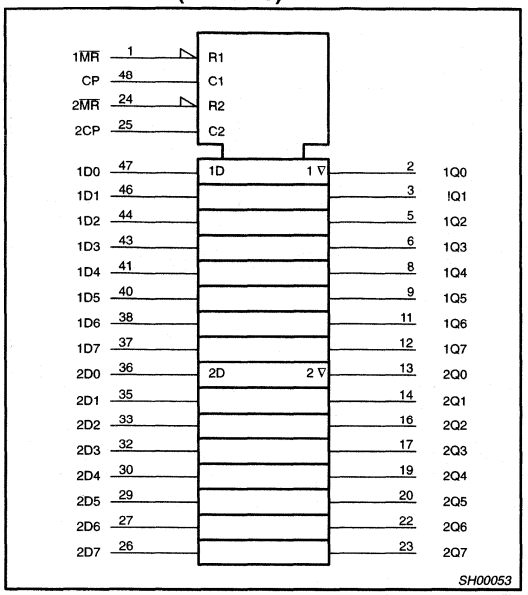
LOGIC SYMBOL



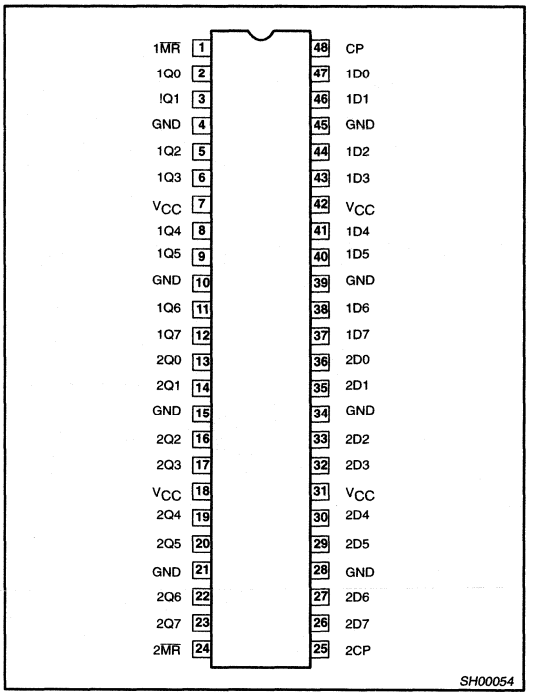
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	1$\overline{MR}$, 2$\overline{MR}$	Master reset input (active-Low)
2, 3, 5, 6, 8, 9, 11, 12,13, 14, 16, 17, 19, 20, 22, 23	1Q0-1Q7 2Q0-2Q7	Data outputs
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0-1D7 2D0-2D7	Data inputs
25, 48	1CP, 2CP	Clock pulse input (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION

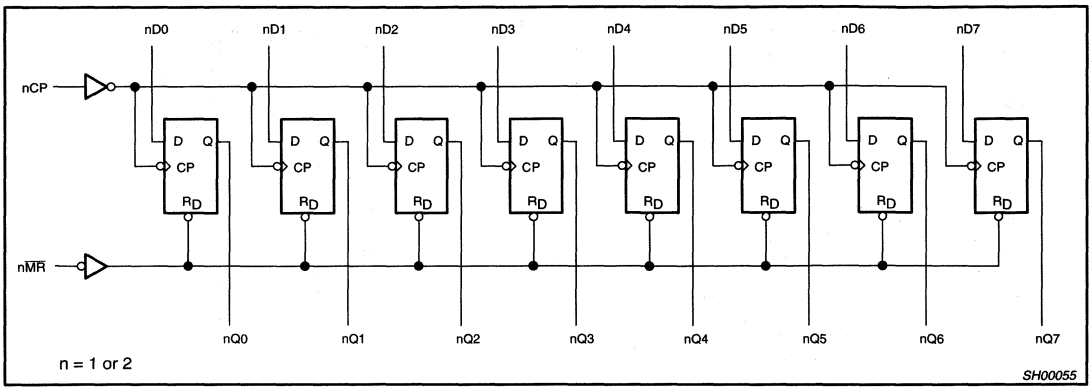


FUNCTION TABLE

Inputs			Output	operating mode
nMR	nCP	nDX	nQ0-nQ7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"
H	L	X	Q_0	Retain state

H = High voltage level
h = high voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Q_0 = Output as it was

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to –7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				Temp = +25°C			Temp = -40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = –32mA; V_{IL} or V_{IH}		2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current 74ABT16273	V_{CC} = 5.5V; V_I = V_{CC} or GND			±0.1	±1		±1	µA
I_I	Input leakage current 74ABTH16273	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0	Data pins		–2	–3		–5	µA
I_{HOLD}	Bus Hold current inputs[4] 74ABTH16273	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC}= 0.0V; V_O or V_I < 4.5V			±5.0	±100		±100	µA
I_O	output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–70	–180	–50	–180	mA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			5.0	50		50	µA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.2	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16273	V_{CC} = 5.5V; One input at 3.4V. Other inputs at V_{CC} or GND			5	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16273	V_{CC} = 5.5V; One input at 3.4V. Other inputs at V_{CC} or GND			0.2	1		1	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω;

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40 to +85 °C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.5 1.2	2.5 2.0	3.4 2.7	1.5 1.2	4.0 3.0	ns
t_{PHL}	Propagation delay $\overline{nMR}$ to nQx	2	1.9	3.7	4.3	1.9	5.3	ns
f_{MAX}	Maximum clock frequency	1	150	240		150		MHz

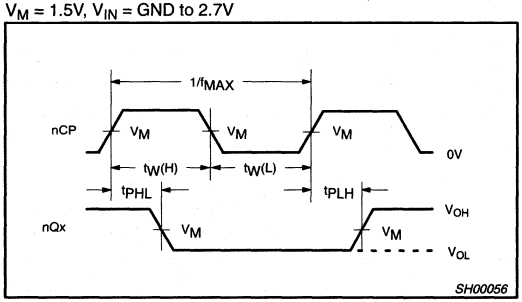
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

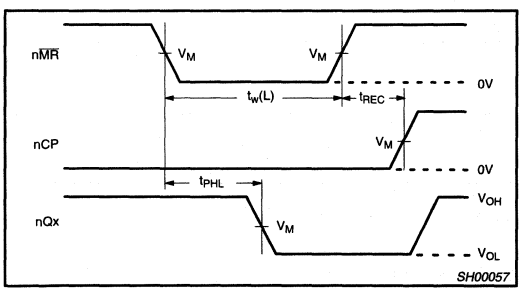
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = −40 to +85 °C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low nDx to nCP	3	2.0 2.0	1.0 1.0	2.0 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	3	0 0	−0.6 −0.6	0 0	ns
$t_W(H)$ $t_W(L)$	Clock pulse width High or Low	1	3.3 3.3	1.2 1.0	3.3 3.3	ns
$t_W(L)$	Master Reset pulse width, Low	2	3.3	1.1	3.3	ns
t_{REC}	Recovery time $n\overline{MR}$ + nCP	2	2.0	0.0	2.0	ns

AC WAVEFORMS

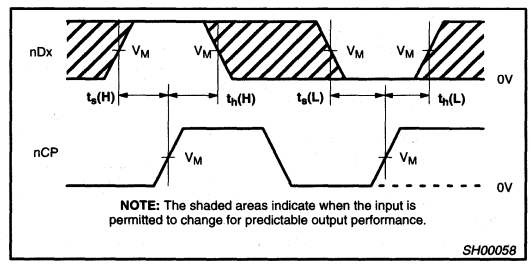
V_M = 1.5V, V_{IN} = GND to 2.7V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

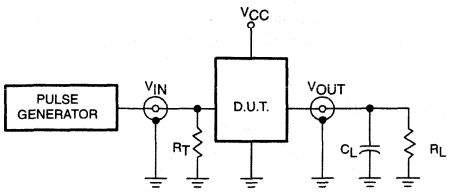


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

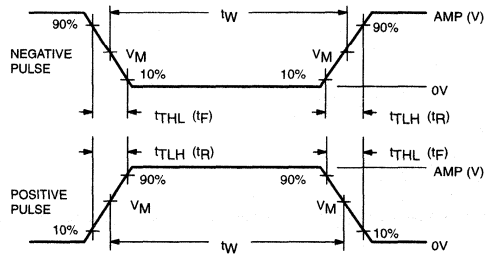


Waveform 3. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00059

16-bit transparent latch (3-State)

74ABT16373B
74ABTH16373B

FEATURES

- 16-bit transparent latch
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- Live insertion/extraction permitted
- Power-up reset
- 3-State output buffers
- 74ABTH16373B incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- I_{CCL} –19 mA maximum
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16373B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16373B device is a dual octal transparent latch coupled to two sets of eight 3-State output buffers. The two sections of the device are controlled independently by Enable (nE) and Output Enable ($n\overline{OE}$) control gates.

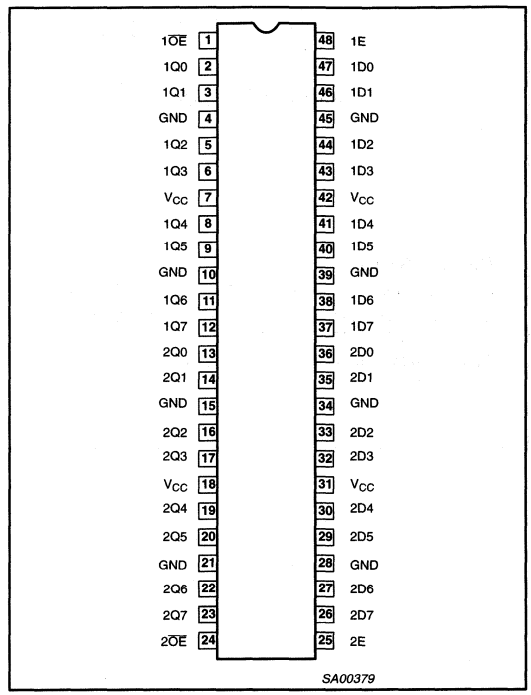
The data on each set of D inputs are transferred to the latch outputs when the Latch Enable (nE) input is High. The latch remains transparent to the data inputs while nE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-Low Output Enable ($n\overline{OE}$) controls eight 3-State buffers independent of the latch operation.

When $n\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $n\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

Two options are available, 74ABT16373B which does not have the bus-hold feature and 74ABTH16373B which incorporates the bus-hold feature.

PIN CONFIGURATION



SA00379

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	2.5 2.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

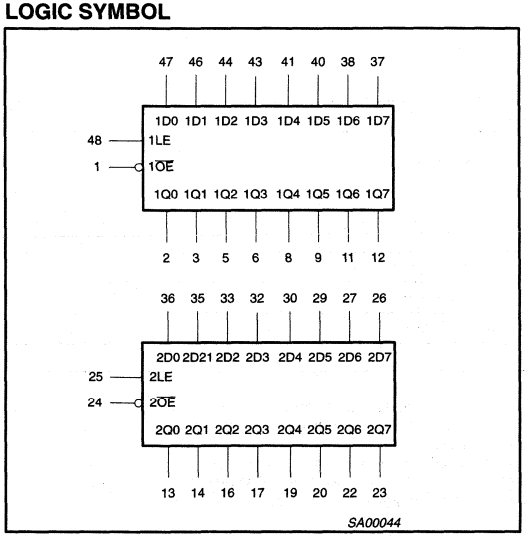
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin SSOP type III	–40°C to +85°C	74ABT16373B DL	BT16373B DL	SOT370-1
48-Pin TSSOP type II	–40°C to +85°C	74ABT16373B DGG	BT16373B DGG	SOT362-1
48-Pin SSOP type III	–40°C to +85°C	74ABTH16373B DL	BH16373B DL	SOT370-1
48-Pin TSSOP type II	–40°C to +85°C	74ABTH16373B DGG	BH16373B DGG	SOT362-1

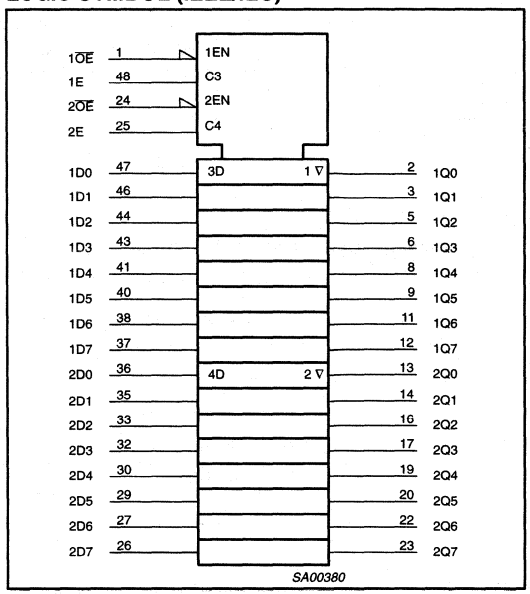
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1E, 2E	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

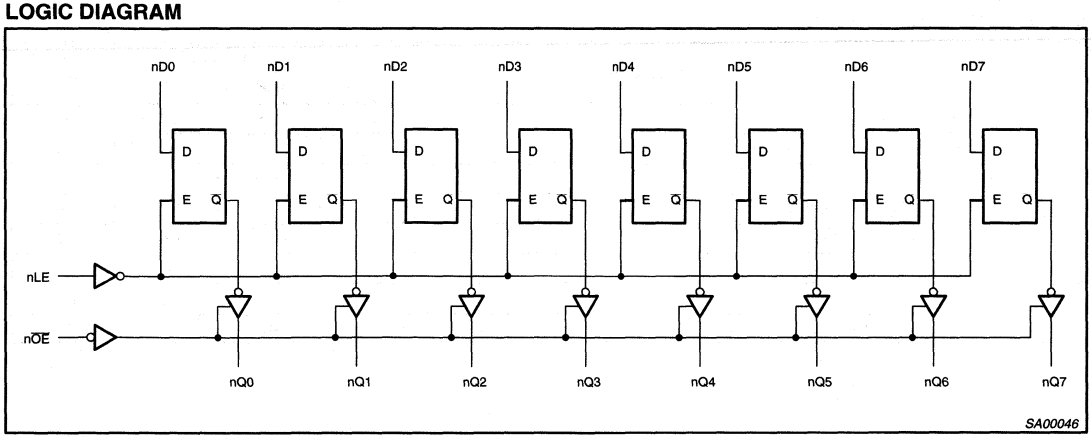
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nE	nDx		nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	i h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current 74ABT16373B	V_{CC} = 5.5V; V_I = V_{CC} or GND			±0.01	±1		±1	µA
I_I	Input leakage current 74ABTH16373B	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins[b]		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0			−1	−3		−5	µA
I_{HOLD}	Bus Hold current A inputs[4] 74ABTH16373B	V_{CC} = 4.5V; V_I = 0.8V		50			50		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = GND			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}			0.5	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}			−0.5	−10		−10	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−70	−180	−50	−180	mA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			0.1	50		50	µA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16373B	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			5	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16373B	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1 to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. Unused pins at V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.5 1.1	2.5 2.0	3.8 3.1	1.5 1.1	4.4 3.8	ns
t_{PLH} t_{PHL}	Propagation delay nE to nQx	1	1.6 1.3	2.5 2.1	3.8 3.1	1.6 1.3	4.4 3.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.2 1.3	2.3 2.3	3.5 3.5	1.2 1.3	4.6 4.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.9 1.7	3.1 2.6	4.5 3.8	1.9 1.7	5.3 4.2	ns

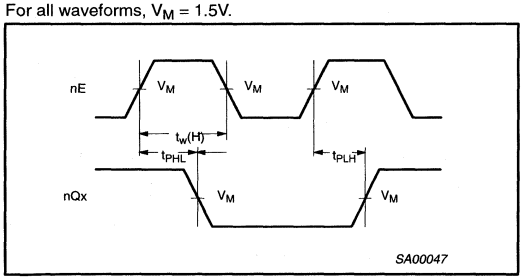
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

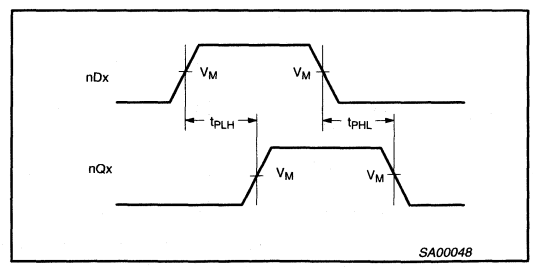
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time, High or Low nDx to nE	3	1.0 1.0	0.0 0.3	1.0 1.0	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nE	3	0.5 0.5	−0.2 0.0	0.5 0.5	ns
t_w(H)	Enable pulse width High	1	2.5	1.0	2.5	ns

AC WAVEFORMS

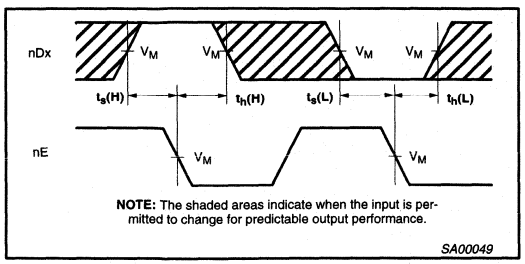
For all waveforms, V_M = 1.5V.



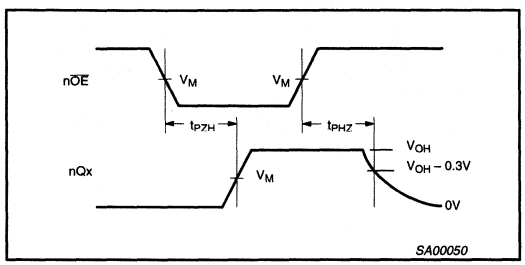
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



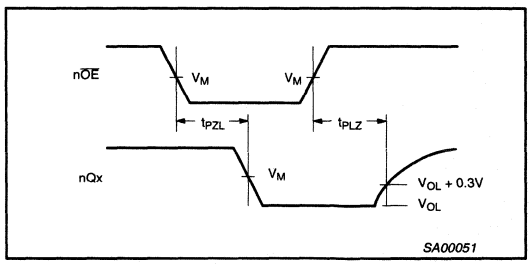
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

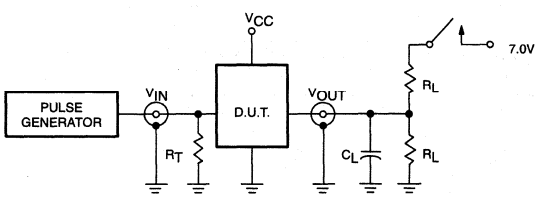


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

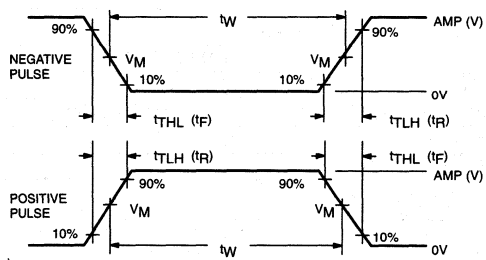


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

16-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT16374B
74ABTH16374B

FEATURES

- Two 8-bit positive edge triggered registers
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State output buffers
- 74ABTH16373B incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16374B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16374B has two 8-bit, edge triggered registers, with each register coupled to eight 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-Low Output Enable ($n\overline{OE}$) controls all eight 3-State buffers for its register independent of the clock operation.

When $n\overline{OE}$ is Low, the stored data appears at the outputs for that register. When $n\overline{OE}$ is High, the outputs for that register are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

Two options are available, 74ABT16374B which does not have the bus-hold feature and 74ABTH16374B which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	2.6 2.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs Low; V_{CC} = 5.5V	8	mA

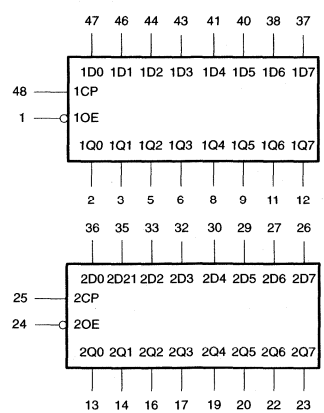
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16374B DL	BT16374B DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16374B DGG	BT16374B DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16374B DL	BH16374B DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16374B DGG	BH16374B DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

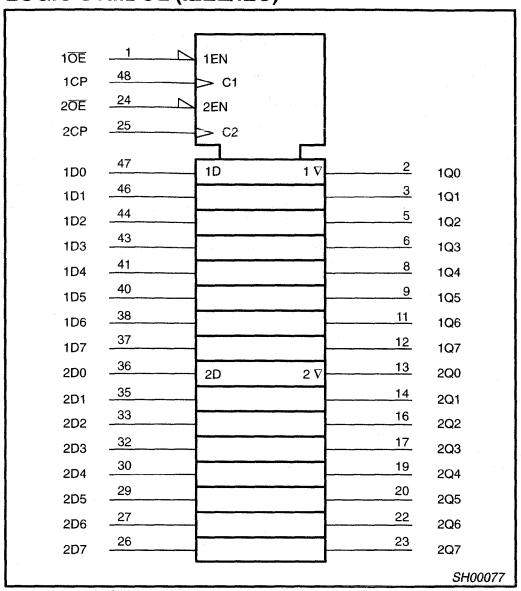
LOGIC SYMBOL



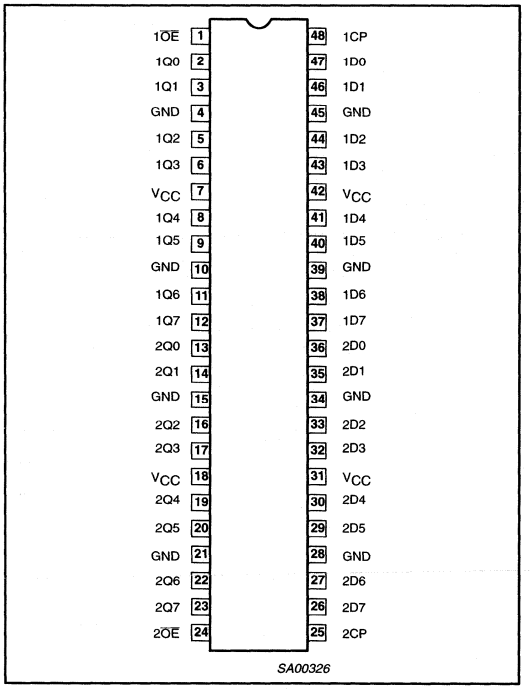
16-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT16374B
74ABTH16374B

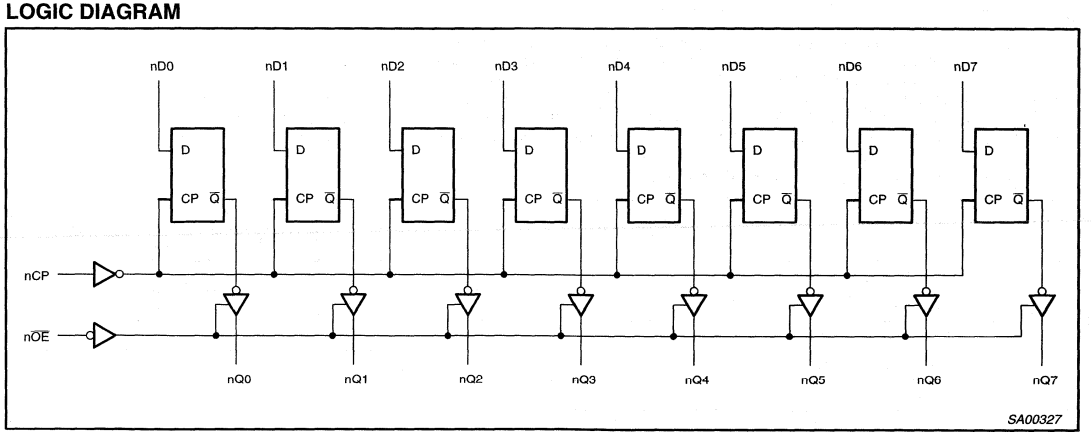
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx		nQ0 – nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↥	X	NC	NC	Hold
H H	↥ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↥ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current 74ABT16374B	V_{CC} = 5.5V; V_I = V_{CC} or GND			0.01	±1		±1	µA
I_I	Input leakage current 74ABTH16374B	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins[5]		0.01	1		1	
		V_{CC} = 5.5V; V_I = 0			−1	−3		−5	
I_{HOLD}	Bus Hold current inputs[4] 74ABTH16374B	V_{CC} = 4.5V; V_I = 0.8V		50			50		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = GND			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			0.5	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			−0.5	−10		−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−70	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16374B	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			5	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16374B	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. Unused pins at V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	180	260				MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.7 1.4	2.6 2.2	4.0 3.4	1.7 1.4	4.7 3.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.3 1.3	2.4 2.3	3.7 3.4	1.3 1.3	4.7 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.9 1.7	3.1 2.6	4.6 4.0	1.9 1.7	5.5 4.4	ns

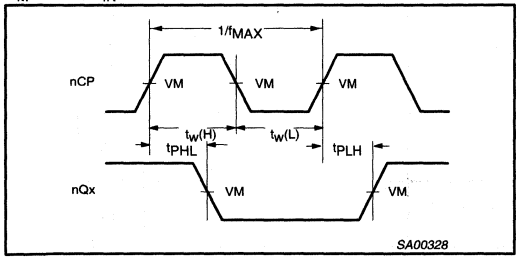
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

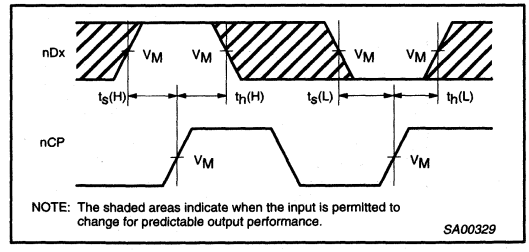
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	2	1.0 1.0	0.3 0.1	1.0 1.0	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	2	1.0 1.0	−0.1 −0.3	1.0 1.0	ns
t_w(H) t_w(L)	nCP pulse width High or Low	1	2.8 2.8	1.2 1.5	2.8 2.8	ns

AC WAVEFORMS

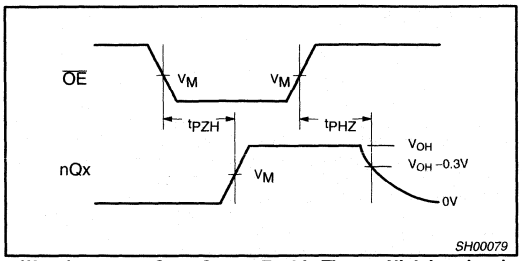
V_M = 1.5V, V_{IN} = GND to 3.0V



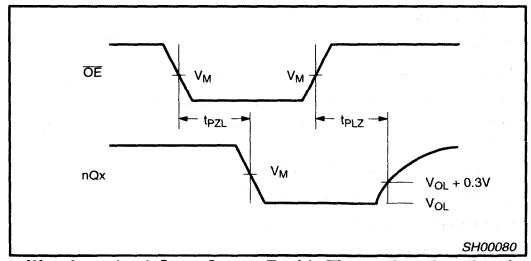
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

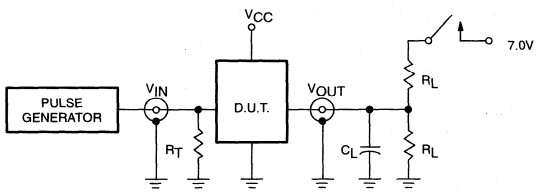


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

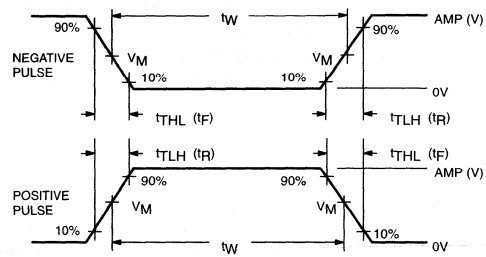


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

18-bit universal bus transceiver (3-State)

74ABT16500C
74ABTH16500C

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- 74ABTH16500C incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Negative edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Flexible operation permits 18 embedded D-type latches or flip-flops to operate in clocked, transparent, or latched modes.

DESCRIPTION

The 74ABT16500C is a high-performance BiCMOS Device which combines low static and dynamic power dissipation with high speed and high output drive.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock ($\overline{\text{CPAB}}$ and $\overline{\text{CPBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if $\overline{\text{CPAB}}$ is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of $\overline{\text{CPAB}}$. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{\text{OEBA}}$, LEBA and $\overline{\text{CPBA}}$. The output enables are complimentary (OEAB is active High, and $\overline{\text{OEBA}}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Two options are available, 74ABT16500C which does not have the bus-hold feature and 74ABTH16500C which incorporates the bus-hold feature.

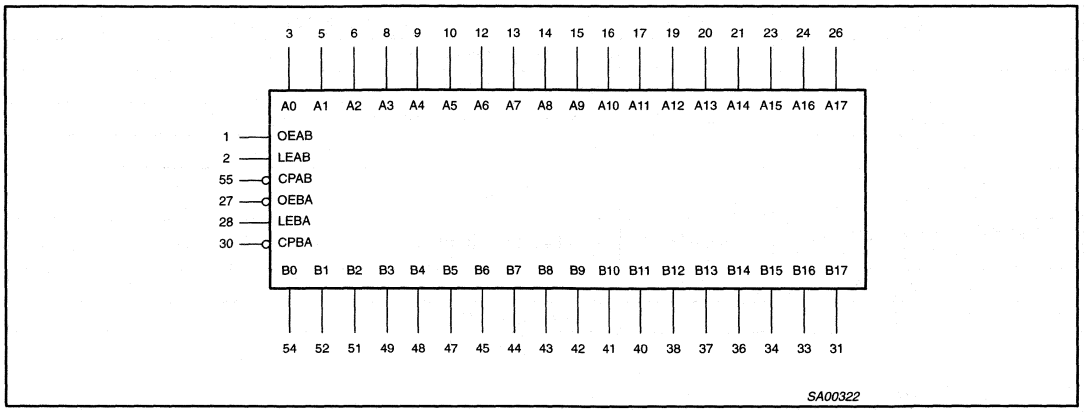
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.1 1.7	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or V_{CC}	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	μA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

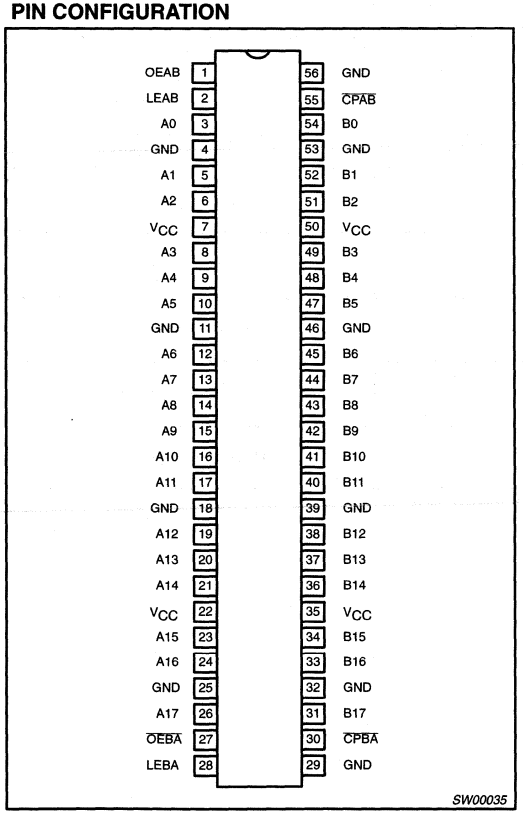
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16500C DL	BT16500C DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16500C DGG	BT16500C DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16500C DL	BH16500C DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16500C DGG	BH16500C DGG	SOT364-1

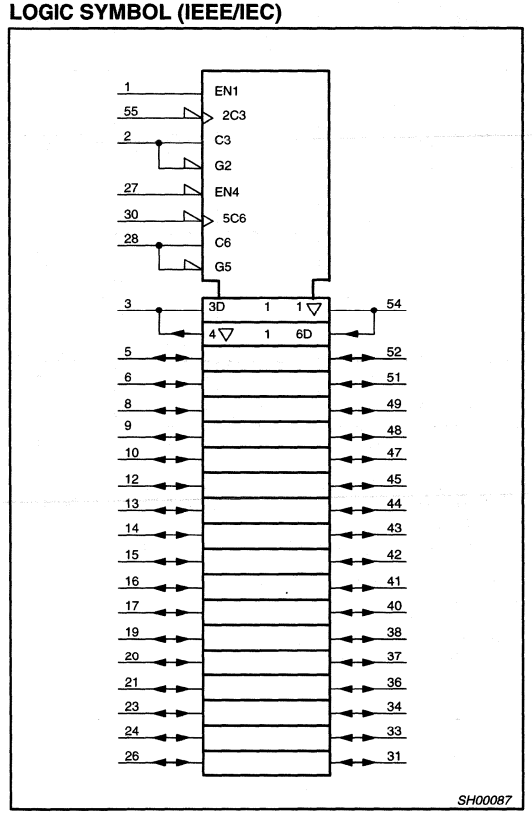
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	$\overline{CPAB}$/$\overline{CPBA}$	A-to-B/B-to-A Clock input (active falling edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

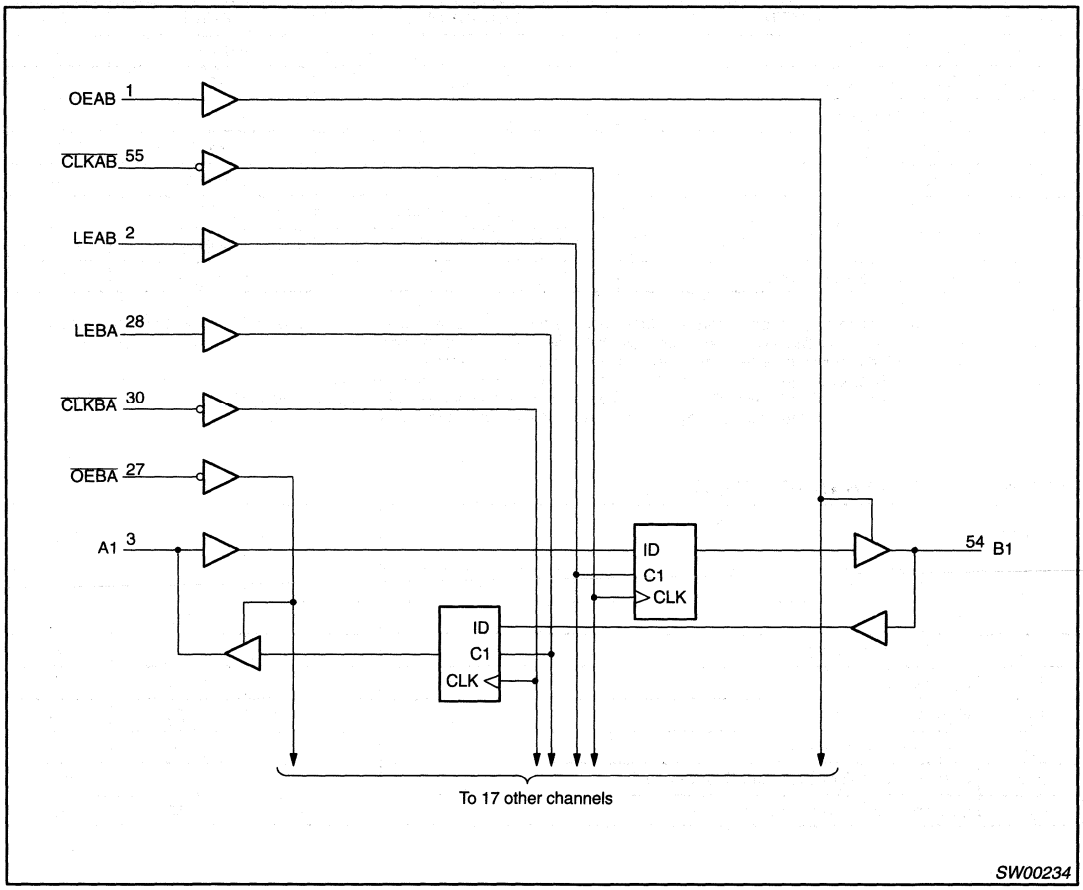
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	$\overline{CPAB}$	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↓	h	H	Z	Disabled, Clock data
L	L	↓	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↓	h	H	H	Clock data & display
H	L	↓	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CPBA}$.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.8	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	4.0		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.35	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V	Control pins		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A and B Ports[4] 74ABTH16500C	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±2	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V or V_{CC}; V_{OE} = Don't care			±2	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}			−1.0	−10		−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			2	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−80	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}			0.5	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16500C	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			5.0	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16500C	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			200	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. Unused pins at V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	1	150	225		150		MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	2.1 1.7	3.0 2.5	1.0 1.0	3.4 3.0	ns
t_{PLH} t_{PHL}	Propagation delay LEAB to Bn or LEBA to An	3	1.0 1.0	3.2 2.8	4.3 3.7	1.0 1.0	4.9 4.0	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.0 1.0	3.4 2.6	4.5 3.5	1.0 1.0	5.3 4.6	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	5 6	1.0 1.5	3.3 2.4	4.4 3.2	1.0 1.5	5.0 3.9	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	5 6	1.5 1.4	3.3 2.5	4.3 3.3	1.5 1.4	5.3 3.9	ns

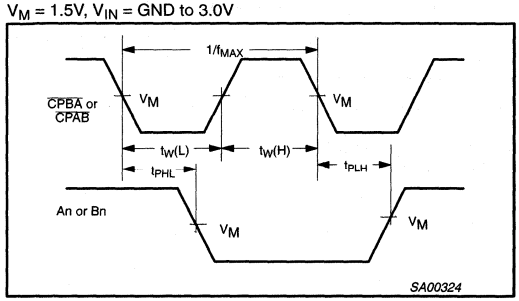
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

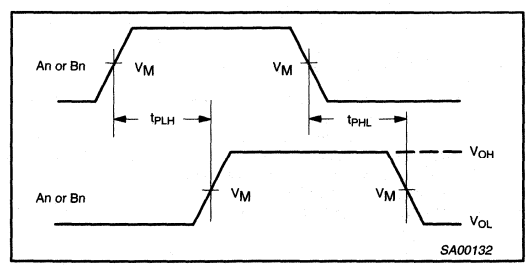
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time, HIGH or LOW An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	2.0 2.0	0.7 0.6	2.0 2.0	ns
t_h(H) t_h(L)	Hold time, HIGH or LOW An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	0.7 0.7	–0.5 –0.8	0.7 0.7	ns
t_s(H) t_s(L)	Setup time, HIGH or LOW An to LEAB or Bn to LEBA	4	2.0 2.0	0.1 0.1	2.0 2.0	ns
t_h(H) t_h(L)	Hold time HIGH or LOW An to LEAB or Bn to LEBA	4	0.7 0.7	–0.1 –0.1	0.7 0.7	ns
t_w	Pulse width, HIGH or LOW $\overline{CPAB}$ or $\overline{CPBA}$	1	3	1.2	3	ns
t_w(H)	Pulse width, HIGH LEAB or LEBA	3	3	1.2	3	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V



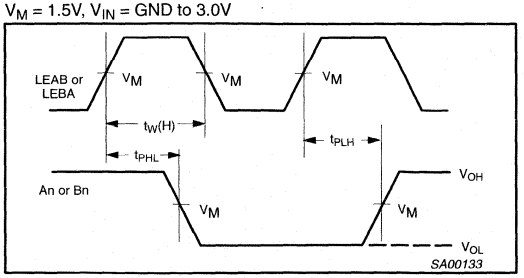
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



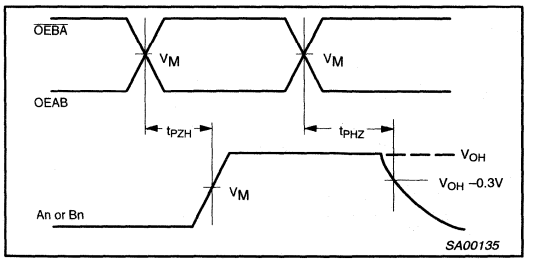
Waveform 2. Propagation Delay, Transparent Mode

AC WAVEFORMS (Continued)

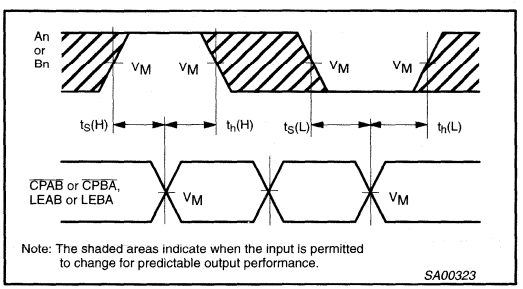
V_M = 1.5V, V_{IN} = GND to 3.0V



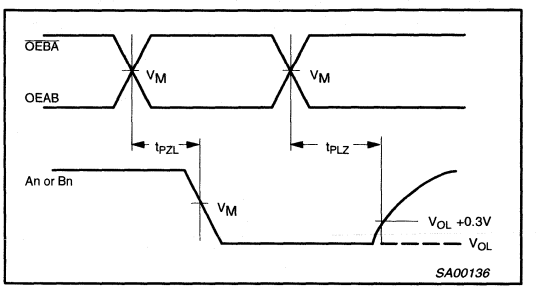
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

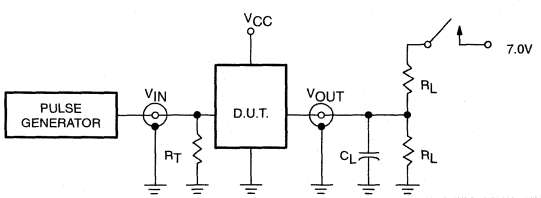


Waveform 4. Data Setup and Hold Times

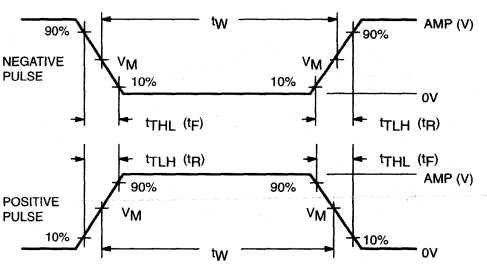


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

18-bit universal bus transceiver (3-State)

74ABT16501A
74ABTH16501A

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- 74ABTH16501A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Positive edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Flexible operation permits 18 embedded D-type latches or flip-flops to operate in clocked, transparent, and latched modes.

DESCRIPTION

The 74ABT16501A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{\text{OEBA}}$, LEBA and CPBA. The output enables are complimentary (OEAB is active High, and $\overline{\text{OEBA}}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Two options are available, 74ABT16501A which does not have the bus-hold feature and 74ABTH16501A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

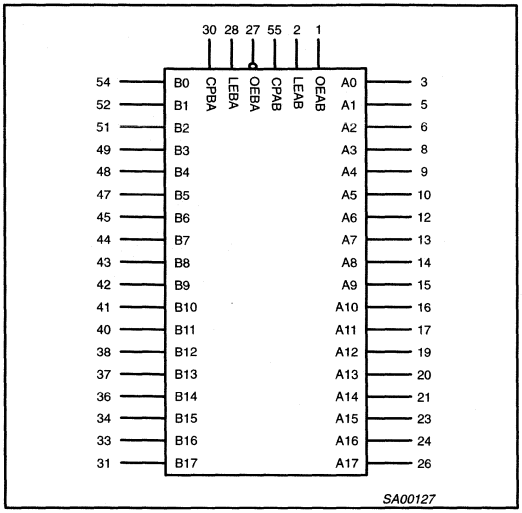
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.2 1.8	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or V_{CC}	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

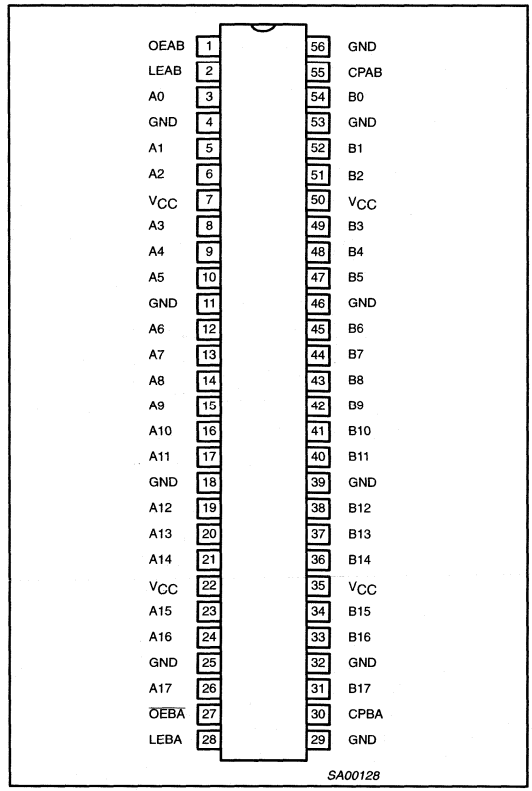
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16501A DL	BT16501A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16501A DGG	BT16501A DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16501A DL	BH16501A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16501A DGG	BH16501A DGG	SOT364-1

18-bit universal bus transceiver (3-State)

LOGIC SYMBOL



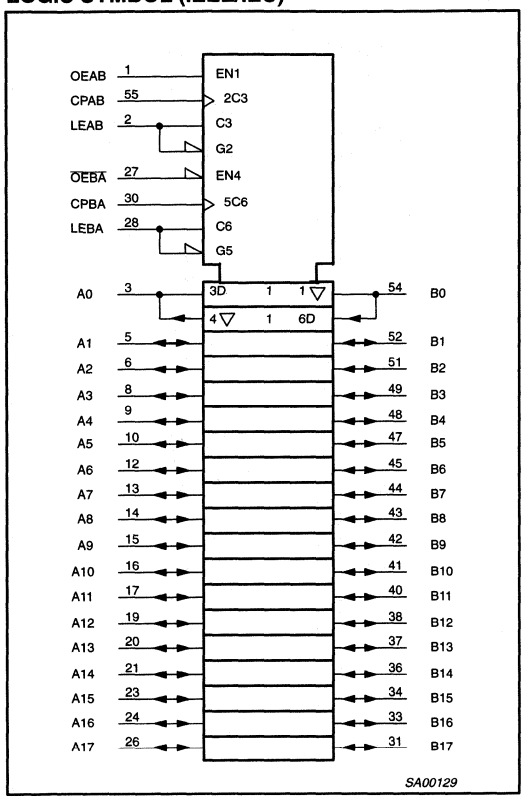
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/ CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



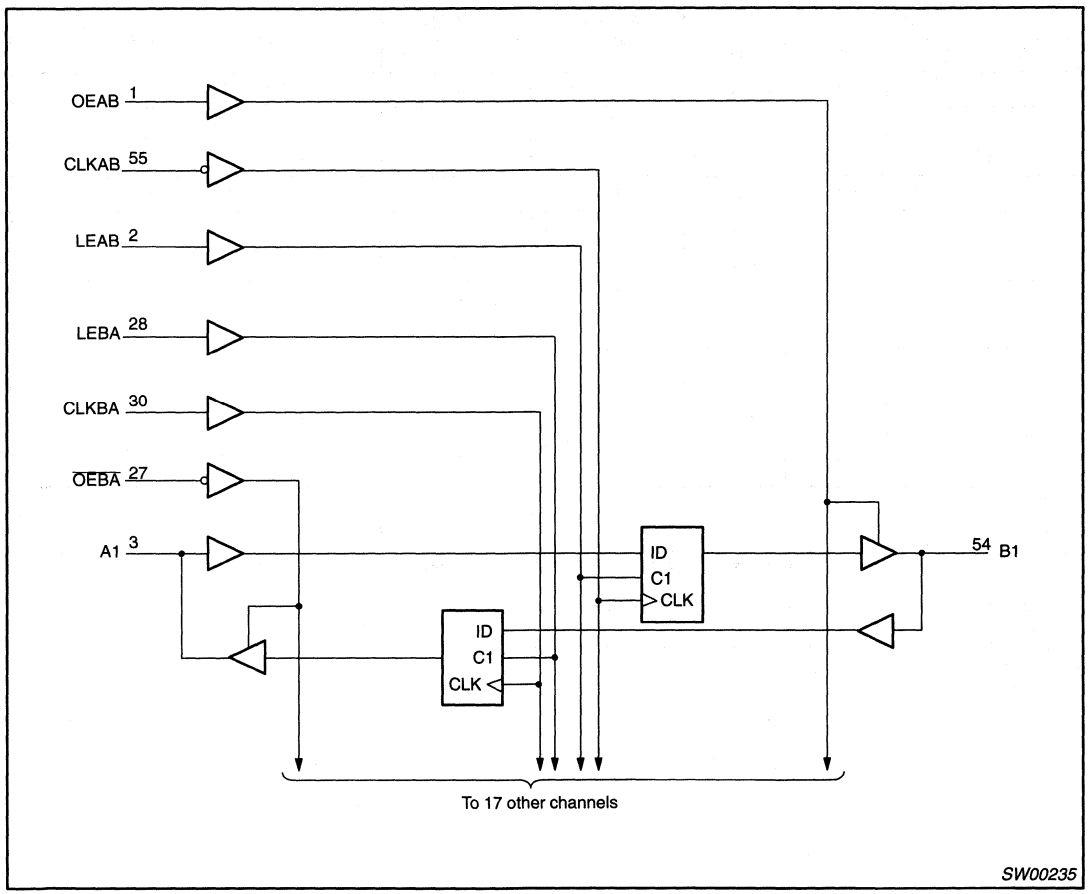
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↑	h	H	Z	Disabled, Clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↑	h	H	H	Clock data & display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CPBA.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition
↑ = Low-to-High Clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.8	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.35	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V; Control pins		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A and B ports[4] 74ABTH16501A	V_{CC} = 4.5V; V_I = 0.8V	35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V	−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V	±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±2	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V or V_{CC}; V_I = GND or V_{CC}; V_{OE} = Don't care		±2	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		1.0	10		10	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		−1.0	−10		−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		2.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−80	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.5	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16501A	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		5.0	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16501A	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		200	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	1	150	225		150		MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	2.2 1.8	3.0 2.5	1.0 1.0	3.5 3.0	ns
t_{PLH} t_{PHL}	Propagation delay LEAB to Bn or LEBA to An	3	1.5 1.4	3.2 2.9	4.3 3.8	1.5 1.4	5.0 4.2	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.6 1.4	3.5 2.9	4.5 3.8	1.6 1.4	5.0 4.2	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	5 6	1.1 1.0	3.0 2.4	4.0 3.4	1.1 1.0	4.7 3.9	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	5 6	1.3 1.0	3.3 2.4	4.3 3.4	1.3 1.0	5.3 3.9	ns

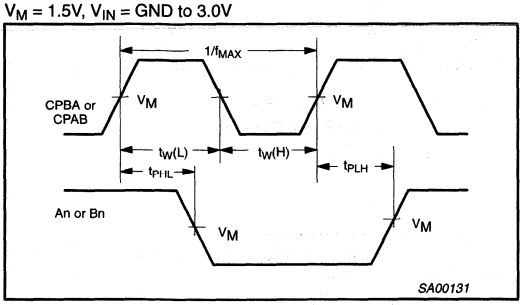
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

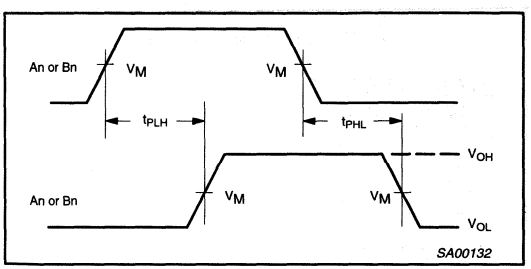
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time, HIGH or LOW An to CPAB or Bn to CPBA	4	2.0 2.0	0.5 0.5	2.0 2.0	ns
t_h(H) t_h(L)	Hold time, HIGH or LOW An to CPAB or Bn to CPBA	4	0.7 0.7	−0.5 −0.5	0.7 0.7	ns
t_s(H) t_s(L)	Setup time, HIGH or LOW An to LEAB or Bn to LEBA	4	2.0 2.0	0.5 0.4	2.0 2.0	ns
t_h(H) t_h(L)	Hold time HIGH or LOW An to LEAB or Bn to LEBA	4	0.7 0.7	−0.4 −0.5	0.7 0.7	ns
t_w	Pulse width, HIGH or LOW CPAB or CPBA	1	3	1.9	3	ns
t_w(H)	Pulse width, HIGH LEAB or LEBA	3	3	1.2	3	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V



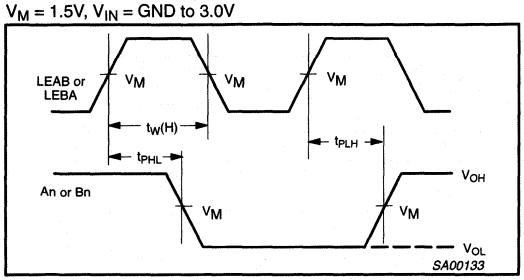
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



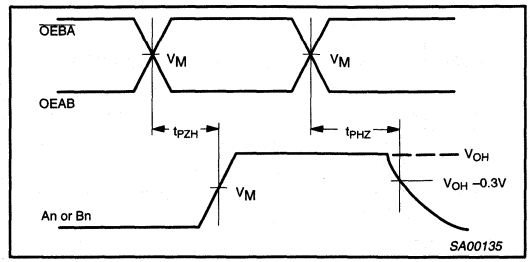
Waveform 2. Propagation Delay, Transparent Mode

AC WAVEFORMS (Continued)

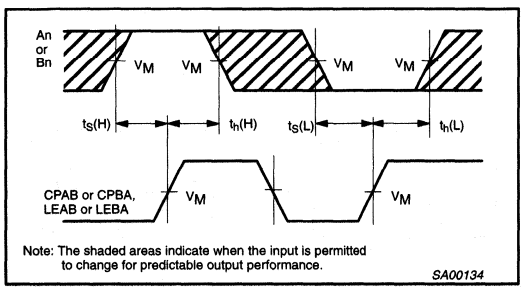
V_M = 1.5V, V_{IN} = GND to 3.0V



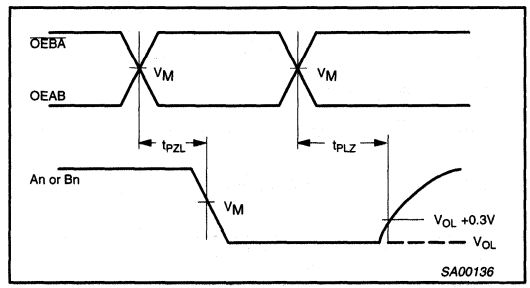
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

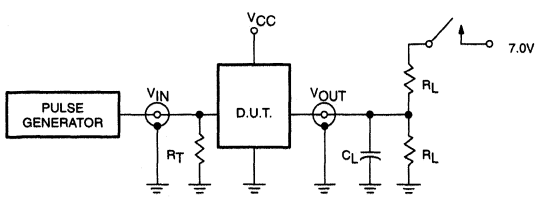


Waveform 4. Data Setup and Hold Times

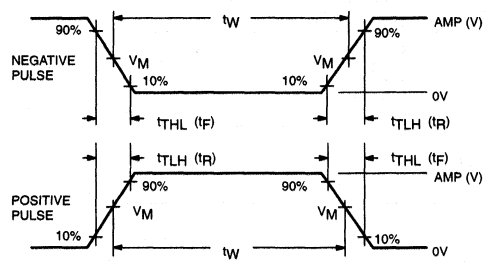


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

16-bit buffer/line driver (3-State)

74ABT16541
74ABTH16541

FEATURES

- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- Provides ideal interface and increases fan-out of MOS Microprocessors
- 3-State buffers sink 64mA and source 32mA
- 74ABTH16541 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Two 8-bit bus interfaces
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT16541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16541 has two octal buffers that are ideal for driving bus lines. The outputs are all capable of sinking 64mA and sourcing 32mA.

Two options are available, 74ABT16541 which does not have the bus-hold feature and 74ABTH16541 which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	2.0 1.5	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =5.5V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5V	8	mA

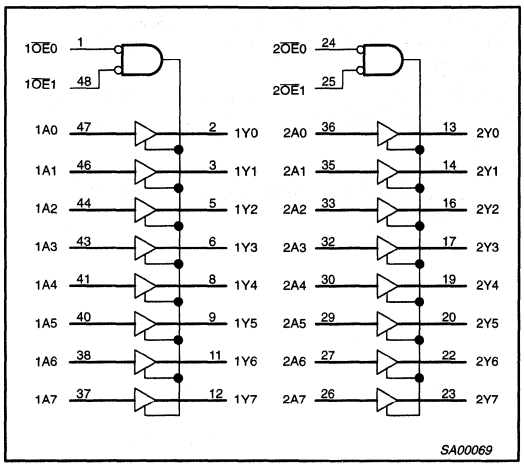
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16541 DL	BT16541 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16541 DGG	BT16541 DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16541 DL	BH16541 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16541 DGG	BH16541 DGG	SOT362-1

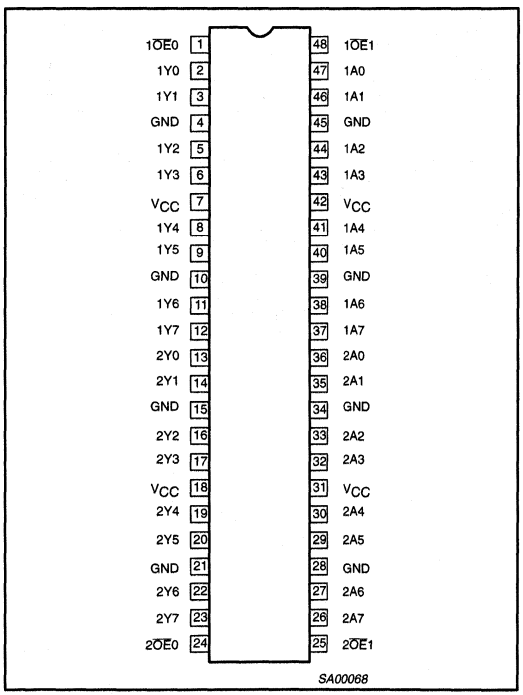
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0 - 1A7 2A0 - 2A7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17 19, 20, 22, 23	1Y0 - 1Y7, 2Y0 - 2Y7	Data outputs
1, 48 24, 25	$1\overline{OE}0$, $1\overline{OE}1$, $2\overline{OE}0$, $2\overline{OE}1$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

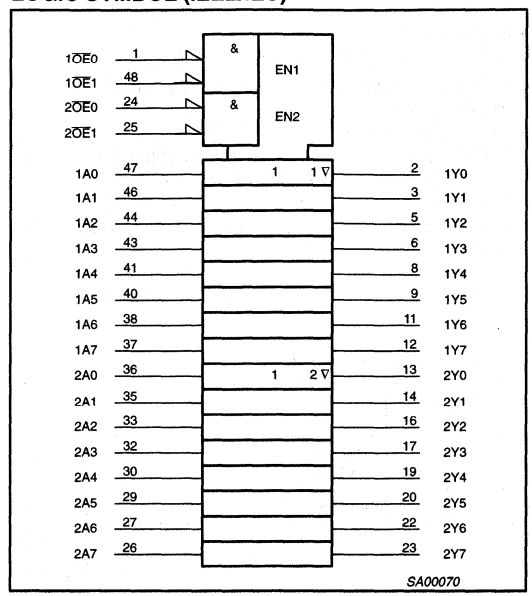
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS			OUTPUTS
$n\overline{OE}0$	$n\overline{OE}1$	nIx	nYx
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = D0n't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH16541	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0	Data pins		−2	−3		−5	µA
I_{HOLD}	Bus Hold current A inputs[3] 74ABTH16541	V_{CC} = 4.5V; V_I = 0.8V		50			50		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		µA
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			−1.0	−10		−10	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−70	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1.0		1.0	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1.0		1.0	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16541	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			100	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16541	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			0.2	1.0		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This is the bus hold overdrive current required to force the input to the opposite logic state.

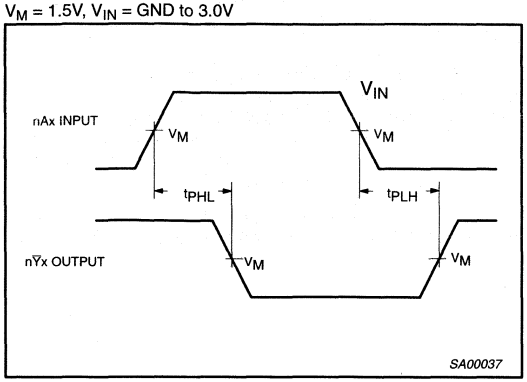
AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

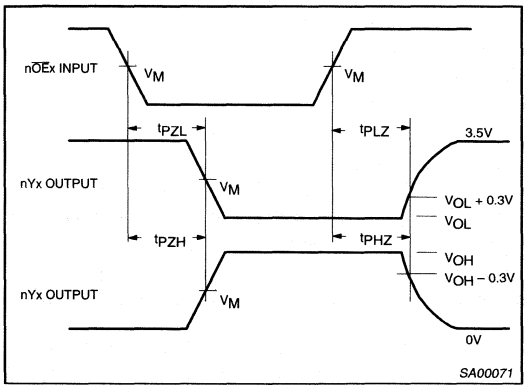
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nIx to nYx	1	1.0 1.0	2.0 1.5	3.0 3.6	1.0 1.0	3.4 4.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 1.6	2.9 3.1	4.3 4.7	1.3 1.6	5.2 6.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.3 1.0	3.5 2.8	4.4 3.6	1.3 1.0	5.1 3.9	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

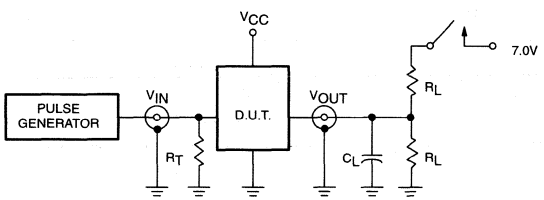


Waveform 1. Input (An) to Output (Yn) Propagation Delays

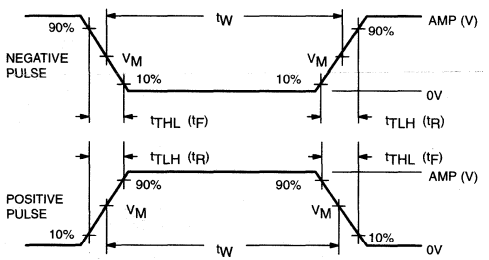


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

16-bit latched transceivers with dual enable (3-State)

74ABT16543
74ABTH16543

FEATURES

- Two 8-bit octal transceivers with D-type latch
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 74ABTH16543 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- See 74ABT161543 for same function with Master Reset control pins

DESCRIPTION

The 74ABT16543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16543 16-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($n\overline{LEAB}$, $n\overline{LEBA}$) and Output Enable ($n\overline{OEAB}$, $n\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

Two options are available, 74ABT16543 which does not have the bus-hold feature and 74ABTH16543 which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	2.5 2.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	550	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	9	mA

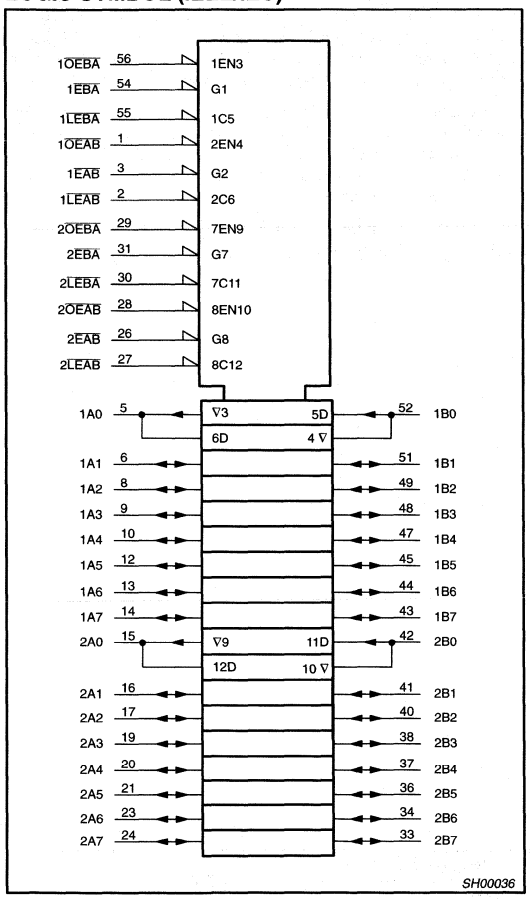
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16543 DL	BT16543 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16543 DGG	BT16543 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16543 DL	BH16543 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16543 DGG	BH16543 DGG	SOT364-1

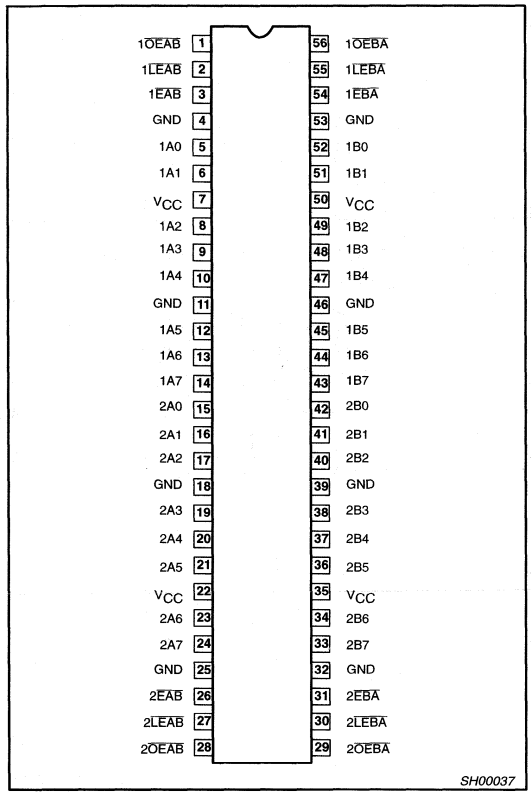
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs
1, 56 28, 29	$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	$1\overline{EAB}$, $1\overline{EBA}$, $2\overline{EAB}$, $2\overline{EBA}$	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	$1\overline{LEAB}$, $1\overline{LEBA}$, $2\overline{LEAB}$, $2\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

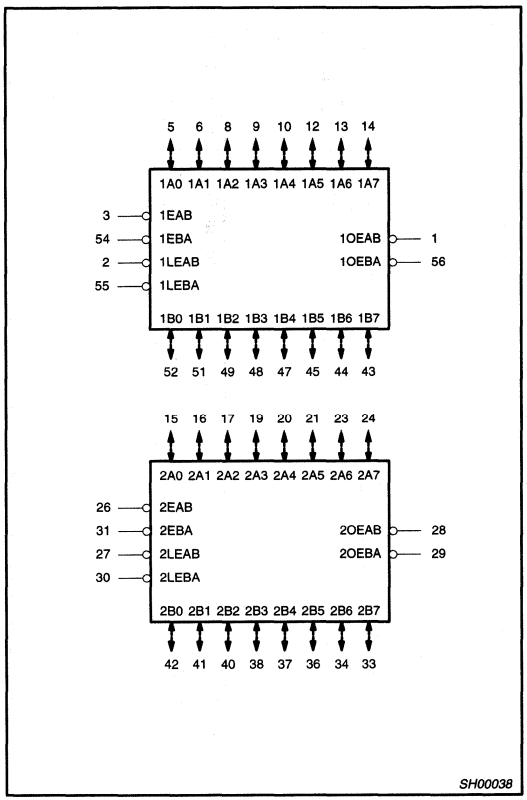
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The 74ABT16543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are Low the A-to-B path is transparent.

A subsequent Low-to-High transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $n\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

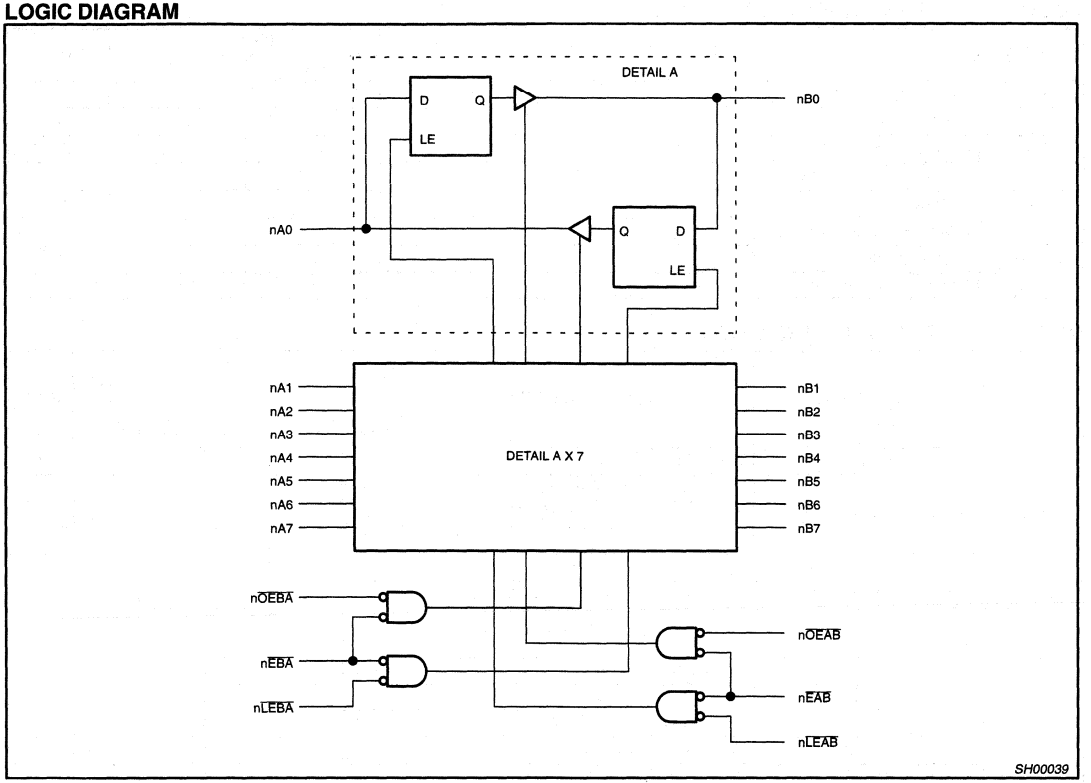
Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$n\overline{OEXX}$	$n\overline{EXX}$	$n\overline{LEXX}$	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	−64	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.36	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V (Control pins)		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A or B Ports[4] 74ABTH16543	V_{CC} = 4.5V; V_I = 0.8V	35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V	–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V	±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±2.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V or V_{CC}; V_I = GND or V_{CC}; V_{OE} = Don't care		±1.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		1.0	10		10	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–200	–50	–200	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.55	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.55	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16543	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		5.0	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16543	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		200	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, nBx to nAx	2	1.0 1.0	2.5 2.2	3.3 4.4	1.0 1.0	3.8 5.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to nAx, $\overline{LEAB}$ to nBx	1, 2	1.0 1.2	3.1 3.0	4.3 4.8	1.0 1.2	5.2 5.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to nAx, $\overline{OEAB}$ to nBx	4 5	1.0 1.1	3.3 3.3	4.3 5.9	1.0 1.1	5.2 7.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to nAx, $\overline{OEAB}$ to nBx	4 5	1.9 1.6	3.5 2.6	5.0 4.2	1.9 1.6	5.7 4.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to nAx, $\overline{EAB}$ to nBx	4 5	1.0 1.2	3.4 3.4	4.9 6.5	1.0 1.2	6.2 7.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to nAx, $\overline{EAB}$ to nBx	4 5	2.0 1.7	3.4 2.6	5.6 5.1	2.0 1.7	6.6 5.4	ns

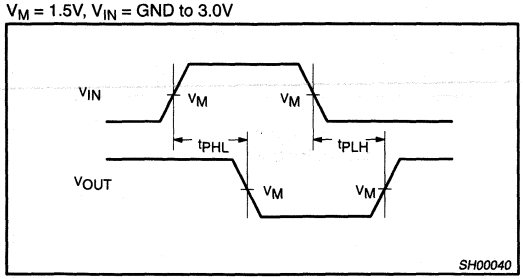
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

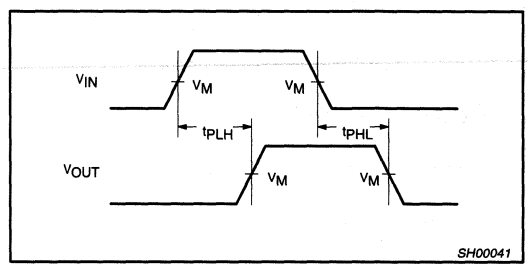
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time nAx to $\overline{LEAB}$, nBx to $\overline{LEBA}$	3	1.5 3.5	0.4 –0.1	1.5 3.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to $\overline{LEAB}$, nBx to $\overline{LEBA}$	3	1.5 2.0	0.2 –0.3	1.5 2.0	ns
$t_s(H)$ $t_s(L)$	Setup time nAx to $\overline{EAB}$, nBx to $\overline{EBA}$	3	1.5 3.5	0.2 –0.3	1.5 3.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to $\overline{EAB}$, nBx to $\overline{EBA}$	3	1.5 2.0	0.3 –0.2	1.5 2.0	ns
$t_w(L)$	Latch enable pulse width, Low	3	4.0	3.1	4.0	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V



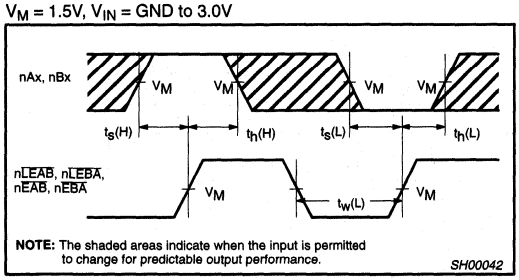
Waveform 1. Propagation Delay For Inverting Output



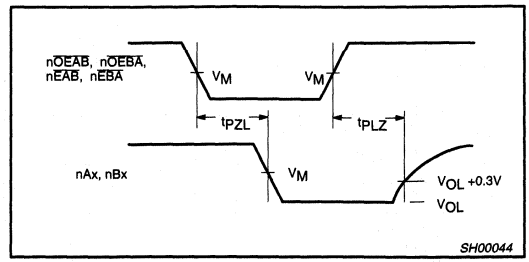
Waveform 2. Propagation Delay For Non-Inverting Output

AC WAVEFORMS (Continued)

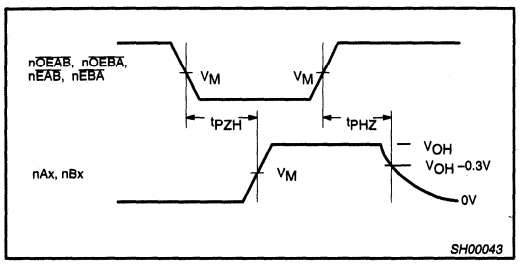
V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width

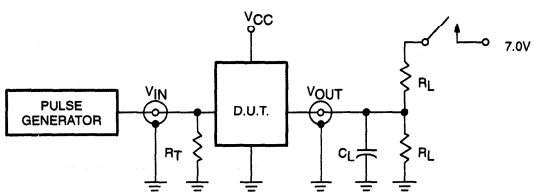


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

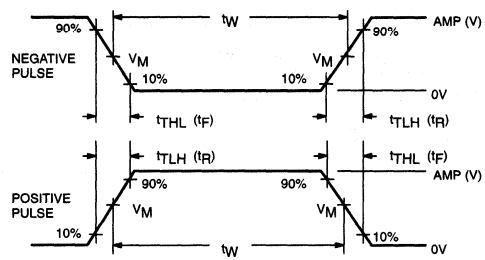


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

16-bit latched transceiver with dual enable and master reset (3-State)

74ABT161543
74ABTH161543

FEATURES

- Two 8-bit octal transceivers with D-type latch
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 74ABTH161543 incorporates Bus hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same function as ABT16543 except for additional Master Reset control pins

DESCRIPTION

The 74ABT161543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT161543 16-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (n$\overline{LEAB}$, n$\overline{LEBA}$) and Output Enable (n$\overline{OEAB}$, n$\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. Master reset ($\overline{MR}$) clears all registers simultaneously and sets them Low. The outputs are guaranteed to sink 64mA.

Two options are available, 74ABT161543 which does not have the Bus hold feature and 74ABTH161543 which inorporates the Bus hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	2.5 2.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-pin plastic SSOP Type III	–40°C to +85°C	BT161543DL	SOT371-1
56-pin plastic TSSOP Type II	–40°C to +85°C	BT161543DGG	SOT364-1

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT161543 DL	BT161543 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT161543 DGG	BT161543 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH161543 DL	BH161543 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH161543 DGG	BH161543 DGG	SOT364-1

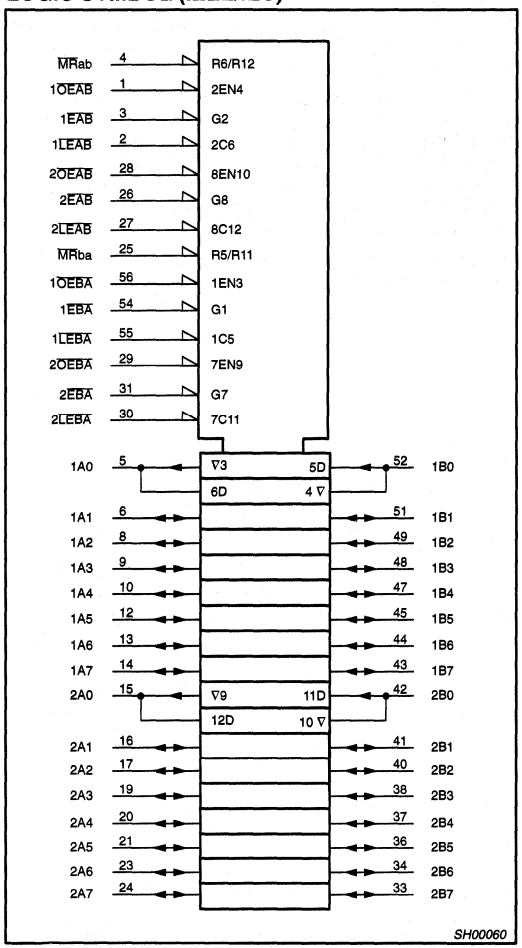
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs
1, 56 28, 29	1$\overline{OEAB}$, 1$\overline{OEBA}$, 2$\overline{OEAB}$, 2$\overline{OEBA}$	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	1$\overline{EAB}$, 1$\overline{EBA}$, 2$\overline{EAB}$, 2$\overline{EBA}$	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	1$\overline{LEAB}$, 1$\overline{LEBA}$, 2$\overline{LEAB}$, 2$\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-Low)
4, 25	$\overline{MR}$ab, $\overline{MR}$ba	Master reset
11, 18, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

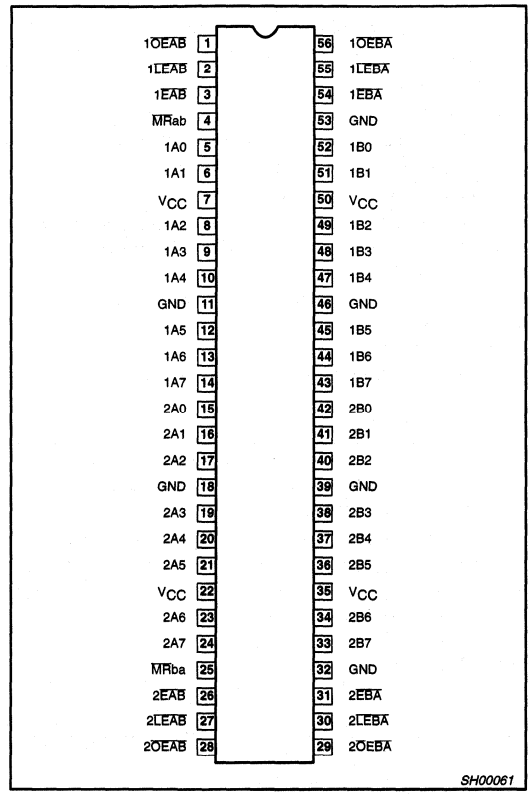
16-bit latched transceiver with dual enable and master reset (3-State)

74ABT161543
74ABTH161543

LOGIC SYMBOL (IEEE/IEC)



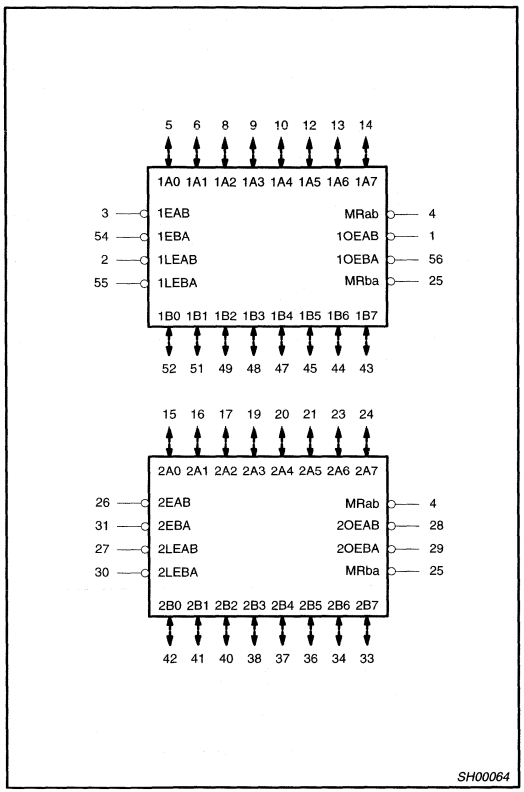
PIN CONFIGURATION



16-bit latched transceiver with dual enable and master reset (3-State)

74ABT161543
74ABTH161543

LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The 74ABT161543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are Low the A-to-B path is transparent.

A subsequent Low-to-High transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $n\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

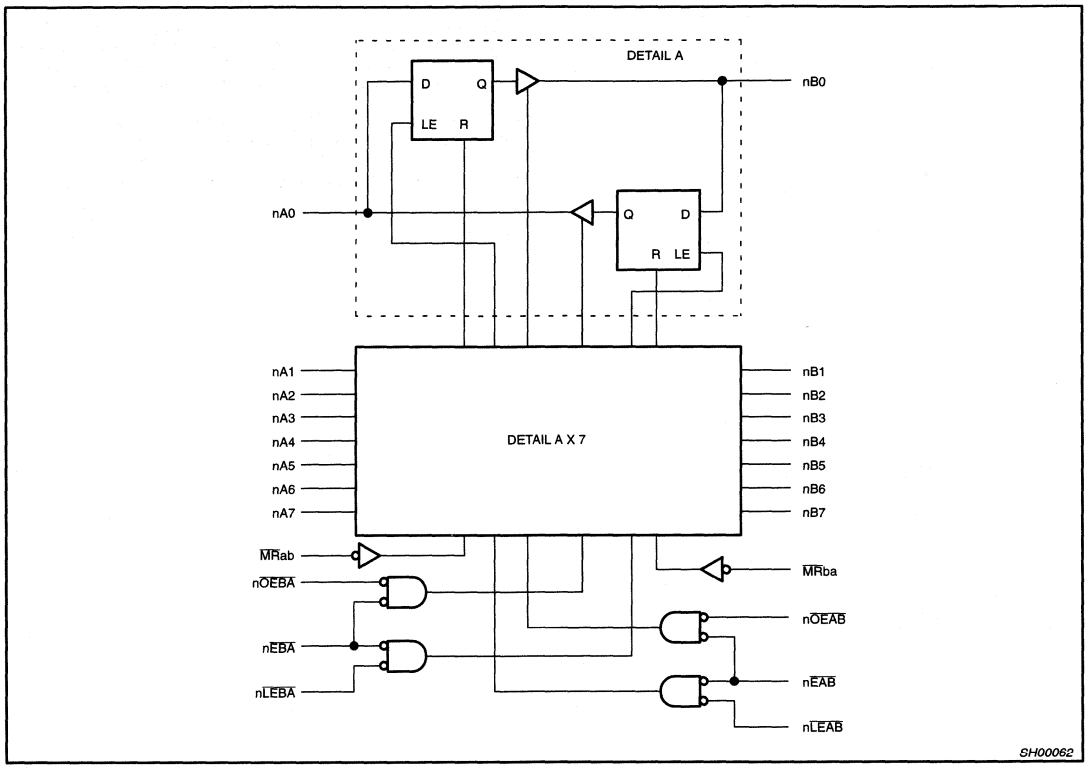
Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

FUNCTION TABLE

INPUTS					OUTPUTS	STATUS
$n\overline{OEXX}$	$n\overline{MRXX}$	$n\overline{EXX}$	$n\overline{LEXX}$	nAx or nBx	nBx or nAx	
L	L	L	X	X	L	Clear
H	X	X	X	X	Z	Disabled
X	X	H	X	X	Z	Disabled
L L	H H	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	H H	L L	↑ ↑	h l	H L	Latch + Display
L L	H H	L L	L L	H L	H L	Transparent
L	H	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	−64	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA				–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		2.5	3.0		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		3.0	3.6		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}		2.0	2.7		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.36	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V	Control pins		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A or B Ports[4] 74ABTH161543	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V			±1.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V or V_{CC}; V_I = GND or V_{CC}; V_{OE} = Don't care			±1.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}			1.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}			–1.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–100	–200	–50	–200	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.50	1.5		1.5	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}			0.50	1.5		1.5	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT161543	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			5.0	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH161543	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.20	1		1	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, nBx to nAx	2	1.2 1.0	2.5 2.2	3.4 2.9	1.2 1.0	3.9 3.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to nAx, $\overline{LEAB}$ to nBx	1 2	1.2 1.2	3.0 2.6	4.1 3.5	1.2 1.2	5.1 4.1	ns
t_{PHL}	$\overline{MR}$ba to nAx, $\overline{MR}$ab to nBx	6	1.2	2.6	3.4	1.2	4.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to nAx, $\overline{OEAB}$ to nBx	4 5	1.4 1.4	3.3 3.4	4.4 4.4	1.4 1.4	5.5 5.6	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to nAx, $\overline{OEAB}$ to nBx	4 5	1.4 1.4	3.5 2.7	4.8 3.5	1.4 1.4	5.4 4.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to nAx, $\overline{EAB}$ to nBx	4 5	1.4 1.4	3.4 3.5	4.4 4.4	1.4 1.4	5.6 5.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to nAx, $\overline{EAB}$ to nBx	4 5	1.3 1.3	3.5 2.7	4.4 3.5	1.3 1.3	5.4 4.0	ns

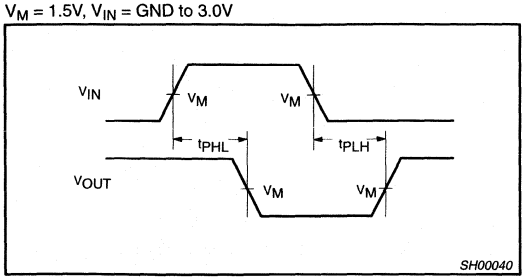
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

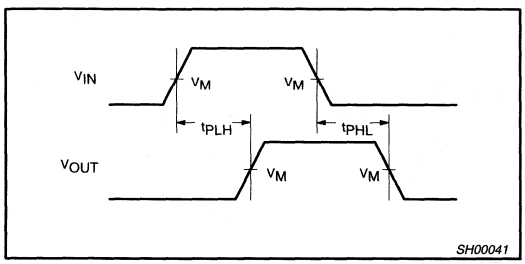
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time nAx to $\overline{LEAB}$, nBx to $\overline{LEBA}$	3	1.5 2.0	–0.3 0.1	1.5 2.0	ns
t_h(H) t_h(L)	Hold time nAx to $\overline{LEAB}$, nBx to $\overline{LEBA}$	3	1.5 2.0	–0.1 0.1	1.5 2.0	ns
t_s(H) t_s(L)	Setup time nAx to $\overline{EAB}$, nBx to $\overline{EBA}$	3	1.5 2.0	–0.1 0.2	1.5 2.0	ns
t_h(H) t_h(L)	Hold time nAx to $\overline{EAB}$, nBx to $\overline{EBA}$	3	1.5 2.0	–0.1 –0.1	1.5 2.0	ns
t_w(L)	Latch enable pulse width, Low	3	4.0	2.0	4.0	ns
t_w(L)	$\overline{MR}$ Pulse width, Low	6	3.0	1.0	3.0	ns

AC WAVEFORMS

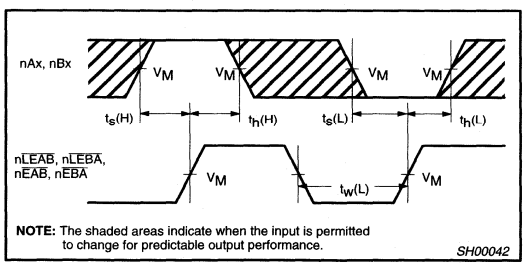
V_M = 1.5V, V_{IN} = GND to 3.0V



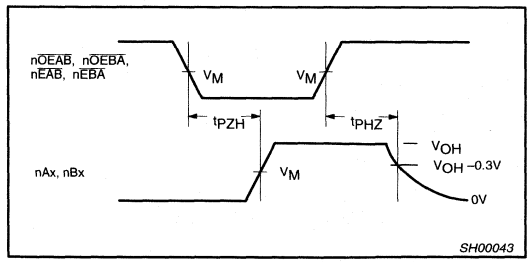
Waveform 1. Propagation Delay For Inverting Output



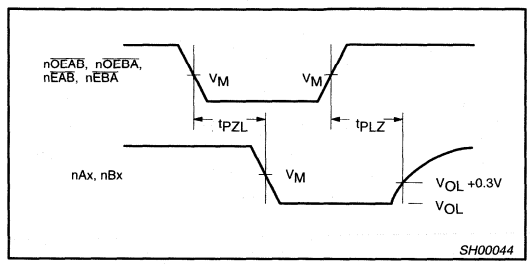
Waveform 2. Propagation Delay For Non-Inverting Output



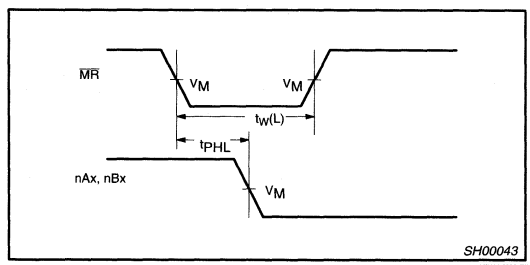
Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

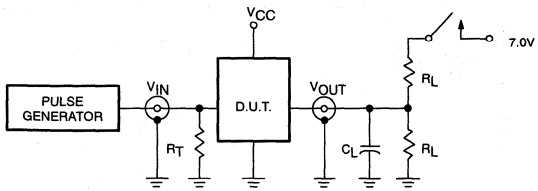


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

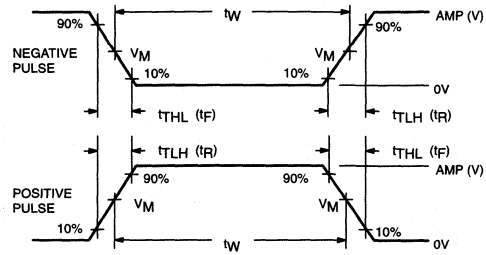


Waveform 6. Master Reset Pulse Width, Master Reset to Output Delay

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

16-bit bus transceiver/register (3-State)

74ABT16646
74ABTH16646

FEATURES

- Independent registers for A and B buses
- Multiple Vcc and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power–up 3-State
- Power–up reset
- Multiplexed real-time and stored data
- Outputs sink 64mA and source 32mA
- Latch–up protection exceeds 500mA per JEDEC Std 17
- 74ABTH16646 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16646 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16646 16-bit transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($n\overline{OE}$) and Direction (nDIR) pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (nSAB, nSBA) pins determine whether data is stored or transferred through the device in real-time. The nDIR determines which bus will receive data when the $n\overline{OE}$ is active Low. In the isolation mode ($n\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

Two options are available, 74ABT16646 which does not have the bus-hold feature and 74ABTH16646 which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	3.3 2.7	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =5.5V	550	µA
		Outputs low; V_{CC} =5.5V	9	mA

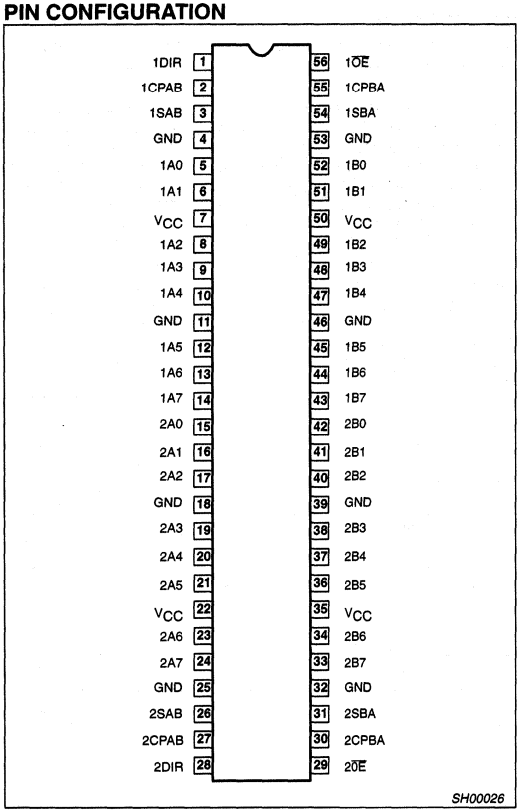
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16646 DL	BT16646 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16646 DGG	BT16646 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16646 DL	BH16646 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16646 DGG	BH16646 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
1, 28	1DIR, 2DIR	Direction control inputs
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
56, 29	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION

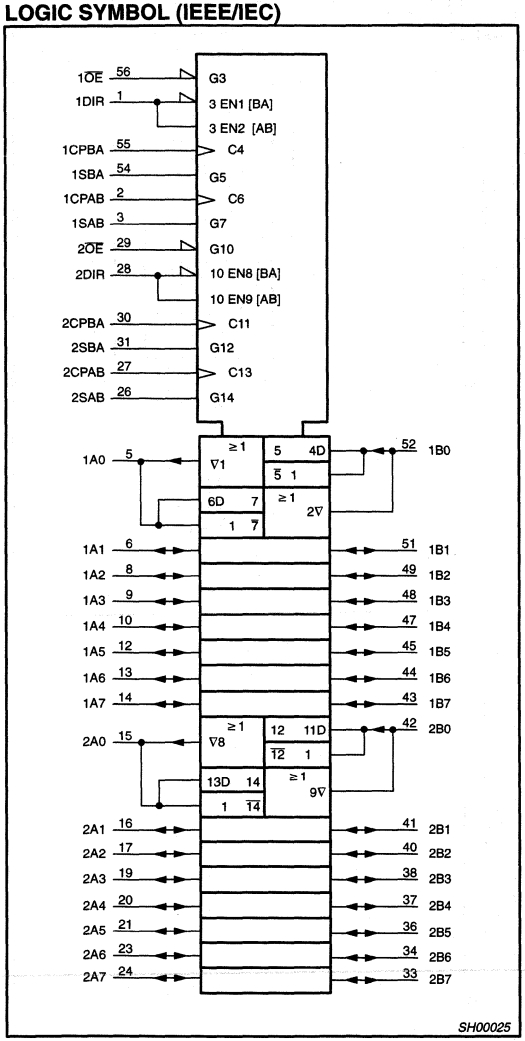


FUNCTION TABLE

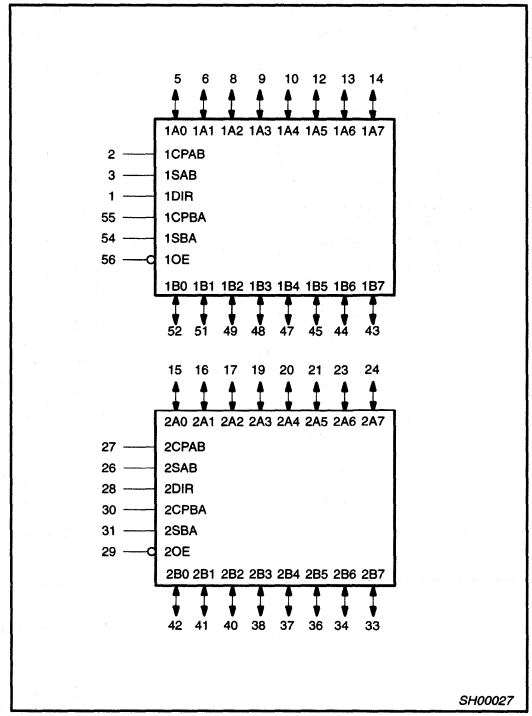
INPUTS						DATA I/O		OPERATING MODE
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $n\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low–to–High transition of the clock.

LOGIC SYMBOL (IEEE/IEC)

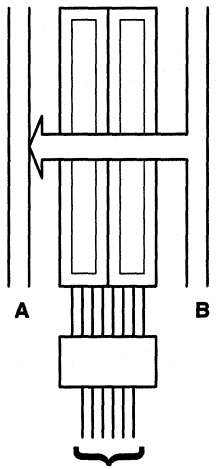


LOGIC SYMBOL



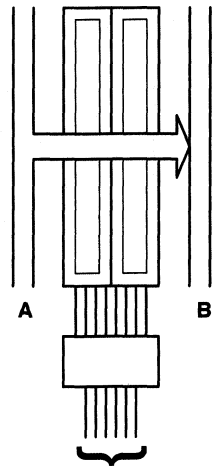
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT16646.

REAL TIME BUS TRANSFER BUS B TO BUS A



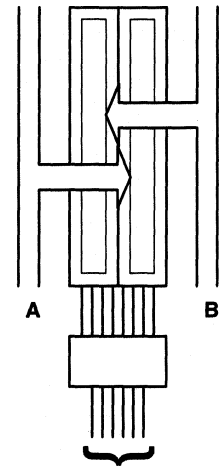
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



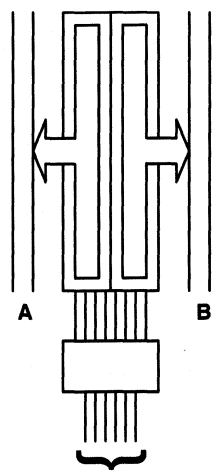
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	↑	X	X	X
L	L	X	↑	X	X
H	X	↑	↑	X	X

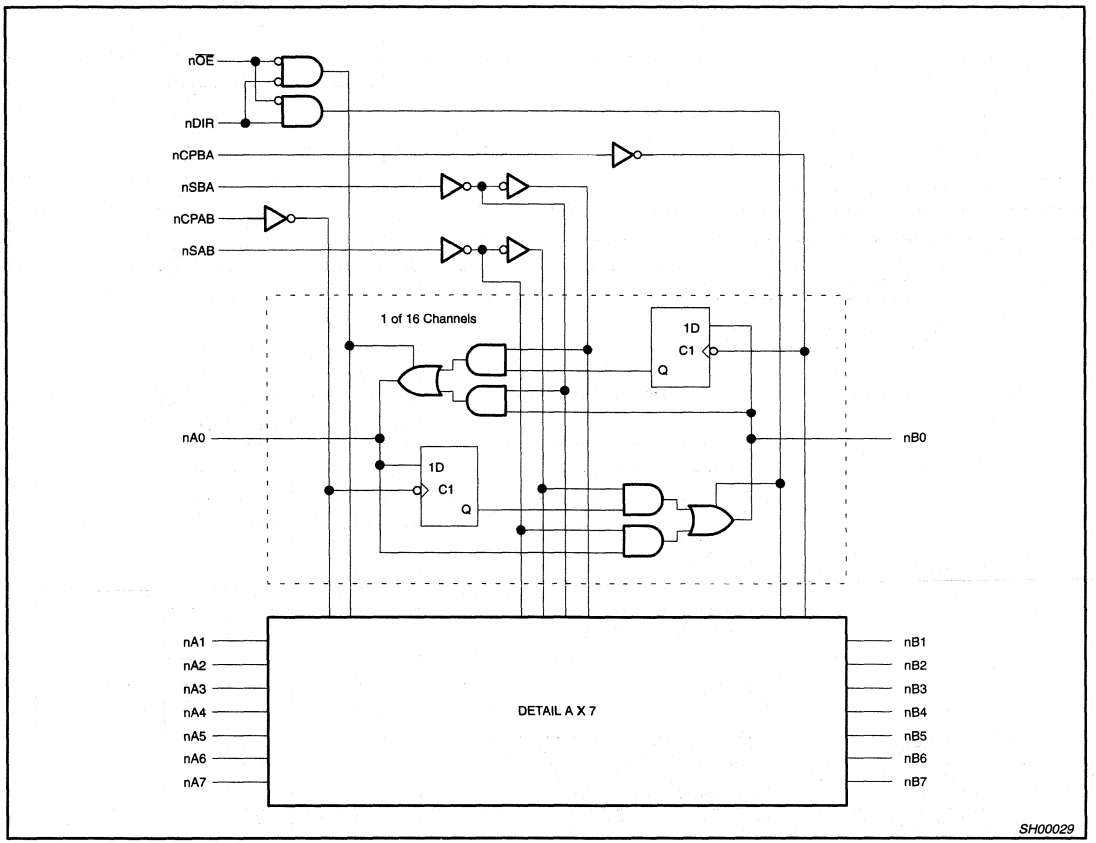
TRANSFER STORED DATA TO A OR B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

SH00028

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	−64	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.35	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V; Control pins		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A or B Ports[4] 74ABTH16646	V_{CC} = 4.5V; V_I = 0.8V	35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V	–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V	±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O = 4.5V; V_I = 0.0V or 5.5V		±2.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V or V_{CC}; V_I = GND or V_{CC}; OE/$\overline{OE}$ = X		±1.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		1.0	10		10	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.55	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.55	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16646	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		5.0	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16646	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		200	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.0V, with a transition time of up to 100msec. From V_{CC} = 21.V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	125			125		MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.5 1.5	3.3 2.7	4.0 4.1	1.5 1.5	4.9 4.7	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.0 1.0	2.3 2.0	3.2 4.1	1.0 1.0	3.9 4.6	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	2, 3	1.0 1.0	3.1 2.7	4.3 4.3	1.0 1.0	5.0 5.0	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OE}$ to nAx or nBx	5, 6	1.0 1.5	3.2 3.3	4.6 4.9	1.0 1.5	5.5 5.7	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OE}$ to nAx or nBx	5, 6	1.5 1.5	3.5 2.7	4.9 4.1	1.5 1.5	5.4 4.5	ns
t_{PZH} t_{PZL}	Output enable time nDIR to nAx or nBx	5, 6	1.0 1.5	4.1 4.3	4.8 4.8	1.0 1.5	5.4 5.6	ns
t_{PHZ} t_{PLZ}	Output disable time nDIR to nAx or nBx	5, 6	2.0 1.5	3.6 2.7	5.7 5.1	2.0 1.5	6.7 5.9	ns

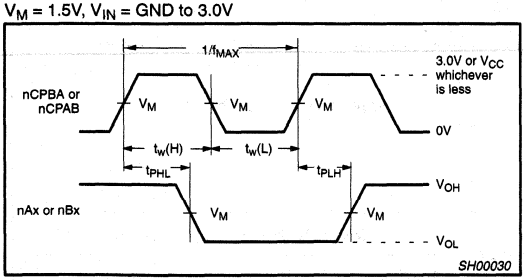
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

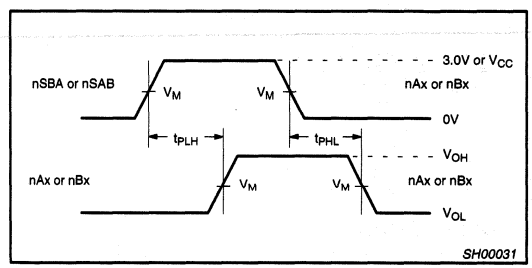
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time nAx to nCPAB, nBx to nCPBA	4	2.0 1.5	1.0 0.8	2.0 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nCPAB, nBx to nCPBA	4	1.5 1.0	0.0 –0.7	1.5 1.0	ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low nCPAB or nCPBA	1	4.5 3.0	2.5 2.0	4.5 3.0	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V



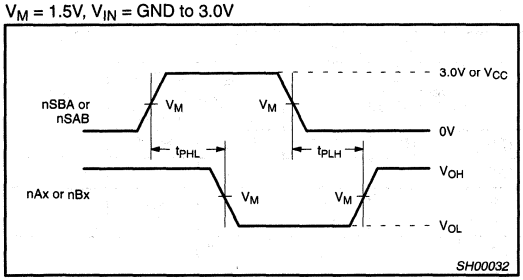
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



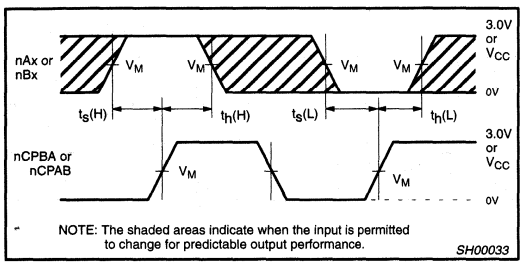
Waveform 2. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx

AC WAVEFORMS (Continued)

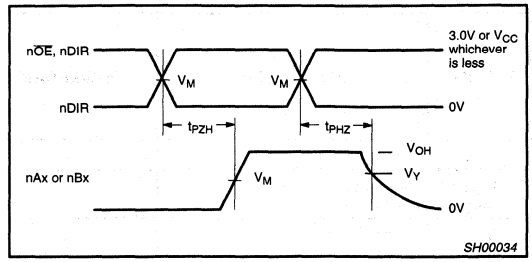
V_M = 1.5V, V_{IN} = GND to 3.0V



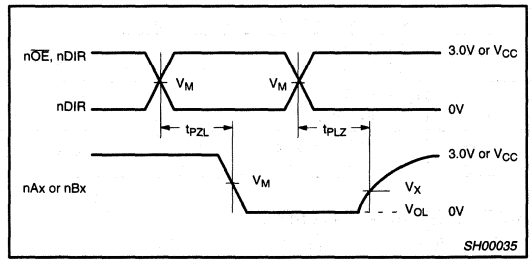
Waveform 3. Propagation Delay, nSBA to nAx or nSAB to nBx



Waveform 4. Data Setup and Hold Times

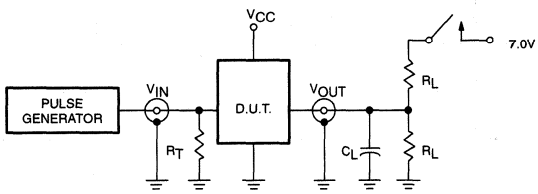


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

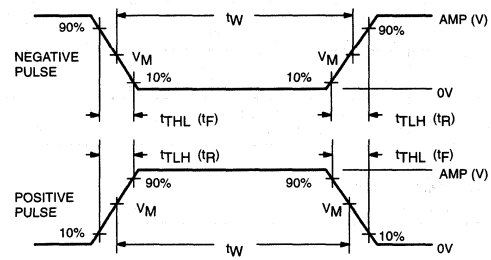


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

16-bit transceiver/register, non-inverting (3-State)

74ABT16652
74ABTH16652

FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- 74ABTH16652 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Live insertion/extraction permitted
- Multiplexed real-time and stored data
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16652 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16652 transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes HIGH. Output Enable (nOEAB, ($n\overline{OEBA}$) and Select ($n\overline{SAB}$, $n\overline{SBA}$) pins are provided for bus management.

Two options are available, 74ABT16652 which does not have the bus-hold feature and 74ABTH16652 which incorporates the bus-hold feature.

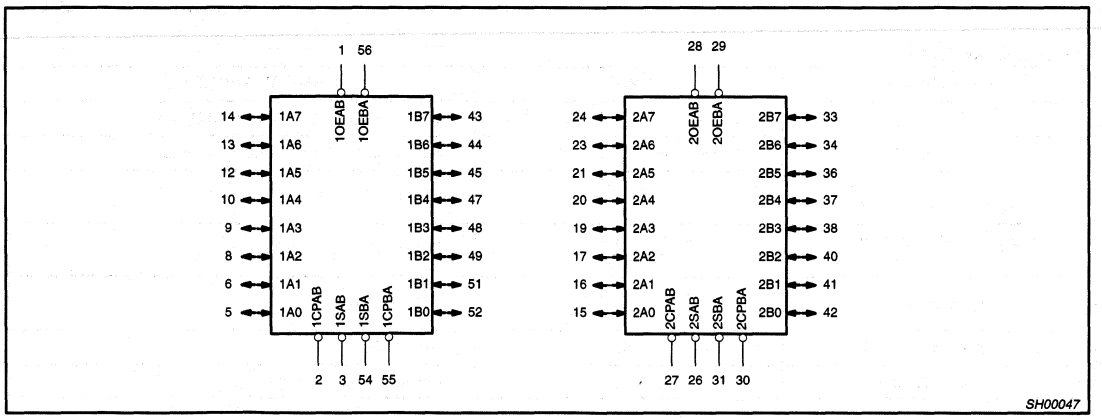
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	2.3 1.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =5.5V	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16652 DL	BT16652 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16652 DGG	BT16652 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16652 DL	BH16652 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16652 DGG	BH16652 DGG	SOT364-1

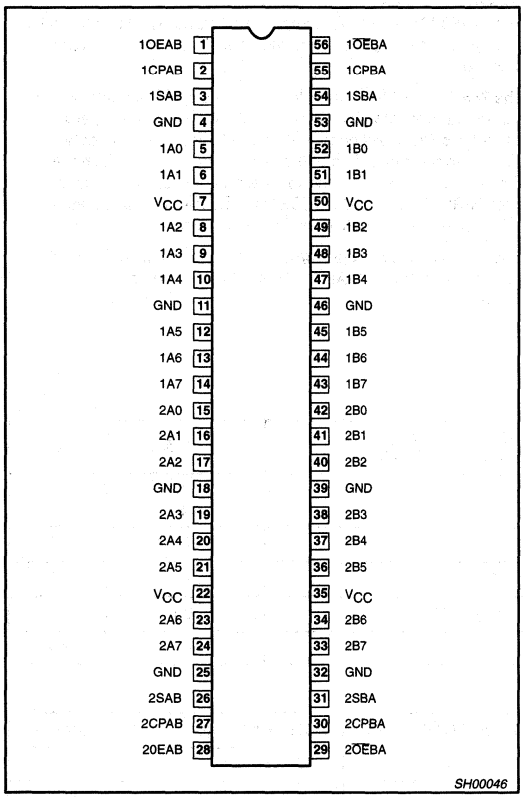
LOGIC SYMBOL



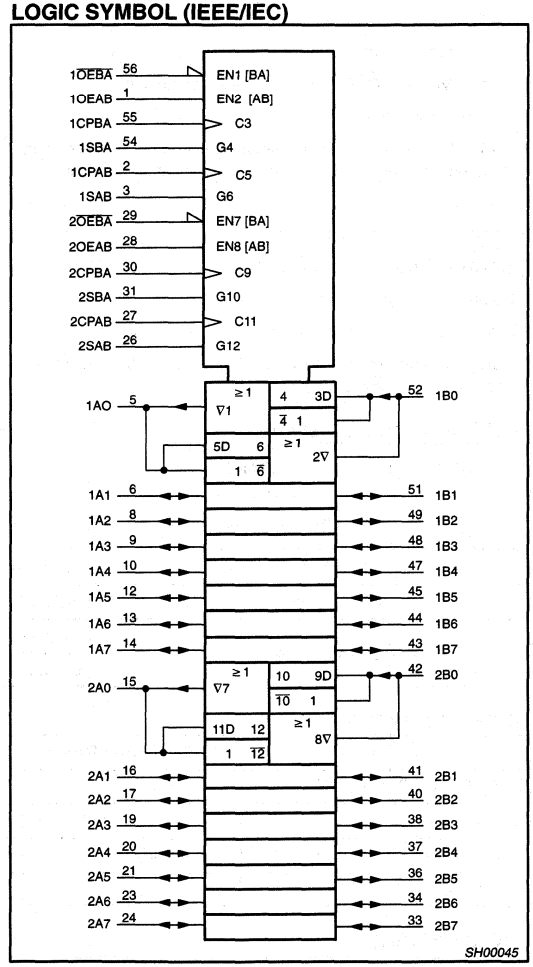
16-bit transceiver/register, non-inverting (3-State)

74ABT16652
74ABTH16652

PIN CONFIGURATION



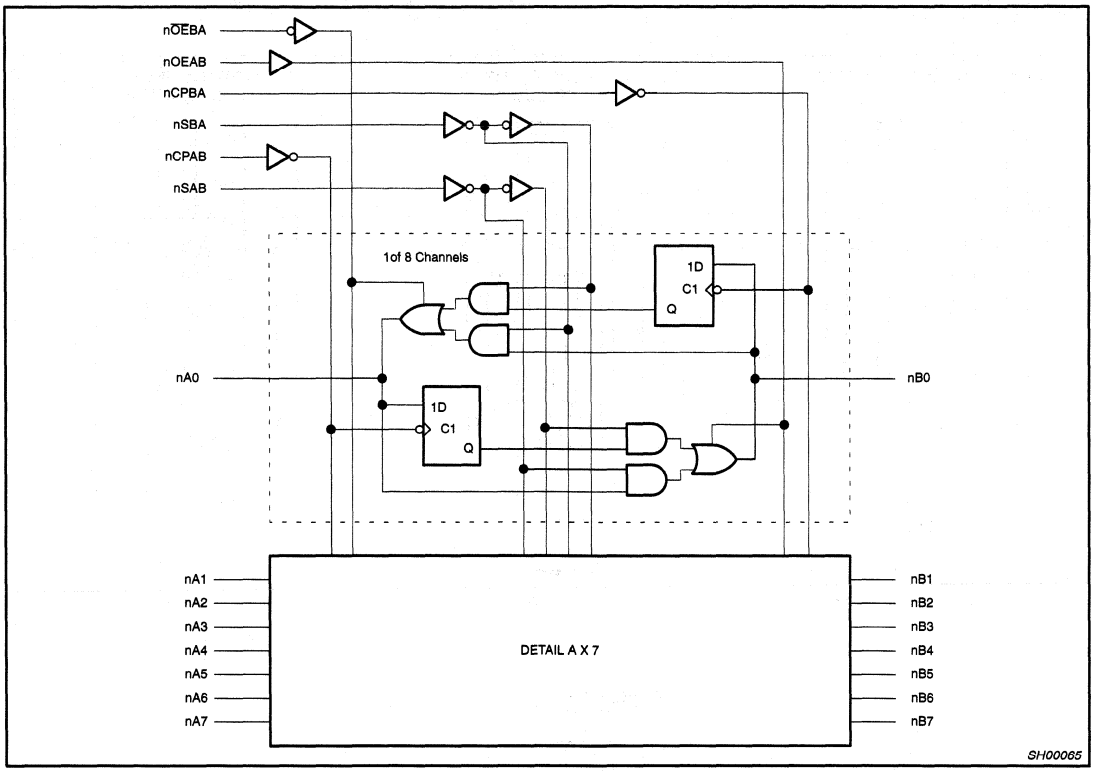
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
1, 56, 28, 29	1OEAB, 1$\overline{\text{OEBA}}$, 2OEAB, 2$\overline{\text{OEBA}}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



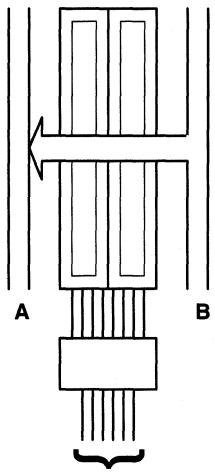
FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOEBA and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (nSAB and nSBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

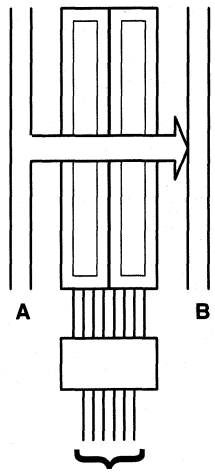
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT16652.The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

REAL TIME BUS TRANSFER BUS B TO BUS A



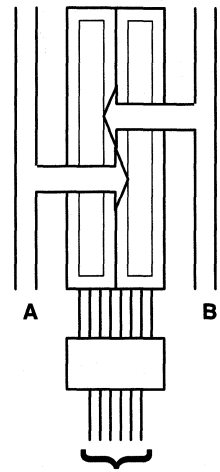
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



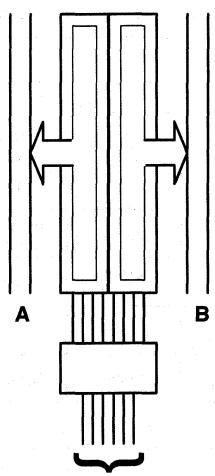
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
H	L	H/L	H/L	H	H

SH00066

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
		output in HIGH state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	4.0		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.35	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_{OL} = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or V_{CC}	Control pins		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A or B Ports[4] 74ABTH16652	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0V; V_O = 4.5V; V_I = 0V or 5.5V			±1.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V; V_I = GND or V_{CC}			±1.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}			−1.0	−10		−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{cc}			5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−80	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16652	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			5.0	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16652	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			200	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0 and 2.1V. When the part enables with V_{CC} between 2.1V and 4.5V, the outputs will correctly function with respect to all input logic states.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	125			125		MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.5 1.5	3.3 2.8	4.0 4.1	1.5 1.5	4.9 4.7	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.0 1.0	2.3 1.8	3.2 4.1	1.0 1.0	3.9 4.6	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	3	1.0 1.0	3.4 2.6	4.3 4.3	1.0 1.0	5.0 5.0	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OEBA}$ to nAx	5 6	1.0 1.5	2.5 2.2	4.1 4.4	1.0 1.5	5.0 5.3	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OEBA}$ to nAx	5 6	1.5 1.5	3.6 2.7	4.4 3.6	1.5 1.5	4.9 4.0	ns
t_{PZH} t_{PZL}	Output enable time nOEAB to nBx	5 6	1.0 1.5	2.9 3.0	3.6 3.9	1.0 1.5	4.2 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time nOEAB to nBx	5 6	2.0 1.5	3.1 2.3	5.5 4.5	2.0 1.5	5.9 5.2	ns

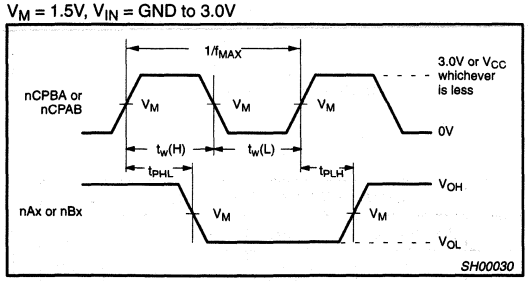
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

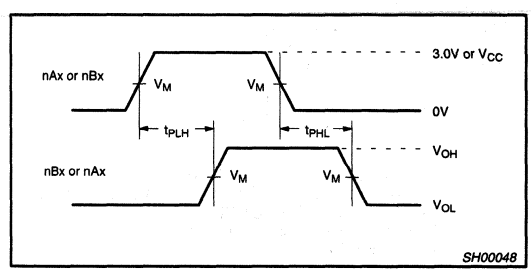
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time nAx to nCPBA, nBx to nCPAB	4	3.0 3.0	1.2 0.8	3.0 3.0	ns
t_h(H) t_h(L)	Hold time nAx to nCPBA, nBx to nCPAB	4	1.0 1.0	–0.7 –1.1	1.0 1.0	ns
t_w(H) t_w(L)	Pulse width, High or Low nCPAB or nCPBA	1	4.3 4.3	1.0 1.0	4.3 4.3	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V



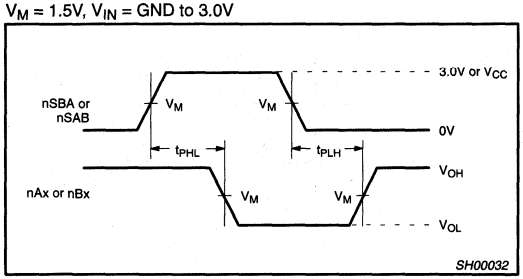
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



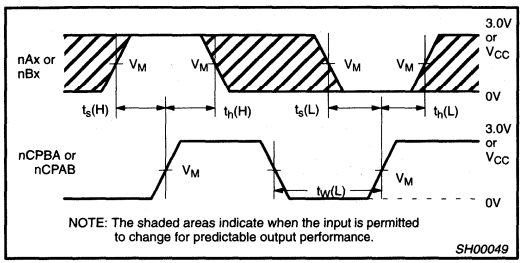
Waveform 2. Propagation Delay, nAx to nBx or nBx to nAx

AC WAVEFORMS (Continued)

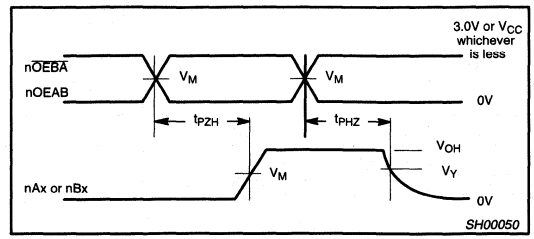
V_M = 1.5V, V_{IN} = GND to 3.0V



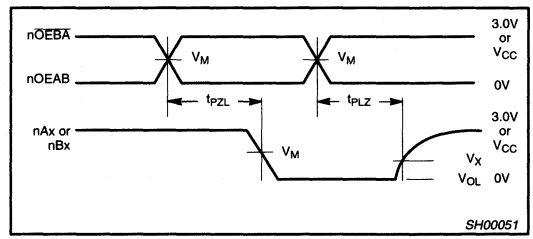
Waveform 3. Propagation Delay, SBA to nAx or SAB to nBx



Waveform 4. Data Setup and Hold Times

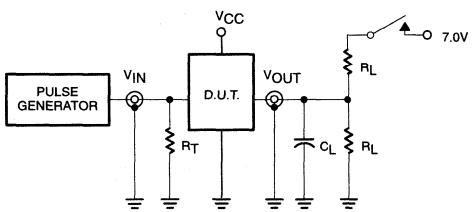


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

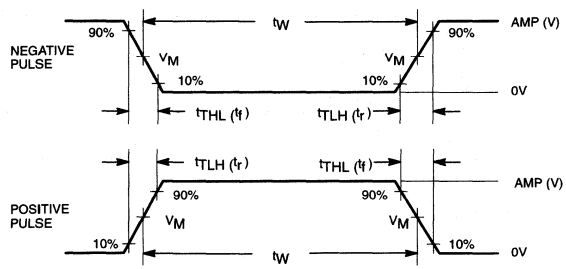


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00022

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

FEATURES

- 20-bit positive-edge triggered register
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- 74ABTH16821A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16821A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16821A has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($n\overline{OE}$) controls all ten 3-State buffers independent of the register operation. When $n\overline{OE}$ is Low, the data in the register appears at the outputs. When $n\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

Two options are available, 74ABT16821A which does not have the bus-hold feature and 74ABTH16821A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	2.4 2.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5V	10	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16821A DL	BT16821A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16821A DGG	BT16821A DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16821A DL	BH16821A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16821A DGG	BH16821A DGG	SOT364-1

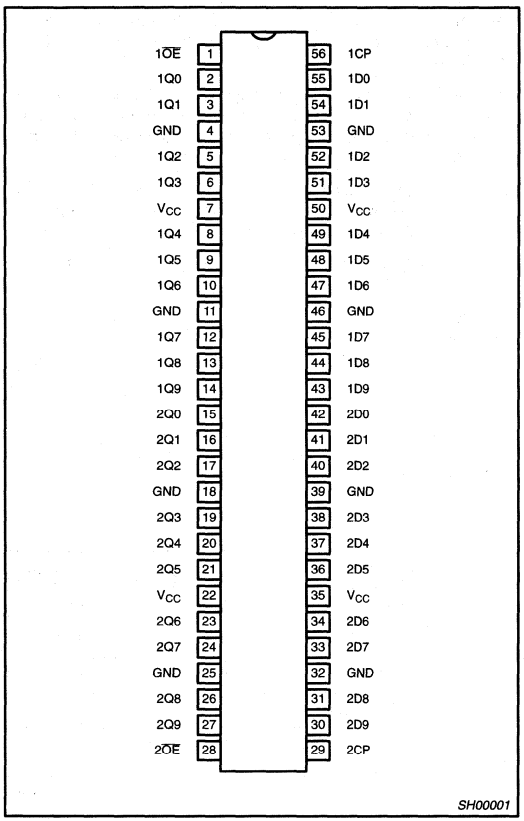
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 - 1D9 2D0 - 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 - 1Q9 2Q0 - 2Q9	Data outputs
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

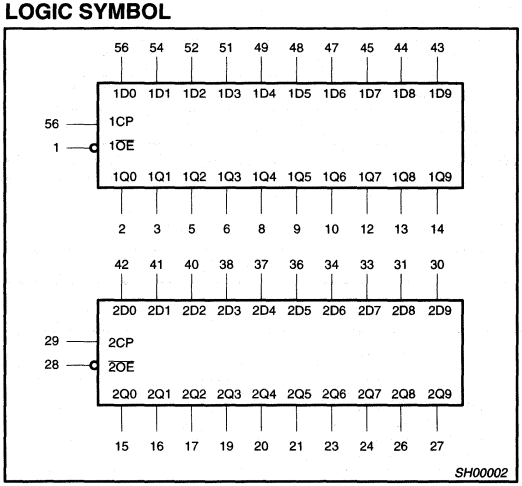
20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

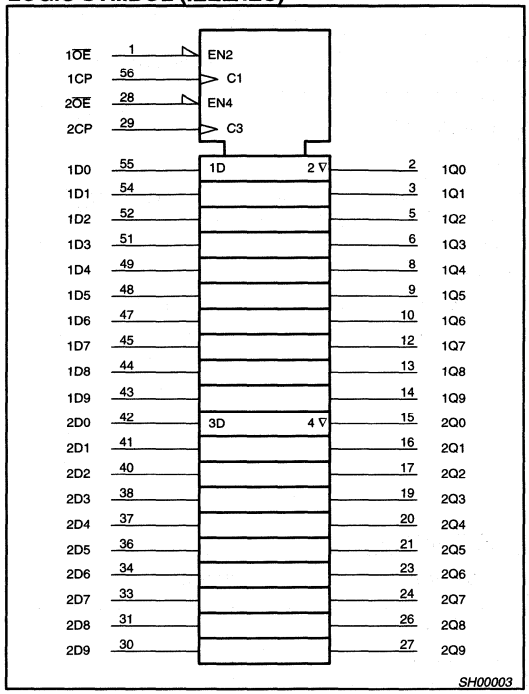
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

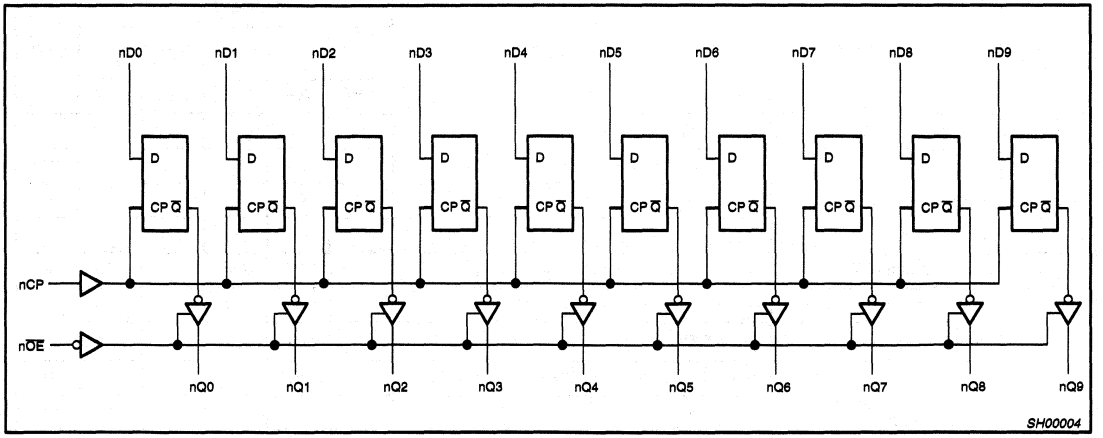


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
n$\overline{OE}$	nCP	nDx		nQ0 - nQ9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.36	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH16821A	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0	Data pins		−1	−3		−5	µA
I_{HOLD}	Bus Hold current inputs[4] 74ABTH16821A	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		µA
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V			±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			−1.0	−10		−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−90	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			10	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.25	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

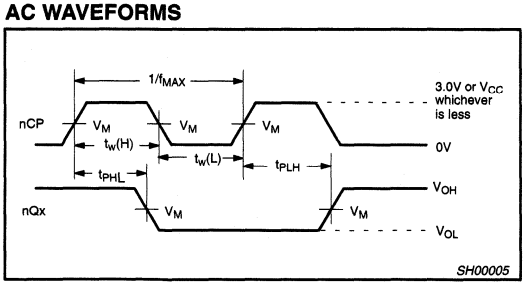
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	160	250		160		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.3 1.1	2.4 2.0	3.3 2.6	1.3 1.1	3.7 3.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.4 1.2	2.5 2.3	3.3 3.0	1.4 1.2	4.1 3.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.6 1.3	3.2 2.3	4.1 3.1	1.6 1.3	4.8 3.3	ns

AC SETUP REQUIREMENTS

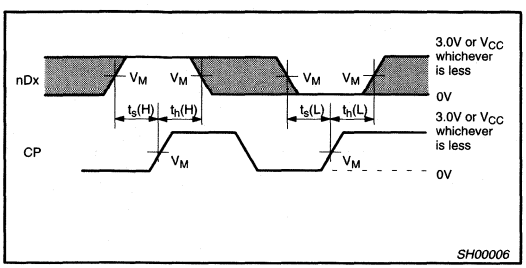
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nCP	2	1.8 1.8	1.2 −0.9	1.8 1.8		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	2	1.0 1.0	0.8 −1.0	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	nCP pulse width High or Low	1	2.5 2.5	0.8 1.0	2.5 2.5		ns

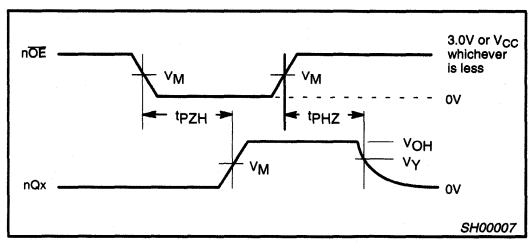
AC WAVEFORMS



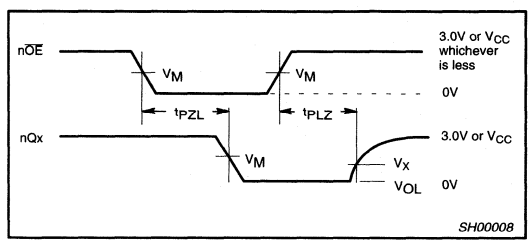
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock frequency



Waveform 2. Data Setup and Hold Times

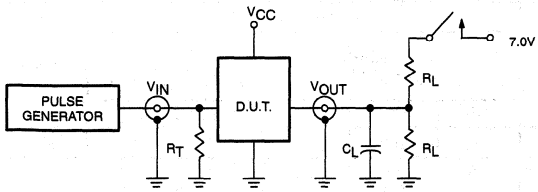


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

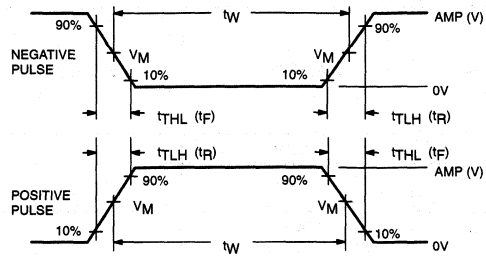


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ABT16823A
74ABTH16823A

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16823A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up Reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16823A 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16823A has two 9-bit wide buffered registers with Clock Enable ($n\overline{CE}$) and Master Reset ($n\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

Two options are available, 74ABT16823A which does not have the bus-hold feature and 74ABTH16823A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	2.3 1.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

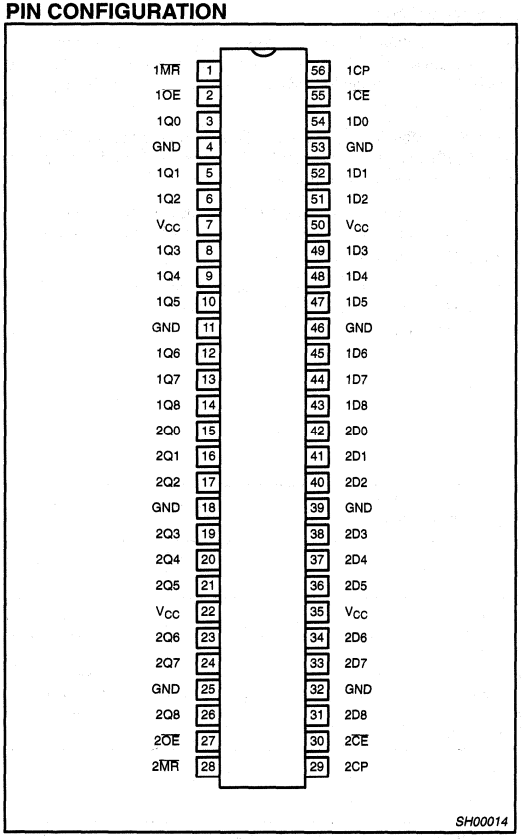
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16823A DL	BT16823A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16823A DGG	BT16823A DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16823A DL	BH16823A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16823A DGG	BH16823A DGG	SOT364-1

PIN DESCRIPTION

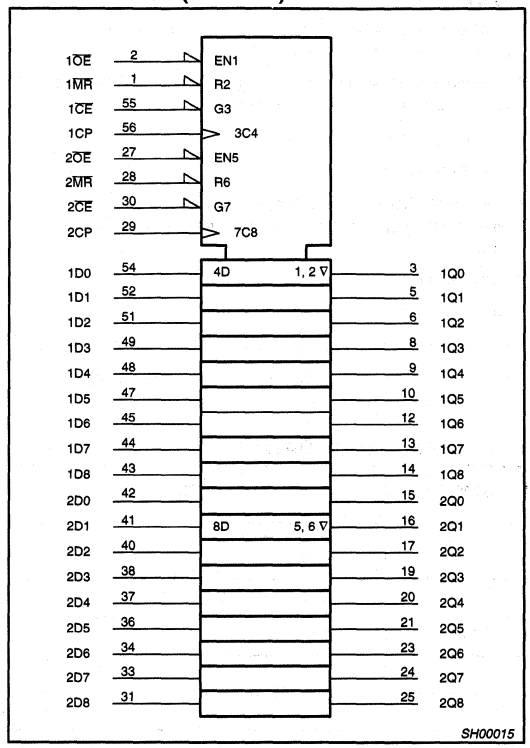
PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active-Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active-Low)
1, 28	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

18-bit bus-interface D-type flip-flop with reset and enable (3-State)

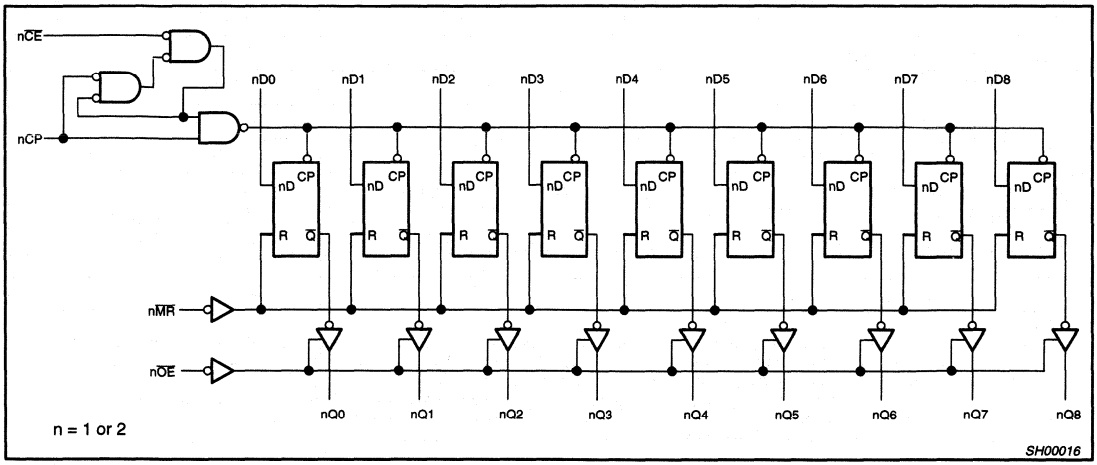
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
nOE	nMR	nCE	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_{OL} = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage curent	V_{CC} = 5.5V; V_I = V_{CC} or GND			±0.01	±1		±1	µA
I_I	Input leakage current 74ABTH16823A	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0	Data pins		–2	–3		–5	µA
I_{HOLD}	Bus Hold current inputs[4] 74ABTH16823A	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		µA
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V			±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}, V_{OE} = Don't care			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			50	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			9.0	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}			0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.2	1		1	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	140	190		140		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.4 1.2	2.3 1.9	3.2 2.6	1.4 1.2	3.7 2.9	ns
t_{PHL}	Propagation delay n$\overline{MR}$ to nQx	2	2.0	3.3	4.3	2.0	5.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.3 1.2	2.4 2.1	3.2 2.9	1.3 1.2	3.9 3.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.7 1.6	2.9 2.3	4.0 3.2	1.7 1.6	4.7 3.4	ns

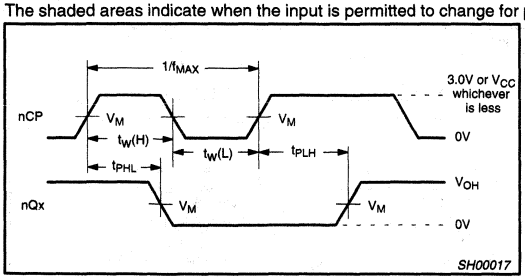
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

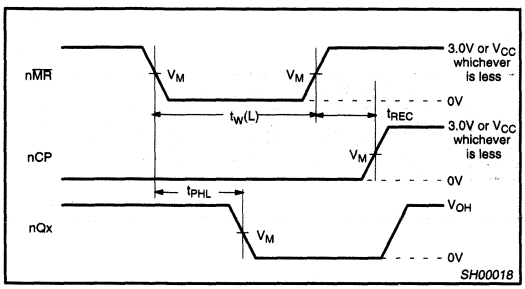
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	3	2.0 1.5	1.3 0.9	2.0 1.5	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	3	1.5 1.5	−0.9 −1.2	1.5 1.5	ns
t_w(H) t_w(L)	nCP pulse width High or Low	1	3.3 3.3	1.7 1.7	3.3 3.3	ns
t_s(H) t_s(L)	Setup time, High or Low n$\overline{CE}$ to nCP	3	1.5 2.0	0.9 0.9	1.5 2.0	ns
t_h(H) t_h(L)	Hold time, High or Low n$\overline{CE}$ to nCP	3	1.5 1.5	−0.8 −0.9	1.5 1.5	ns
t_w(L)	n$\overline{MR}$ pulse width, Low	2	3.0	1.7	3.0	ns
t_{rec}	Recovery time n$\overline{MR}$ to nCP	2	2.5	1.0	2.5	ns

AC WAVEFORMS

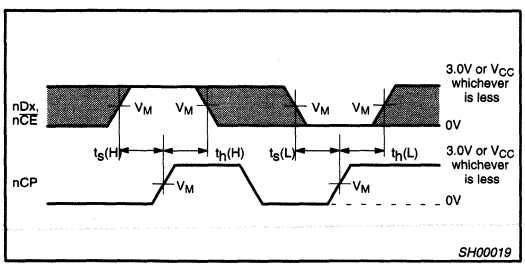
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



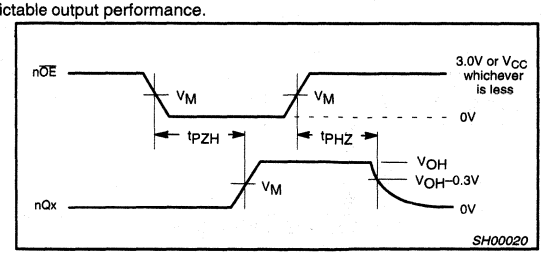
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



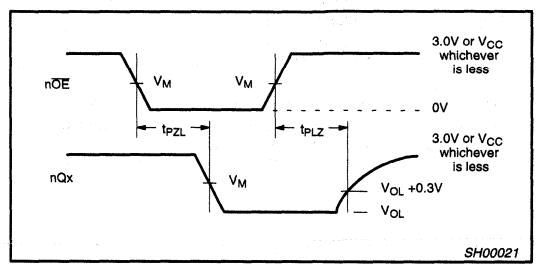
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Setup and Hold Times

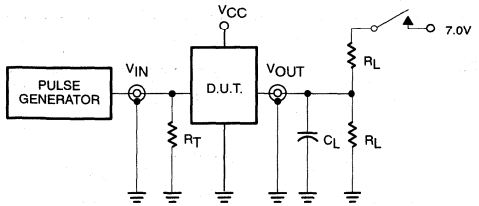


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

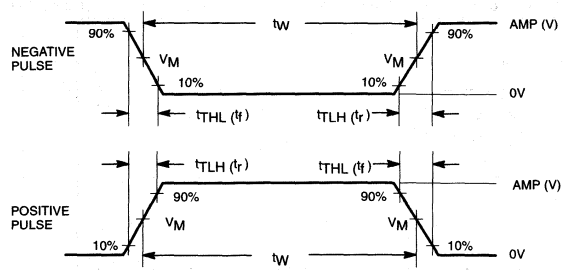


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00022

18-bit buffer/line driver; non-inverting (3-State)

74ABT16825A
74ABTH16825A

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- 74ABTH16825A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The74ABT16825A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The74ABT16825A 18-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

Two options are available, 74ABT16825A which does not have the bus-hold feature and 74ABTH16825A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	1.8 1.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs Low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

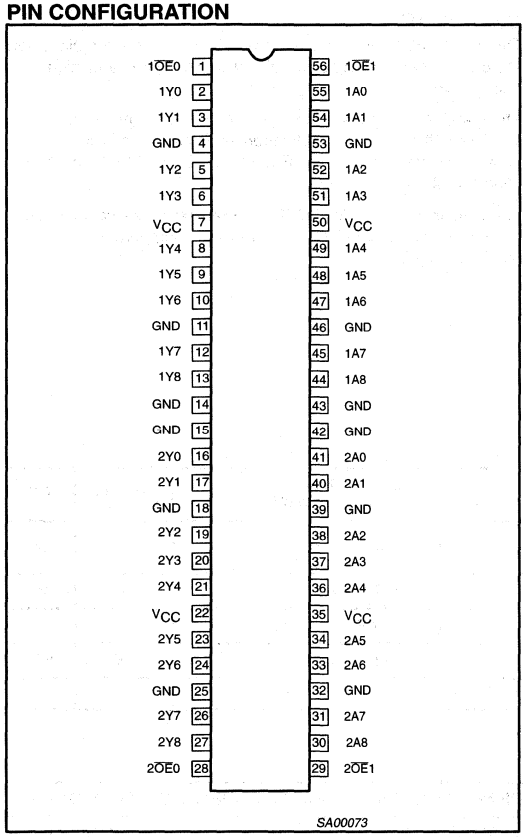
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-pin SSOP Type III	–40°C to +85°C	74ABT16825A DL	BT16825A DL	SOT371-1
56-pin TSSOP Type II	–40°C to +85°C	74ABT16825A DGG	BT16825A DGG	SOT364-1
56-pin SSOP Type III	–40°C to +85°C	74ABTH16825A DL	BH16825A DL	SOT371-1
56-pin TSSOP Type II	–40°C to +85°C	74ABTH16825A DGG	BH16825A DGG	SOT364-1

PIN DESCRIPTION

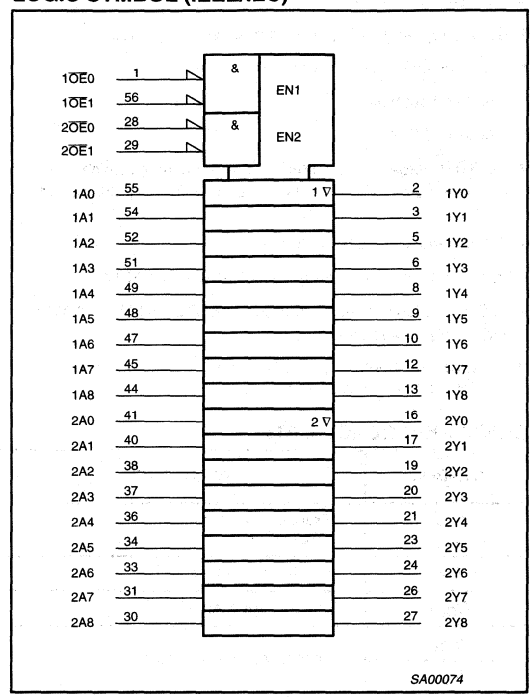
PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 – 1A9 2A0 – 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 – 1Y9 2Y0 – 2Y9	Data outputs
1, 56 28, 29	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active-Low)
4, 11, 14, 15, 18, 25, 32, 39, 42, 43, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

18-bit buffer/line driver; non-inverting (3-State)

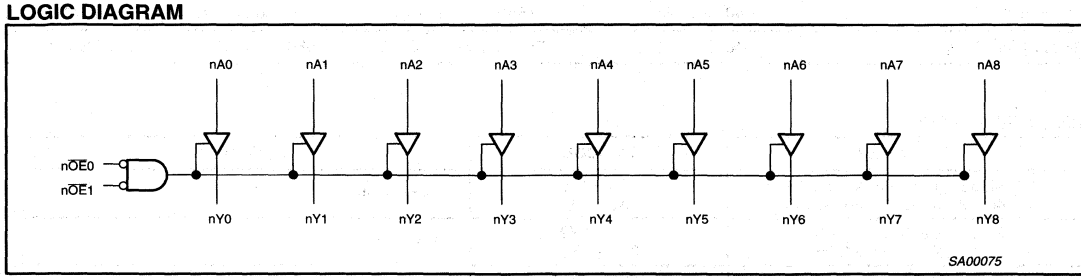
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



18-bit buffer/line driver; non-inverting (3-State)

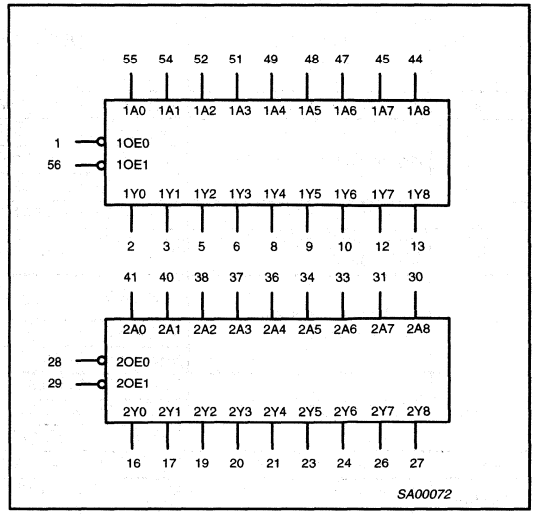
74ABT16825A
74ABTH16825A

FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$n\overline{OE}x$	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current ABT16825A	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH16825A	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins[4]		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0			−1	−3		−5	µA
I_{HOLD}	Bus Hold current A inputs[4] 74ABTH16825A	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O = 4.5V; V_I = 0V or 5.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}			−1.0	−10		−10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−70	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16825A	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			10	500		500	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16825A	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.2	1		1	mA

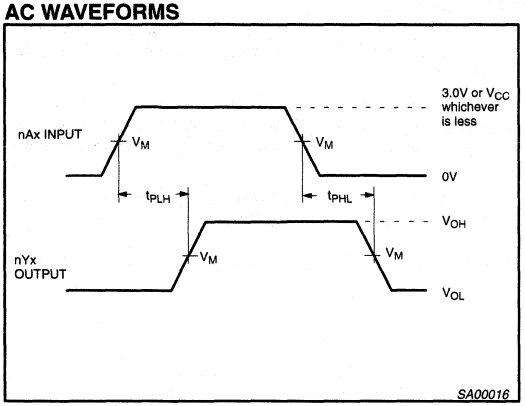
NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
4. Unused pins at V_{CC} or GND.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

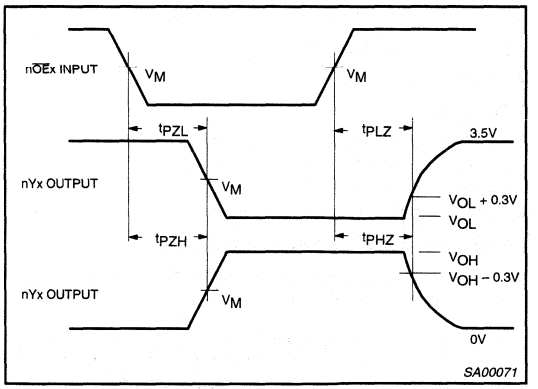
GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 0.6	1.8 1.4	2.5 2.0	1.0 0.6	2.8 2.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.9 2.9	3.8 3.8	1.0 1.0	4.8 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.0 1.6	3.3 2.5	4.5 3.4	2.0 1.6	5.2 3.7	ns

AC WAVEFORMS

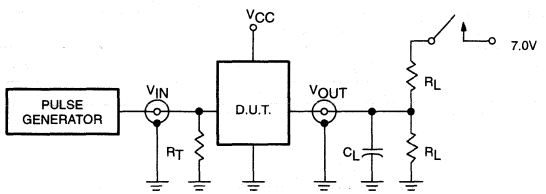


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

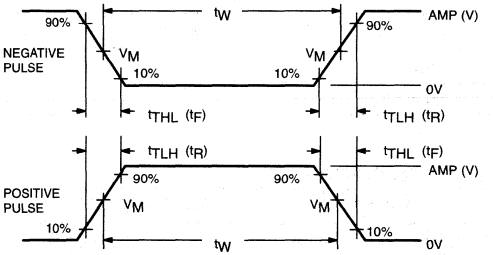


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

20-bit buffer/line driver, non-inverting (3-State)

74ABT16827A
74ABTH16827A

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- 74ABTH16827A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16827A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16827A 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

Two options are available, 74ABT16827A which does not have the bus-hold feature and 74ABTH16827A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	1.7 1.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs Low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16827A DL	BT16827A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16827A DGG	BT16827A DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16827A DL	BH16827A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16827A DGG	BH16827A DGG	SOT364-1

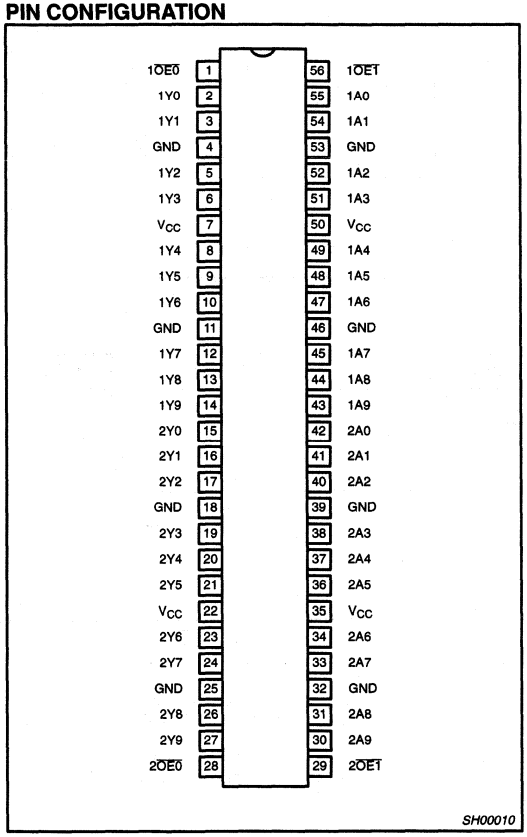
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 - 1A9 2A0 - 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 - 1Y9 2Y0 - 2Y9	Data outputs
1, 56, 28, 29	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

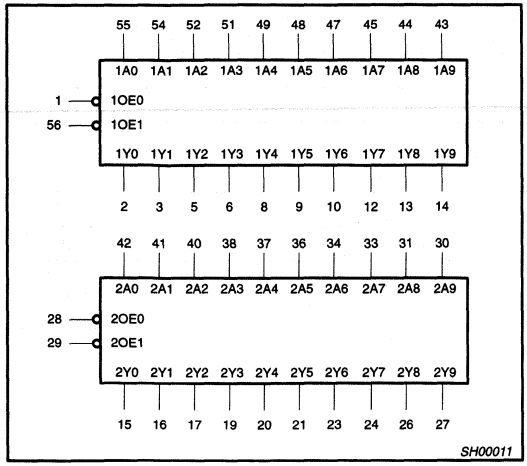
20-bit buffer/line driver, non-inverting (3-State)

74ABT16827A
74ABTH16827A

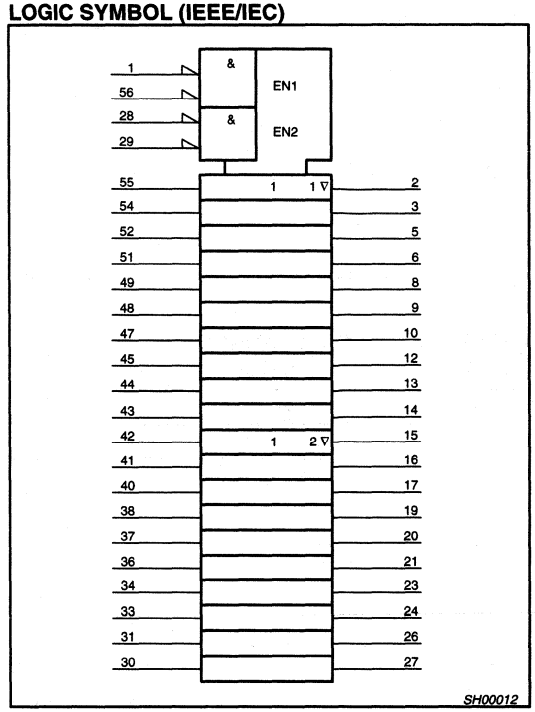
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

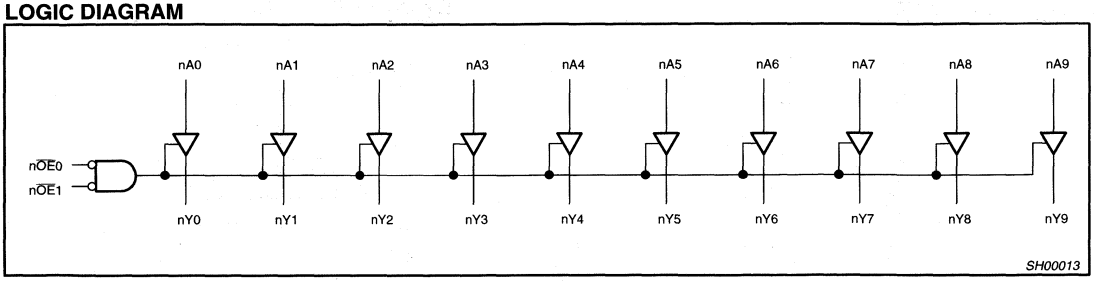


FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$n\overline{OE}x$	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = High voltage level
L = Low voltage level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH16827A	V_{CC} = 5.5V; V_I = 5.5V			0.01	1		1	µA
		V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins[4]		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0			–1	–3		–5	µA
I_{HOLD}	Bus Hold current A inputs[4] 74ABTH16827A	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O = 4.5V; V_I = 0V or 5.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.2	1		1	mA

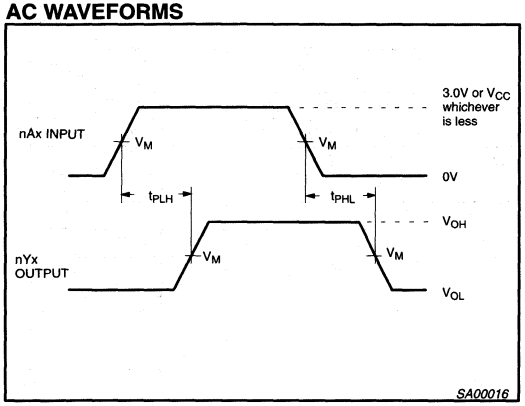
NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
4. Unused pins at V_{CC} or GND.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

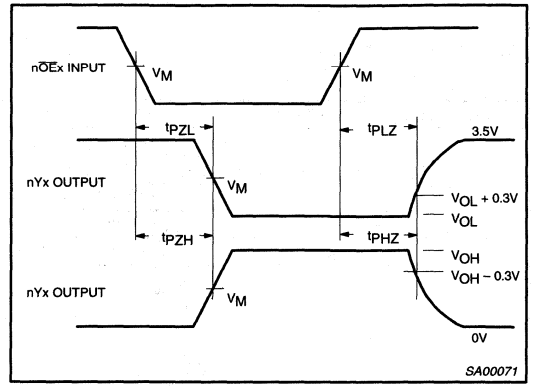
GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 0.6	1.7 1.4	2.4 2.0	1.0 0.6	2.7 2.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.0 3.0	4.1 4.0	1.0 1.0	5.0 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.0 1.6	3.2 2.4	4.3 3.2	2.0 1.6	5.0 3.5	ns

AC WAVEFORMS

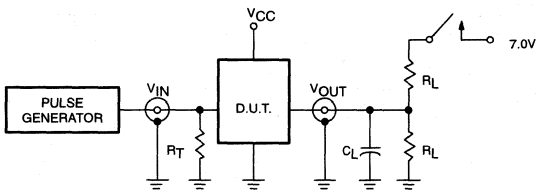


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

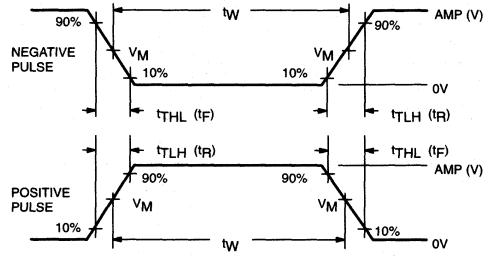


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

74ABT162827A
74ABTH162827A

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- 74ABTH162827A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT162827A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT162827A 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

The 74ABT162827A is designed with 30Ω series resistance in both the pull–up and pull–down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

Two options are available, 74ABT162827A which does not have the bus-hold feature and 74ABTH162827A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	1.8 1.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs Low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT162827A DL	BT162827A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT162827A DGG	BT162827A DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH162827A DL	BH162827A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH162827A DGG	BH162827A DGG	SOT364-1

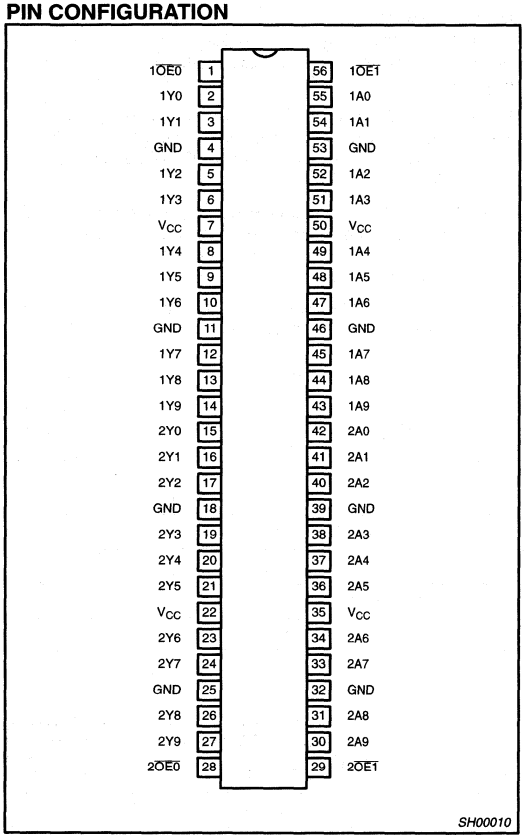
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 - 1A9 2A0 - 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 - 1Y9 2Y0 - 2Y9	Data outputs
1, 56, 28, 29	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

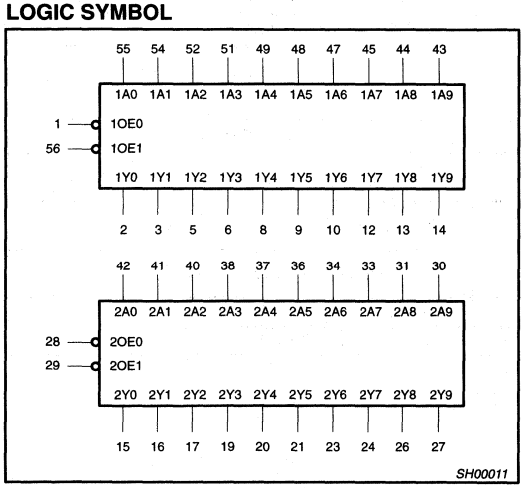
20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

74ABT162827A
74ABTH162827A

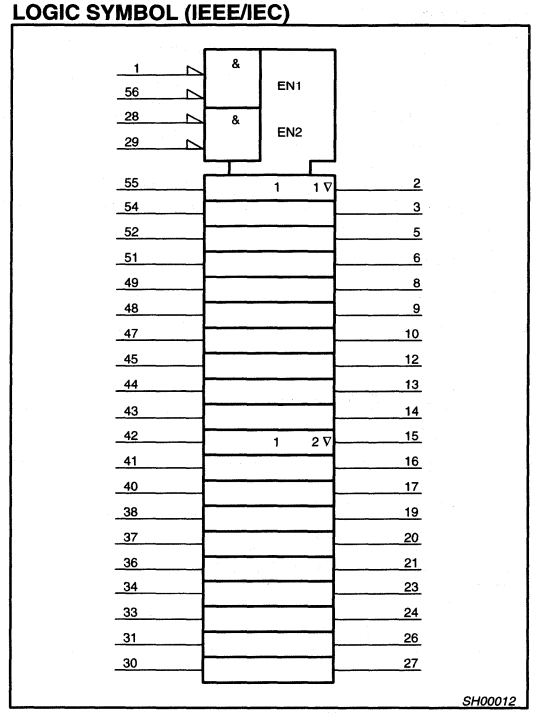
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

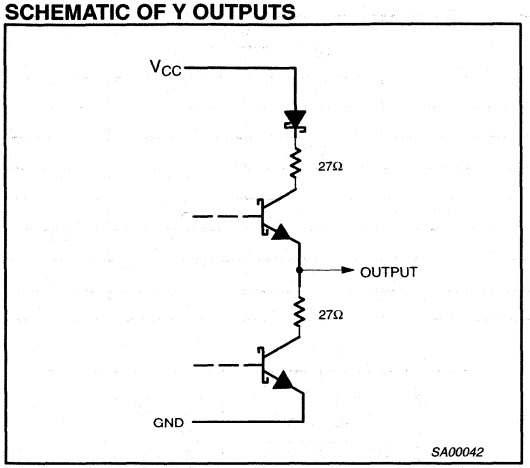


FUNCTION TABLE

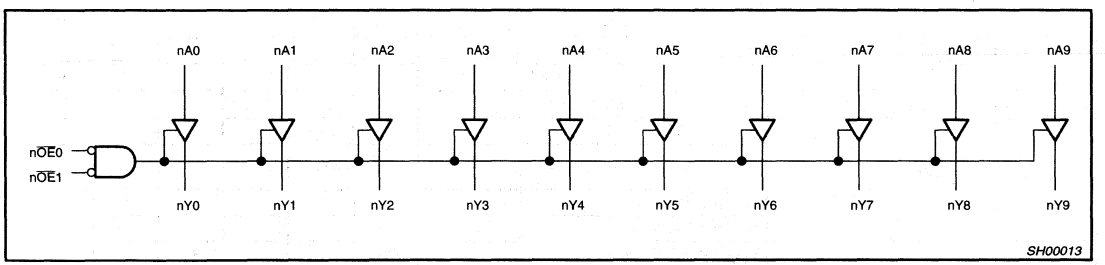
INPUTS		OUTPUTS	OPERATING MODE
$n\overline{OE}x$	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = High voltage level
L = Low voltage level

SCHEMATIC OF Y OUTPUTS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}		2.5	3.1		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}		3.0	3.6		3.0		V
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}		2.0	2.7		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OH} = 8mA; V_I = V_{IL} or V_{IN}				0.65		0.65	V
		V_{CC} = 4.5V; I_{OL} = 12mA; V_I = V_{IL}				0.80		0.80	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH162827A	V_{CC} = 5.5V; V_I = 5.5V			0.01	1		1	µA
		V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins[4]		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0			–1	–3		–5	µA
I_{HOLD}	Bus Hold current A inputs[4] 74ABTH162827A	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O = 4.5V; V_I = 0V or 5.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.2	1		1	mA

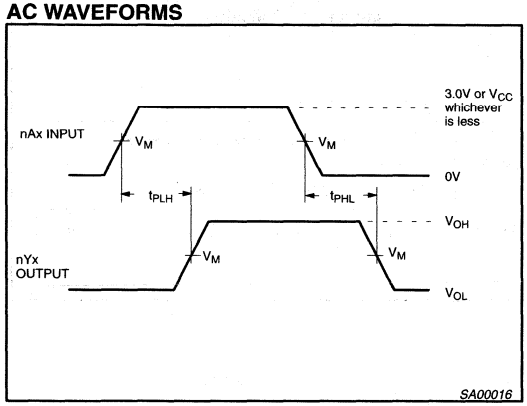
NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
4. Unused pins at V_{CC} or GND.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

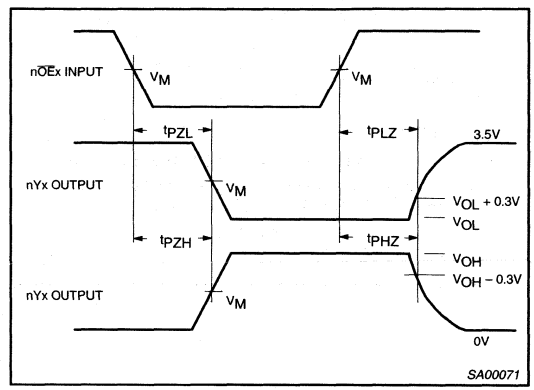
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	1.8 1.4	2.6 2.6	1.0 1.0	2.9 2.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 2.0	3.0 3.6	4.2 4.9	1.5 2.0	5.2 6.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.0 1.5	3.4 2.8	4.8 4.0	2.0 1.5	5.4 4.3	ns

AC WAVEFORMS

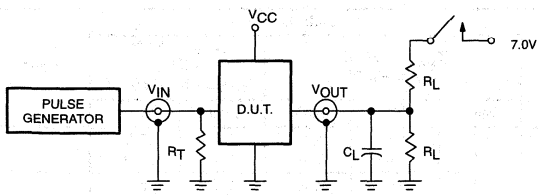


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

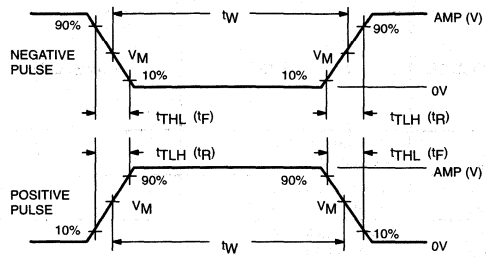


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

20-bit bus interface latch (3-State)

74ABT16841A
74ABTH16841A

FEATURES

- High speed parallel latches
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- 74ABTH16841A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16841A Bus interface latch is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16841A consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($n\overline{OE}$) is Low. When $n\overline{OE}$ is High the output is in the High-impedance state.

Two options are available, 74ABT16841A which does not have the bus-hold feature and 74ABTH16841A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF; V_{CC} = 5V	3.1 2.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5V	10	mA

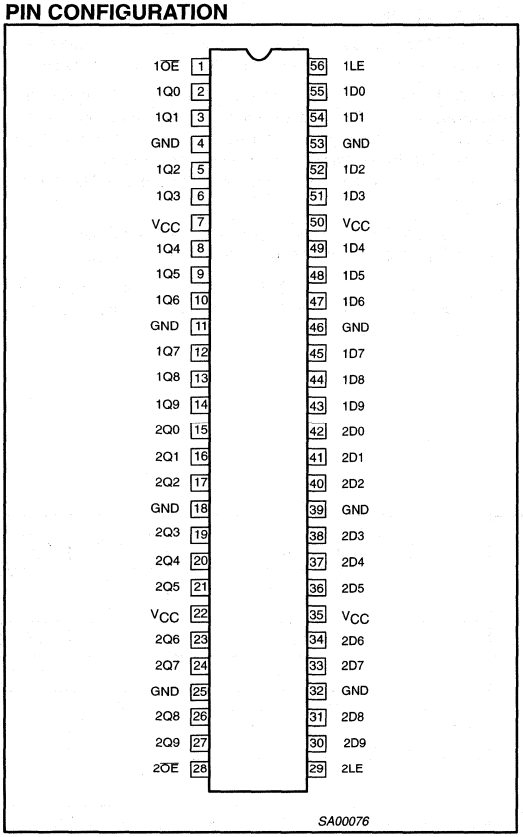
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16841A DL	BT16841A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16841A DGG	BT16841A DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16841A DL	BH16841A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16841A DGG	BH16841A DGG	SOT364-1

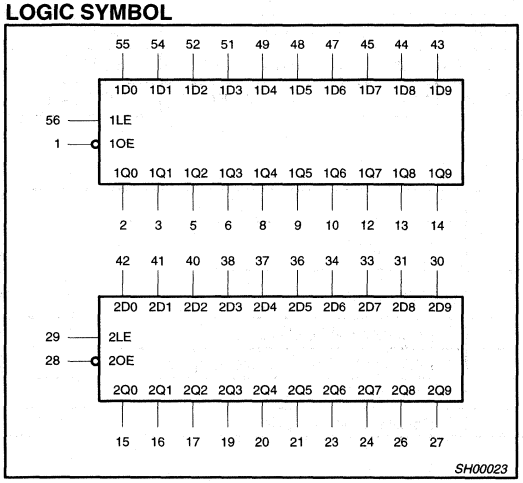
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 – 1D9 2D0 – 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
56, 29	1LE, 2LE	Latch enable inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

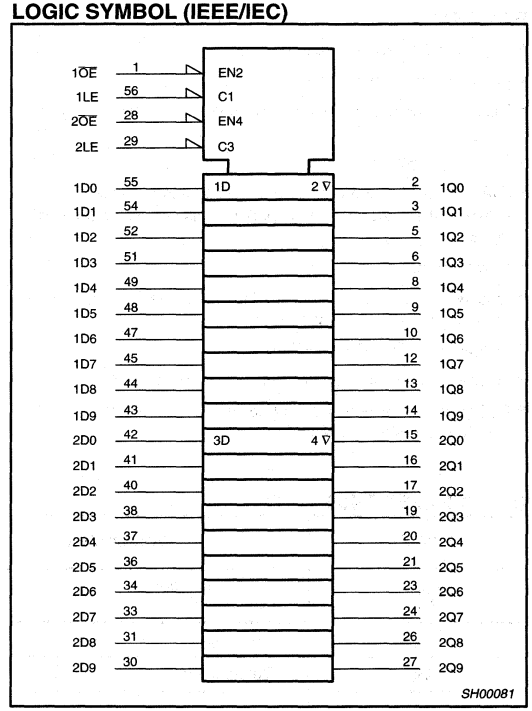
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

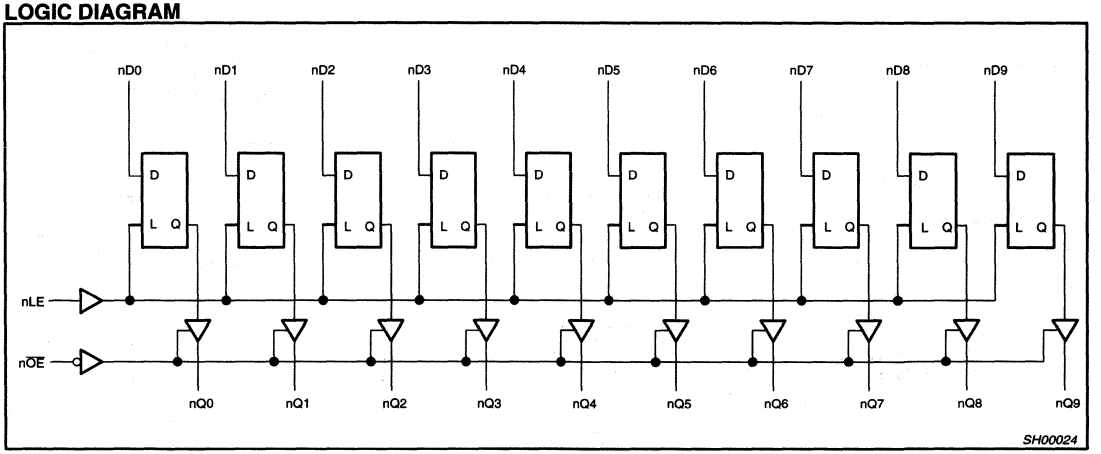


FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
nOE	nLE	nDx	nQ0 – nQ9	
L L	H H	L H	L H	Transparent
L L	↓ ↓	l h	L H	Latched
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
↓ = High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current 74ABT16841A	V_{CC} = 5.5V; V_I = V_{CC} or GND			±0.01	±1		±1.0	µA
I_I	Input leakage current 74ABTH16841A	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins[5]		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0			–2	–3		–5	µA
I_{HOLD}	Bus Hold current inputs[4] 74ABTH16841A	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V			±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = Don't care			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			5.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–5.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			10	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.2	1		1	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. Unused pins at V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.1 1.5	3.1 2.2	4.1 3.1	1.1 1.5	4.9 3.6	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.5 1.0	2.5 2.1	3.3 2.8	1.5 1.0	3.7 3.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.2 1.2	2.4 2.2	3.2 2.9	1.2 1.2	4.0 3.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.8 1.5	3.0 2.5	4.0 3.2	1.8 1.5	4.9 3.7	ns

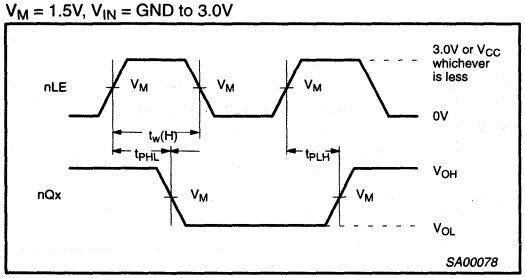
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

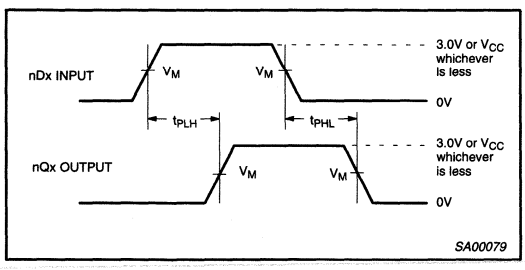
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nLE	3	2.0 1.0	1.0 0.4	2.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nLE	3	2.0 2.0	–0.3 –0.7	2.0 2.0		ns
$t_w(H)$	nLE pulse width High	1	2.9	1.9	2.9		ns

AC WAVEFORMS

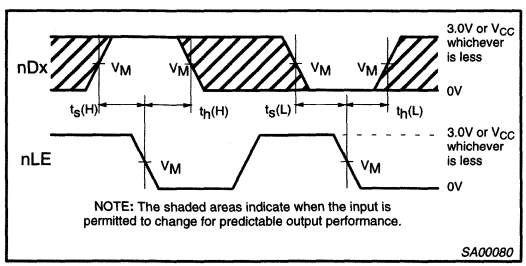
V_M = 1.5V, V_{IN} = GND to 3.0V



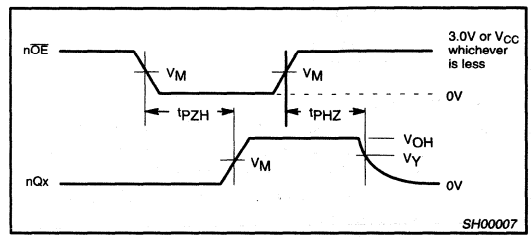
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



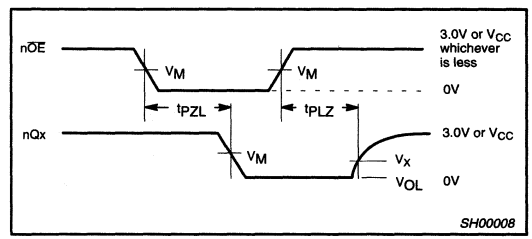
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

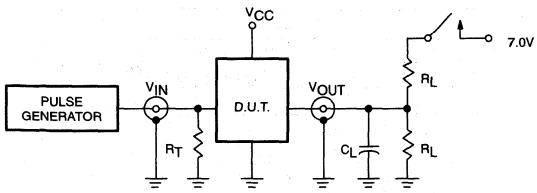


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

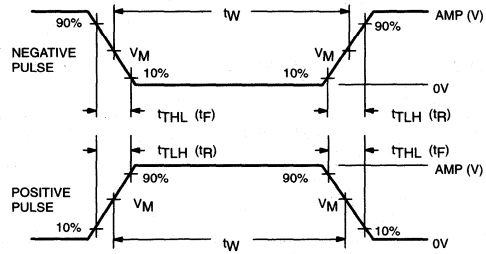


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

16-bit latch transceiver with 8-bit parity generator/checker (3-State)

74ABT16899
74ABTH16899

FEATURES

- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/$\overline{\text{EVEN}}$ parity
- Continuously checks parity of both A bus and B bus latches as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$
- Open-collector $\overline{\text{ERR}}$ output
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data
- Output capability: +64 mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up 3-State
- Power-up reset
- Live insertion/extraction permitted
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT/H16899 is a 16-bit to 16-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the $\overline{\text{SEL}}$ input.

Parity error checking of the A and B bus latches is continuously provided with $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$, even with both buses in 3-State.

The 74ABT/H16899 features independent latch enables for the A and B bus latches, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION

The 74ABT/H16899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEA and LEB are High and the Mode Select ($\overline{\text{SEL}}$) is Low, the parity generated from A0-A7 and B0-B7 can be checked and monitored by $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$. (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is High. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ and can be used as an interrupt to signal a data/parity bit error to the CPU.

Latched input, Generate/Feed-through parity, Check A (and B) bus parity:
Independent latch enables (LEA and LEB) allow other permutations of:

- Transparent latch / 1 bus latched / both buses latched
- Feed-through parity / generate parity
- Check in bus parity / check out bus parity / check in and out bus parity

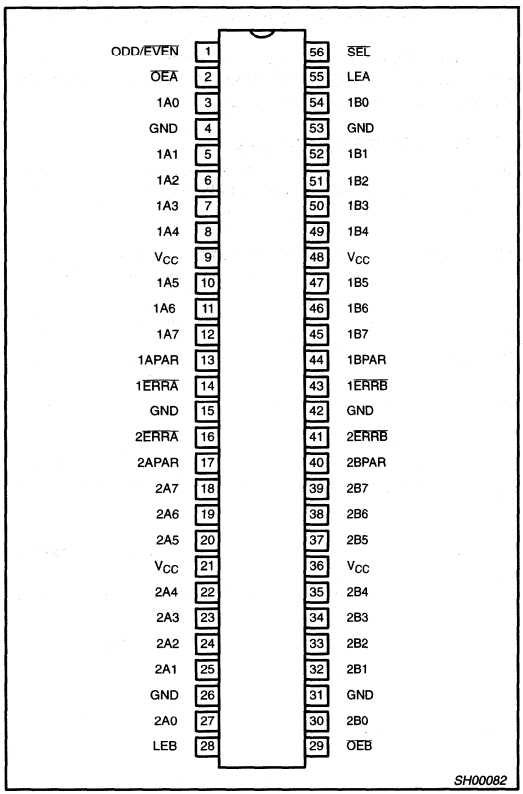
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	2.7	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{\text{ERRA}}$	C_L = 50pF; V_{CC} = 5V	5.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =5.5V	500	µA
I_{CCL}		Output Low; V_{CC} = 5.5V	10.5	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16899 DL	BT16899 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16899 DGG	BT16899 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16899 DL	BH16899 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16899 DGG	BH16899 DGG	SOT364-1

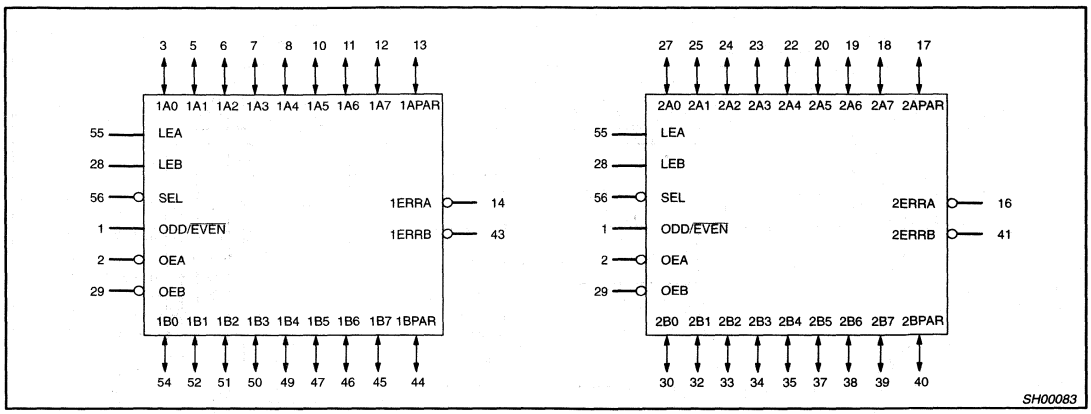
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1A0 - 1A7 2A0 - 2A7	3, 5, 6, 7, 8, 10, 11, 12 27, 25, 24, 23, 22, 20, 19, 18	Latched A bus 3-State inputs/outputs
1B0 - 1B7 2B0 - 2B7	54, 52, 51, 50, 49, 47, 46, 45 30, 32, 33, 34, 35, 37, 38, 39	Latched B bus 3-State inputs/outputs
1APAR 2APAR	13, 17	A bus parity 3-State input
1BPAR 2BPAR	44, 40	B bus parity 3-State input
ODD/$\overline{\text{EVEN}}$	1	Parity select input (Low for EVEN parity)
$\overline{\text{OEA}}$, $\overline{\text{OEB}}$	2, 29	Output enable inputs (gate A to B, B to A)
$\overline{\text{SEL}}$	56	Mode select input (Low for generate)
LEA, LEB	55, 28	Latch enable inputs (transparent High)
1$\overline{\text{ERRA}}$, 1$\overline{\text{ERRB}}$ 2$\overline{\text{ERRA}}$, 2$\overline{\text{ERRB}}$	14, 43, 16, 41	Error signal outputs (active-Low)
GND	4, 15, 26, 31, 42, 53	Ground (0V)
V_{CC}	9, 21, 36, 48	Positive supply voltage

LOGIC SYMBOL



PARITY AND ERROR FUNCTION TABLE

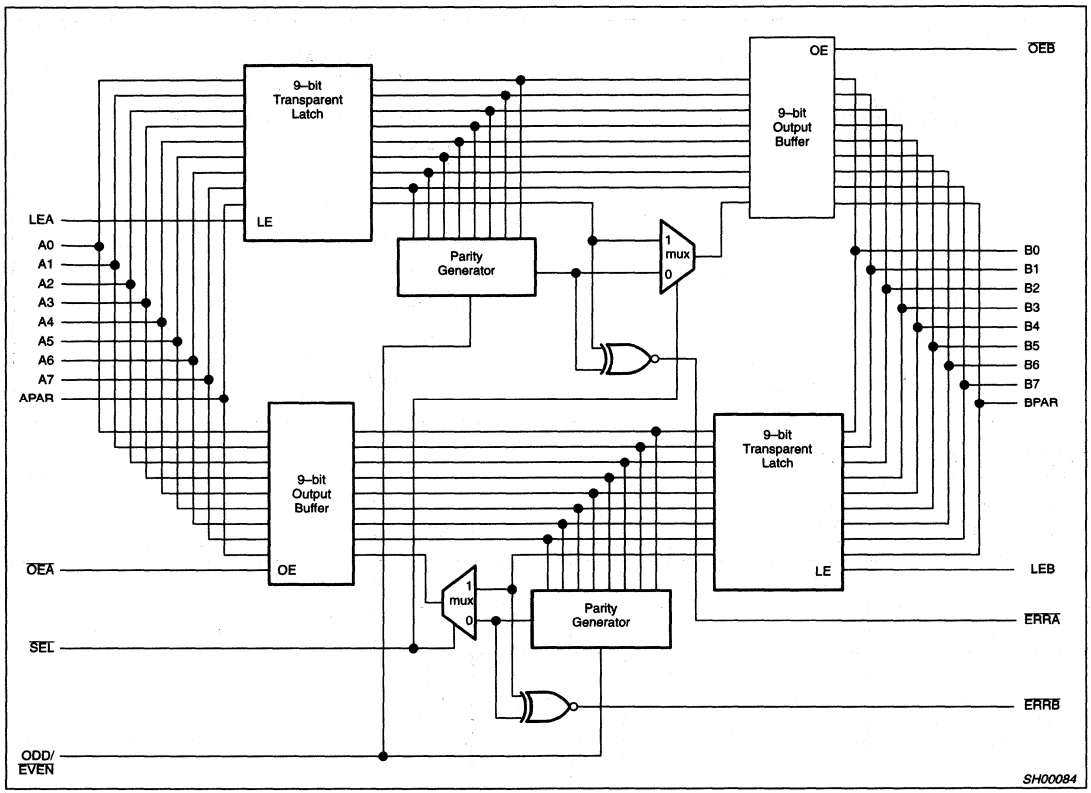
INPUTS				OUTPUTS			PARITY MODES	
$\overline{SEL}$	ODD/$\overline{EVEN}$	xPAR (A or B)	Σ of High Inputs	xPAR (B or A)	$\overline{ERRt}$	$\overline{ERRr}$*		
H	H	H	Even Odd	H H	H L	H L	Odd Mode	Feed-through/check parity
H	H	L	Even Odd	L L	L H	L H		
H	L	H	Even Odd	H H	L H	L H	Even Mode	
H	L	L	Even Odd	L L	H L	H L		
L	H	H	Even Odd	H L	H L	H H	Odd Mode	Generate parity
L	H	L	Even Odd	H L	L H	H H		
L	L	H	Even Odd	L H	L H	H H	Even Mode	
L	L	L	Even Odd	L H	H L	H H		

H = High voltage level
L = Low voltage level
t = Transmit–if the data path is from A→B then $\overline{ERRt}$ is $\overline{ERRA}$
r = Receive–if the data path is from A→B then $\overline{ERRr}$ is $\overline{ERRB}$
* Blocked if latch is not transparent

16-bit latch transceiver with 8-bit parity generator/checker (3-State)

74ABT16899
74ABTH16899

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OEB}$	$\overline{OEA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	3-State A bus and B bus (input A & B simultaneously)
H	L	L	L	H	B → A, transparent B latch, generate parity from B0 - B7, check B bus parity
H	L	L	H	H	B → A, transparent A & B latch, generate parity from B0 - B7, check A & B bus parity
H	L	L	X	L	B → A, B bus latched, generate parity from latched B0 - B7 data, check B bus parity
H	L	H	X	H	B → A, transparent B latch, parity feed-through, check B bus parity
H	L	H	H	H	B → A, transparent A & B latch, parity feed-through, check A & B bus parity
L	H	L	H	X	A → B, transparent A latch, generate parity from A0 - A7, check A bus parity
L	H	L	H	H	A → B, transparent A & B latch, generate parity from A0 - A7, check A & B bus parity
L	H	L	L	X	A → B, A bus latched, generate parity from latched A0 - A7 data, check A bus parity
L	H	H	H	L	A → B, transparent A latch, parity feed-through, check A bus parity
L	H	H	H	H	A → B, transparent A & B latch, parity feed-through, check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 1505C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = −18mA		−0.7	−1.2		−1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	3.1		2.5		V
			V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.6		3.0		V
			V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.7		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.36	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.2	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±1.0	±100		±100	µA
I_{HOLD}	Bushold current A or B inputs[4] 74ABTH16899		V_{CC} = 4.5V; V_I = 0.8V	75			75		µA
			V_{CC} = 4.5V; V_I = 2.0V	−75			−75		
			V_{CC} = 5.5V; V_I = 0 to 5.5V	±500					
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±2.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		2.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−2.0	−50		−50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		2.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	−50	−100	−180	−50	−180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	1		1	mA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		10.5	19		19	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.2	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.7 2.2	4.5 3.5	1.0 1.0	5.5 6.9	ns
t_{PLH} t_{PHL}	Propagation delay An to BPAR or Bn to APAR	2	2.5 2.5	4.9 5.0	7.2 7.4	2.5 2.5	8.8 8.7	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{ERRA}$ or Bn to $\overline{ERRB}$	3	2.8 2.8	5.0 4.9	9.3 8.0	2.8 2.8	11.0 10.2	ns
t_{PLH} t_{PHL}	Propagation delay APAR to BPAR or BPAR to APAR	1	1.5 1.5	3.1 2.5	3.9 3.1	1.5 1.5	4.8 3.9	ns
t_{PLH} t_{PHL}	Propagation delay APAR to $\overline{ERRA}$ or BPAR to $\overline{ERRB}$	6	1.0 1.0	2.5 2.5	3.3 3.3	1.0 1.0	4.3 3.9	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to APAR or BPAR	5	2.5 2.5	4.1 3.9	5.1 5.0	2.5 2.5	6.1 5.7	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$ or $\overline{ERRB}$	4	2.5 2.5	4.1 4.0	6.1 5.5	2.5 2.5	7.1 6.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to APAR or BPAR	8	1.5 1.5	3.1 2.6	4.0 3.4	1.5 1.5	5.0 4.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to $\overline{ERRA}$ or $\overline{ERRB}$	8	2.5 2.5	5.0 4.4	7.5 5.9	2.5 2.5	8.3 7.1	ns
t_{PLH} t_{PHL}	Propagation delay LEA to Bn or LEB to An	9	1.0 1.0	3.1 2.8	4.2 4.3	1.0 1.0	5.2 4.7	ns
t_{PLH} t_{PHL}	Propagation delay LEA to BPAR or LEB to APAR	9	2.8 2.8	5.5 5.1	8.0 7.7	2.8 2.8	9.7 9.1	ns
t_{PLH} t_{PHL}	Propagation delay LEA to $\overline{ERRA}$ or LEB to $\overline{ERRB}$	7	1.1 1.2	5.4 5.8	8.0 8.0	1.1 1.2	9.2 9.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	11, 12	1.0 1.0	2.6 2.3	3.6 3.2	1.0 1.0	5.1 4.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	11, 12	2.5 1.5	3.9 2.8	5.6 4.1	2.5 1.5	6.0 4.4	ns

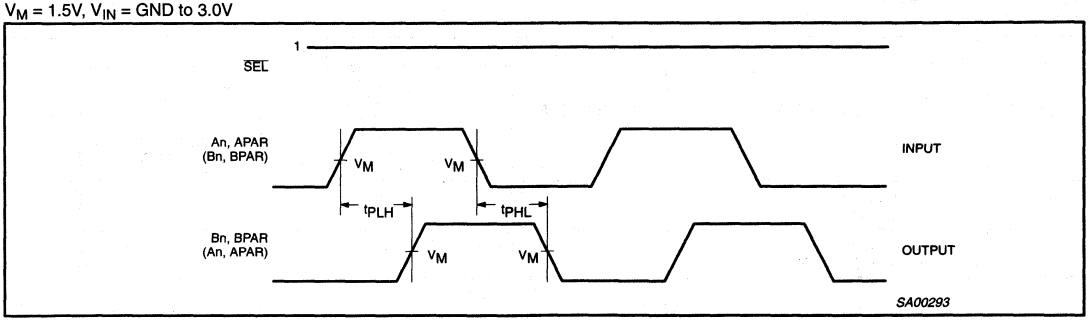
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

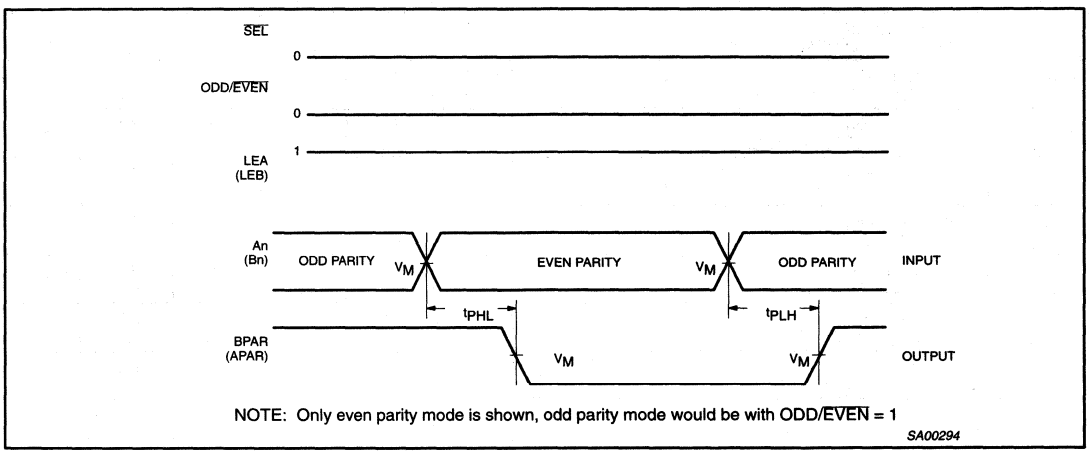
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω		T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω	
			Min	Typ	Min	
t_s(H) t_s(L)	Setup time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	1.5 1.0	0.3 −0.1	1.5 1.0	ns
t_h(H) t_h(L)	Hold time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	1.5 1.0	0.1 −0.2	1.5 1.0	ns
t_w(H)	Pulse width, High LEA or LEB	10	3.0	1.0	3.0	ns

AC WAVEFORMS

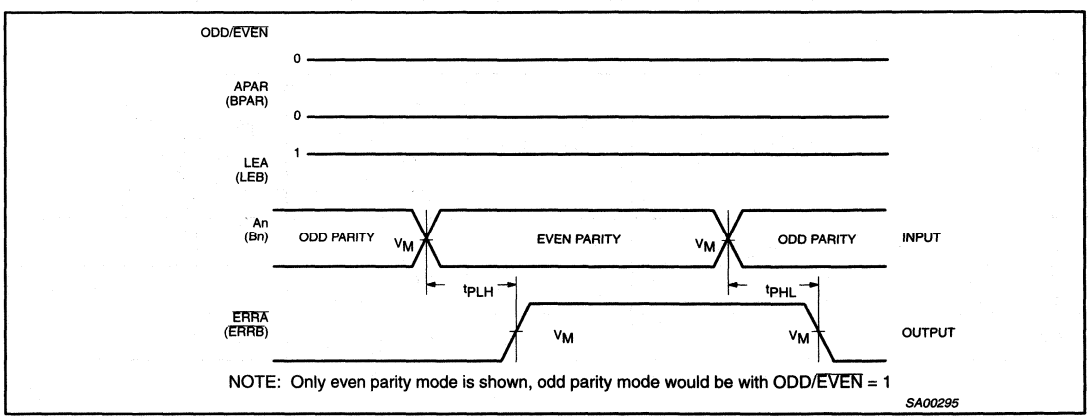
V_M = 1.5V, V_{IN} = GND to 3.0V



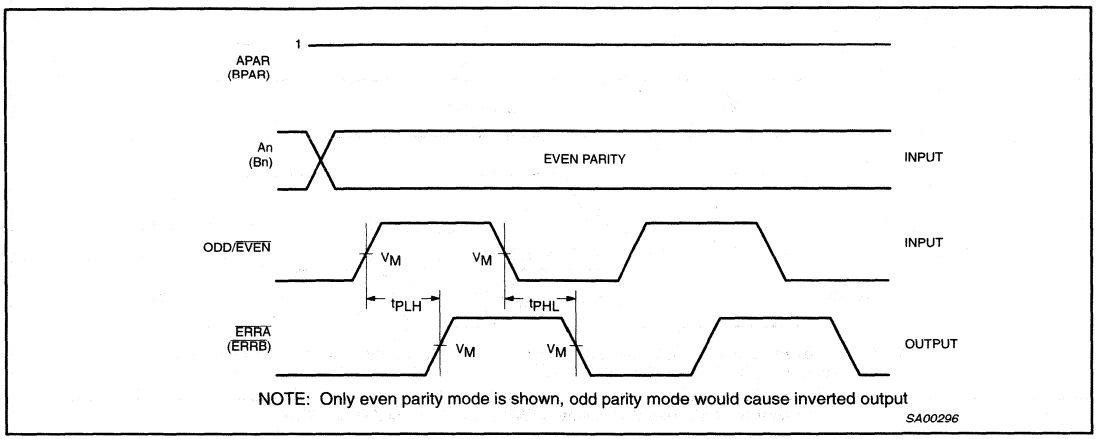
Waveform 1. Propagation Delay, An to Bn, Bn to An, APAR to BPAR, BPAR to APAR



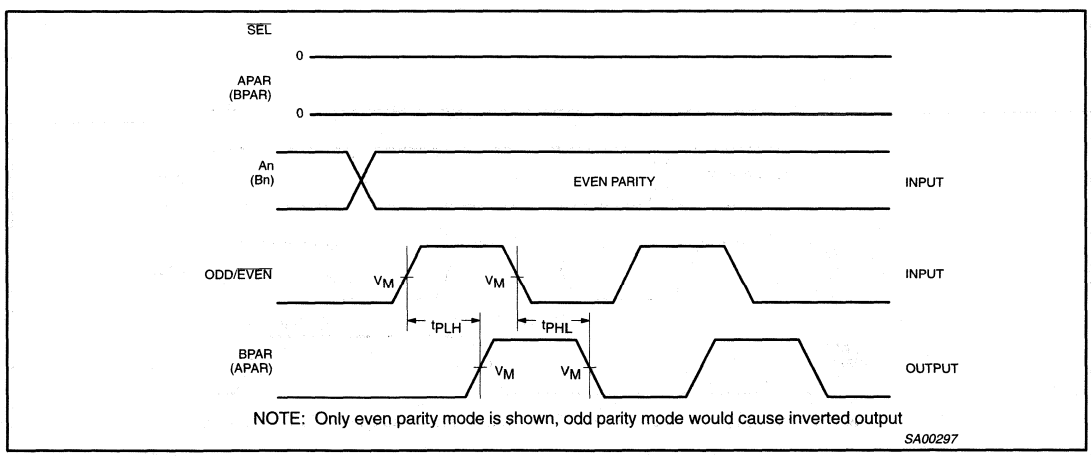
Waveform 2. Propagation Delay, An to BPAR or Bn to APAR



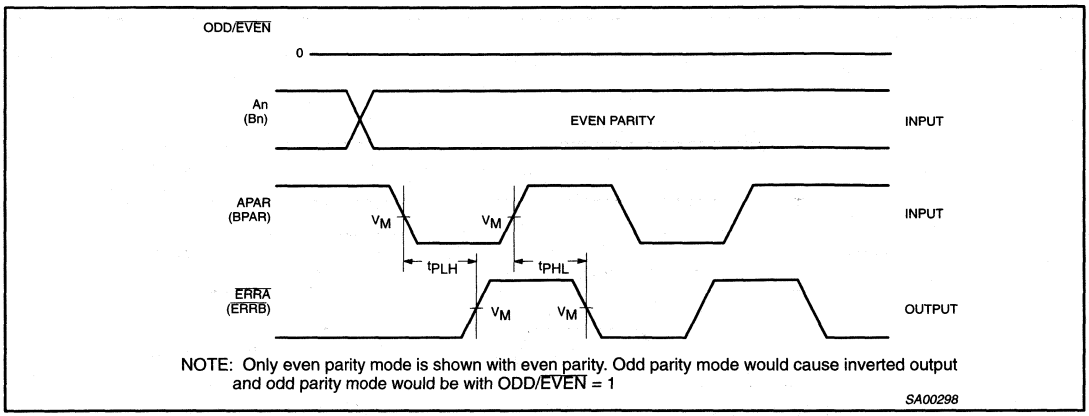
Waveform 3. Propagation Delay, An to ERRA or Bn to ERRB



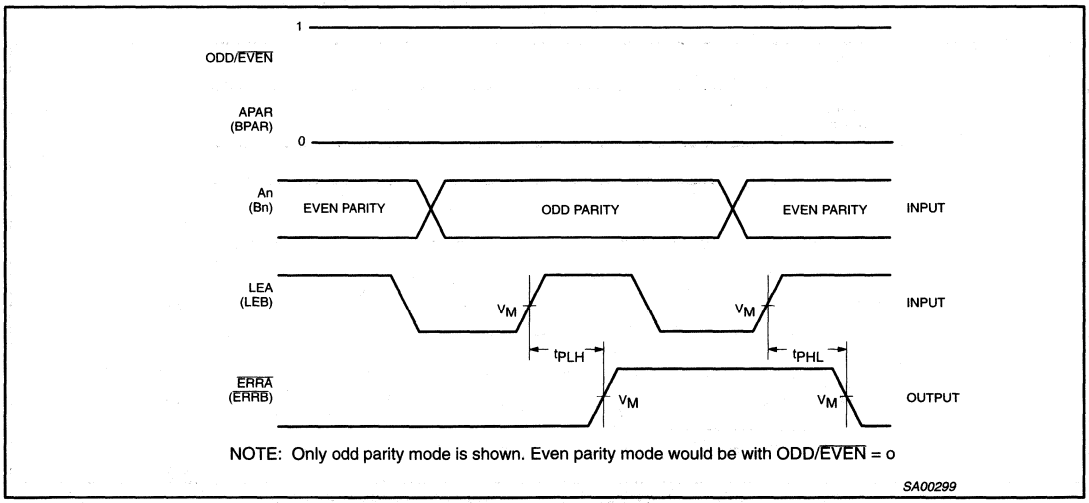
Waveform 4. Propagation Delay, ODD/EVEN to ERRA or ODD/EVEN to ERRB



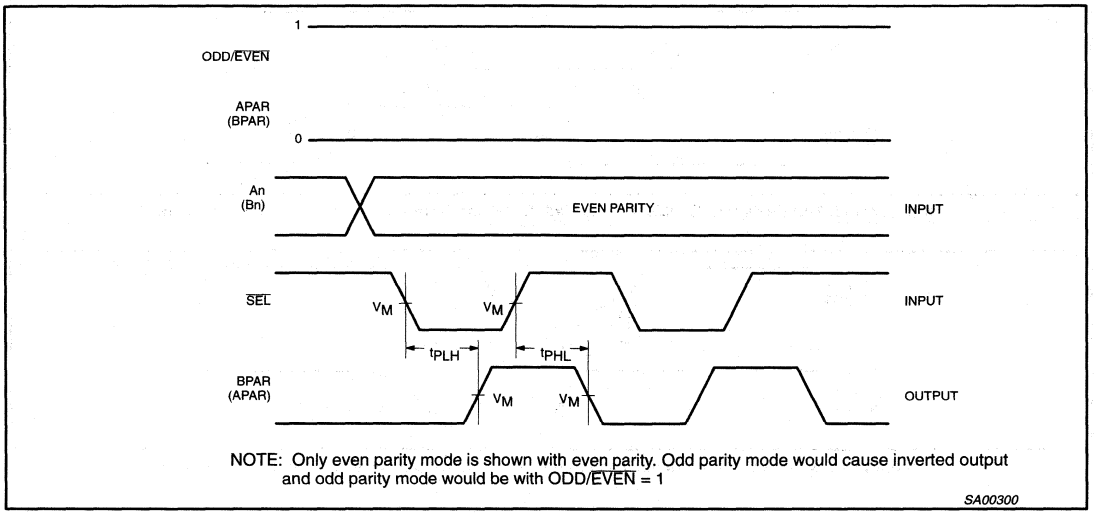
Waveform 5. Propagation Delay, ODD/EVEN to APAR or ODD/EVEN to BPAR



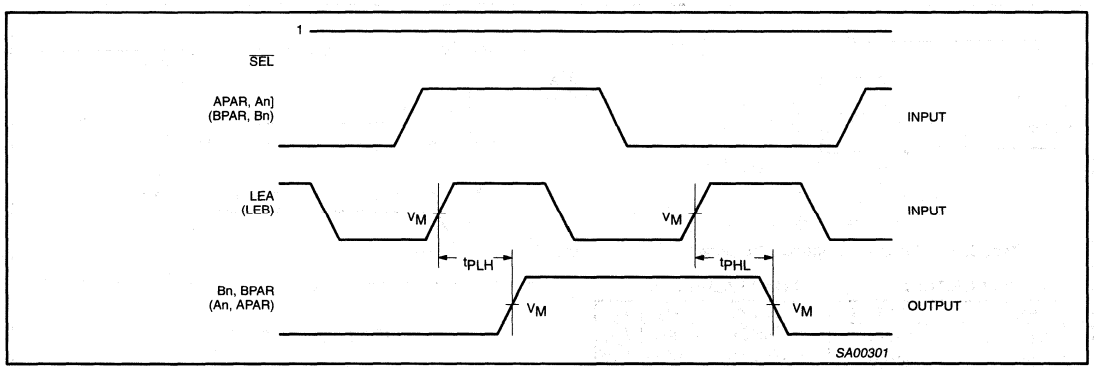
Waveform 6. Propagation Delay, APAR to $\overline{\text{ERRA}}$ or BPAR to $\overline{\text{ERRB}}$



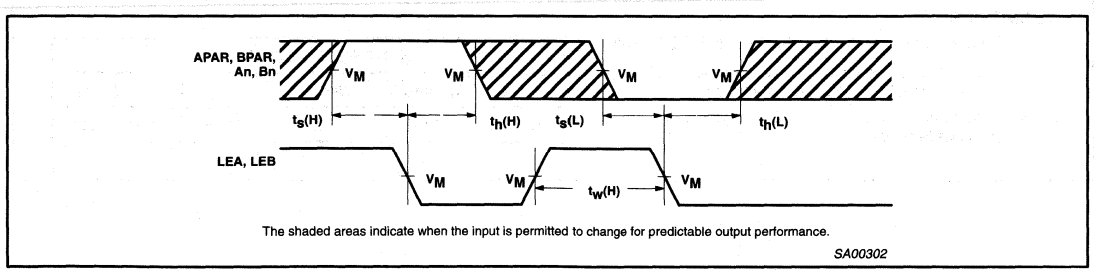
Waveform 7. Propagation Delay, LEA to $\overline{\text{ERRA}}$ or LEB to $\overline{\text{ERRB}}$



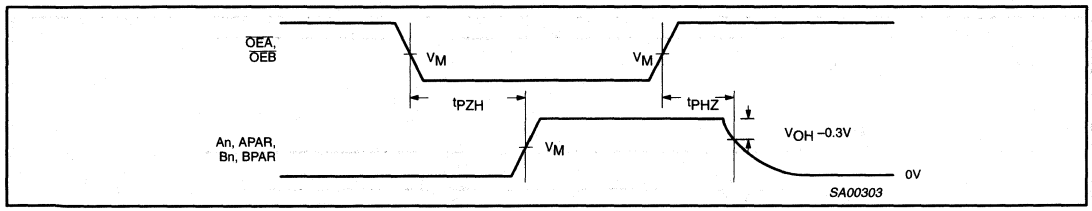
Waveform 8. Propagation Delay, $\overline{SEL}$ to BPAR or $\overline{SEL}$ to APAR



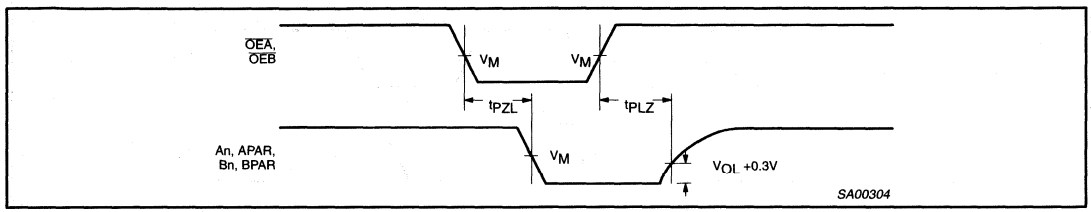
Waveform 9. Propagation Delay, LEA to BPAR or LEB to APAR, LEA to Bn or LEB to An



Waveform 10. Data Setup and Hold Times, Pulse Width High

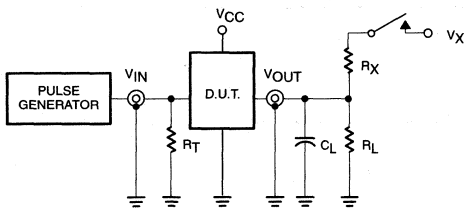


Waveform 11. 3-State Output Enable Time to High Level and Output Disable Time from High Level

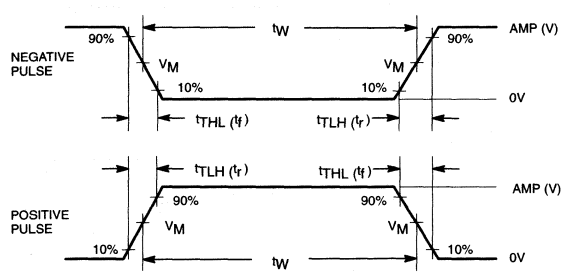


Waveform 12. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

LOAD VALUES

OUTPUT	R_X	V_X
$\overline{ERROR}$	100 Ω	V_{CC}
All other	500 Ω	7.0V

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00009

16-bit registered transceiver (3-State)

74ABT16952
74ABTH16952

FEATURES

- Two 8-bit registered transceivers
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16952 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Independent registers for A and B buses
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT16952 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16952 is a dual octal registered transceiver. Two 8-bit registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (nCPXX) provided that the Clock Enable ($n\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($n\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

Two options are available, 74ABT16952 which does not have the bus-hold feature and 74ABTH16952 which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx or nCPAB to nBx	C_L = 50pF; V_{CC} = 5V	2.8 2.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5V	8	mA

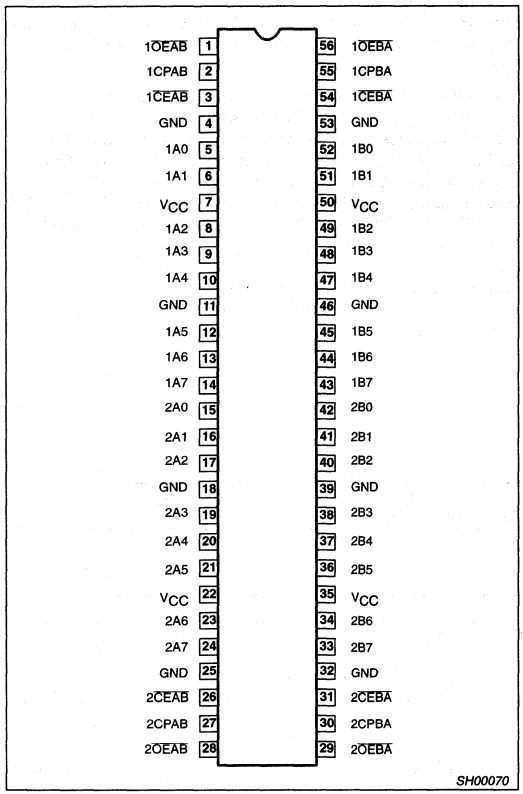
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16952 DL	BT16952 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16952 DGG	BT16952 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16952 DL	BH16952 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16952 DGG	BH16952 DGG	SOT364-1

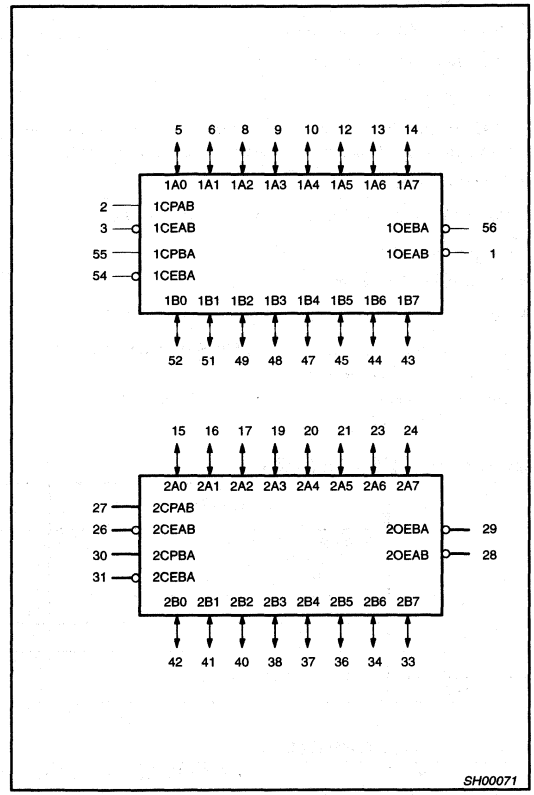
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55 18, 22	1CPAB / 1CPBA 2CPAB / 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	$1\overline{CEAB}$ / $1\overline{CEBA}$ $2\overline{CEAB}$ / $2\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1A0 – 1A7 2A0 – 2A7	Data inputs/outputs (A side)
1, 56 8, 29	1B0 – 1B7 2B0 – 2B7	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 45, 53	$1\overline{OEAB}$ / $1\overline{OEBA}$ $2\overline{OEAB}$ / $2\overline{OEBA}$	Output enable inputs
4, 17, 30, 43	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

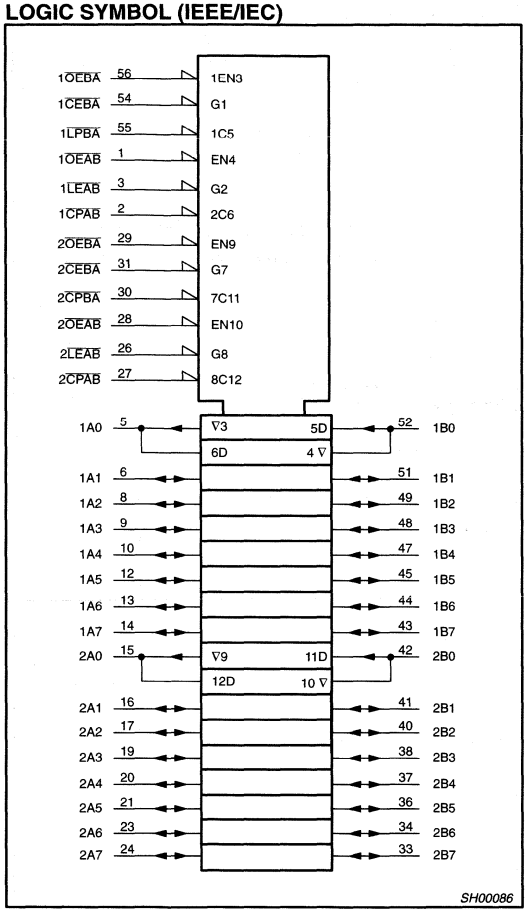
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL	OPERATING
nAx or nBx	nCPXX	$n\overline{CEXX}$	Q	MODE
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

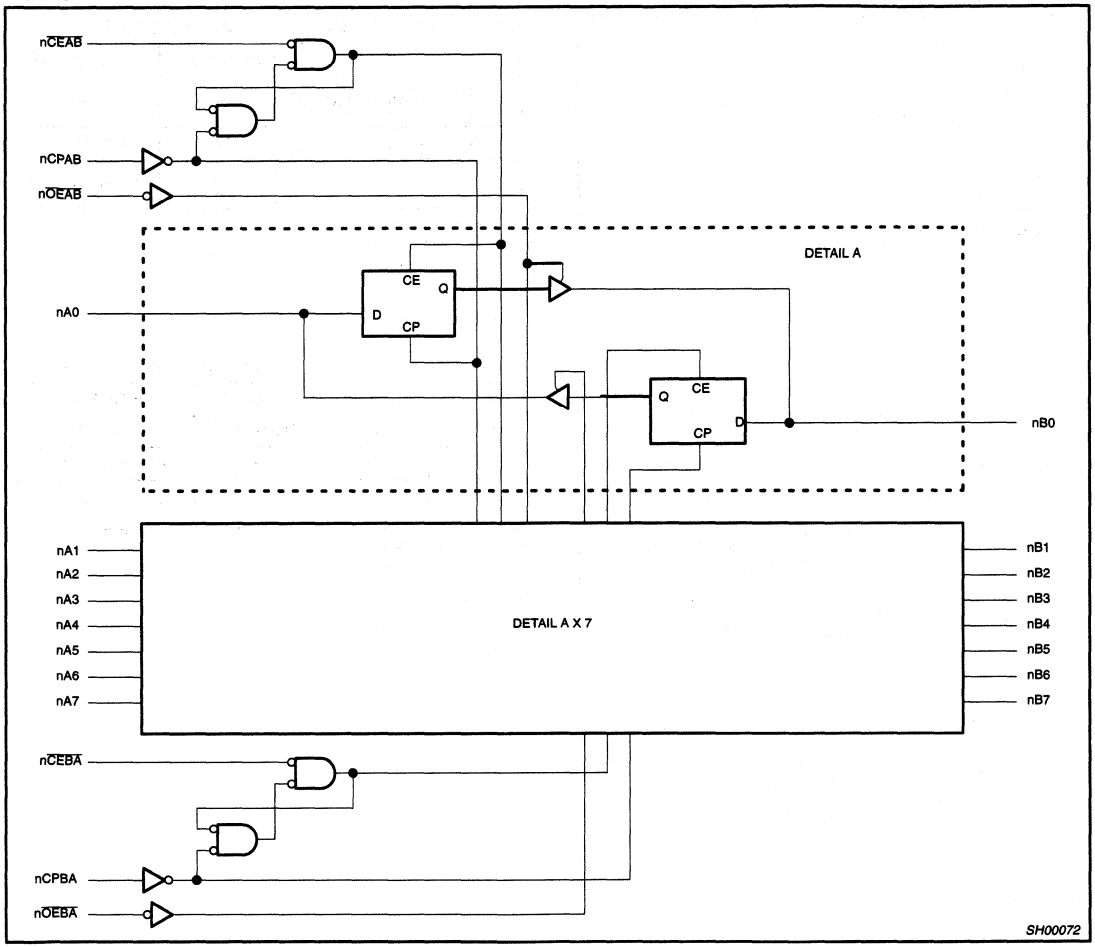
H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	nAx or nBx	OPERATING
$n\overline{OEXX}$	Q	OUTPUTS	MODE
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_{OL} = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current — Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A inputs[4] 74ABTH16952	V_{CC} = 4.5V, V_I = 0.8V	50			50		µA
		V_{CC} = 4.5V; V_I = 2.0V	–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V	±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{cc}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	1.5		1.5	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	1.5		1.5	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16952	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		5	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16952	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		100	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. Unused pins at V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

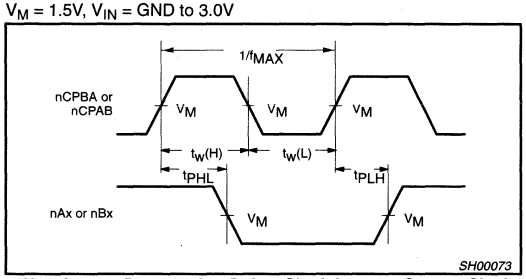
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	150			150		MHz
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx, nCPAB to nBx	1	1.0 1.0	2.8 2.3	3.9 3.9	1.0 1.0	4.3 4.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{nOEBA}$ to nAx, $\overline{nOEAB}$ to nBx	3 4	1.0 1.0	2.5 2.2	3.8 3.8	1.0 1.0	4.6 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{nOEBA}$ to nAx, $\overline{nOEAB}$ to nBx	3 4	1.7 1.3	3.4 2.6	4.4 3.9	1.7 1.3	5.2 4.2	ns

AC SETUP REQUIREMENTS

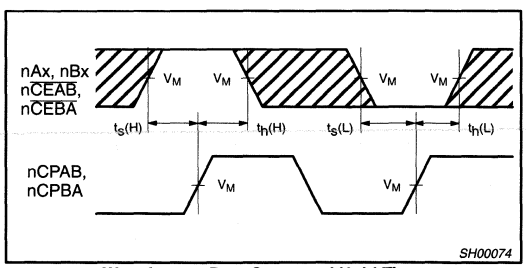
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C V_{CC} = +5.0V		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_S(H)$ $t_s(L)$	Setup time nAx to nCPAB or nBx to nCPBA	2	1.2 1.5	0.9 1.2	1.2 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nCPAB or nBx to nCPBA	2	0.0 0.0	–1.2 –0.9	0.0 0.0	ns
$t_s(H)$ $t_s(L)$	Setup time $n\overline{CEAB}$ to nCPAB, $n\overline{CEBA}$ to nCPBA	2	1.2 1.6	0.9 1.1	1.2 1.6	ns
$t_h(H)$ $t_h(L)$	Hold time $n\overline{CEAB}$ to nCPAB, $n\overline{CEBA}$ to nCPBA	2	0.0 0.0	–1.1 –0.9	0.0 0.0	ns
$t_w(H)$ $t_w(L)$	nCPAB or nCPBA pulse width, High or Low	1	3.3 2.5	2.6 1.0	3.3 2.5	ns

AC WAVEFORMS

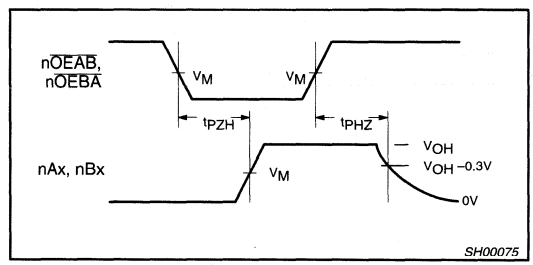
V_M = 1.5V, V_{IN} = GND to 3.0V



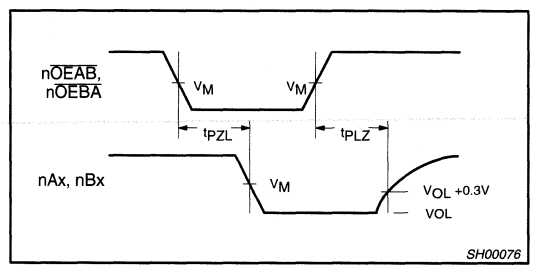
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

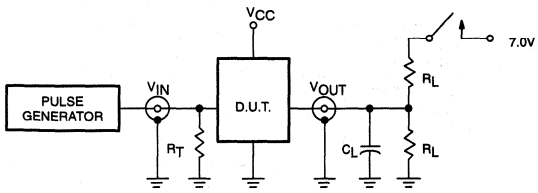


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

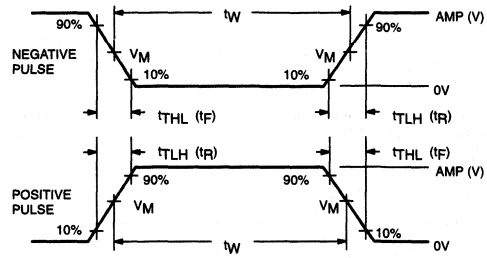


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

16-bit registered transceiver (3-State) MB2052

FEATURES

- Two 8-bit registered transceivers
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Independent registers for A and B buses
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2052 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2052 is a 16-bit registered transceiver. Two 8-bit registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (nCPXX) provided that the Clock Enable (n$\overline{\text{CEXX}}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable (n$\overline{\text{OEXX}}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

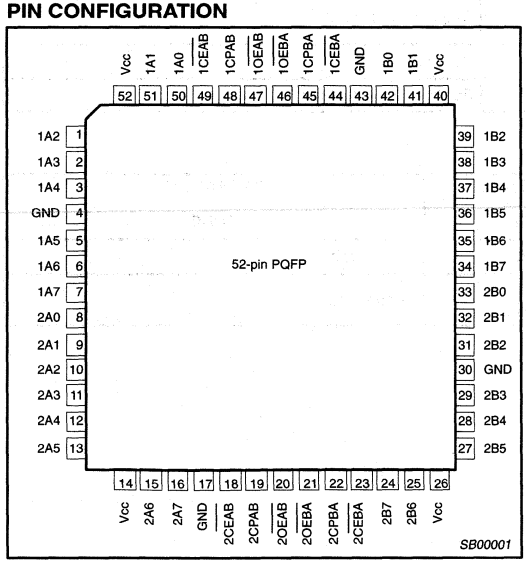
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx or nCPAB to nBx	C_L = 50pF; V_{CC} = 5V	3.7 4.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

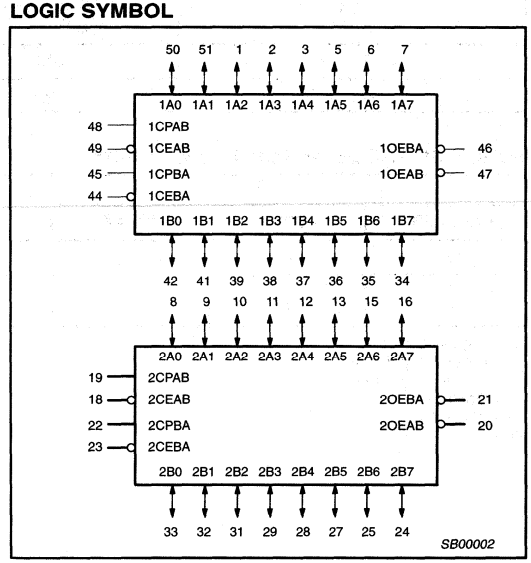
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2052 BB	MB2052 BB	SOT379-1

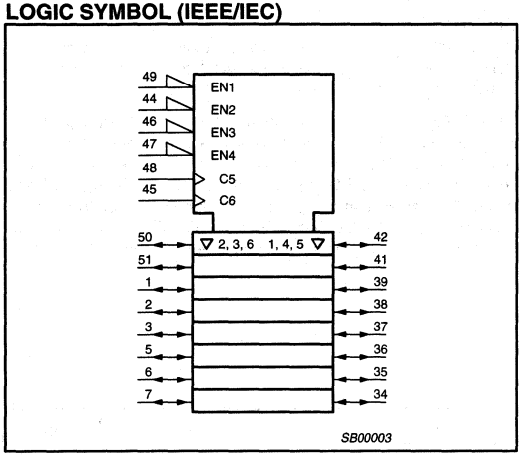
PIN CONFIGURATION

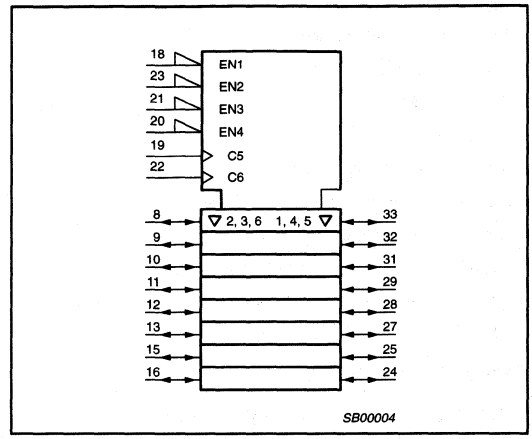


LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)





PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
48, 45 19, 22	1CPAB / 1CPBA 2CPAB / 2CPBA	Clock input A to B / Clock input B to A
49, 44 18, 23	$1\overline{CEAB}$ / $1\overline{CEBA}$ $2\overline{CEAB}$ / $2\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
50, 51, 1, 2, 3, 5, 6, 7 8, 9, 10, 11, 12, 13, 15, 16	1A0 – 1A7 2A0 – 2A7	Data inputs/outputs (A side)
42, 41, 39, 38, 37, 36, 35, 34 33, 32, 31, 29, 28, 27, 25, 24	1B0 – 1B7 2B0 – 2B7	Data inputs/outputs (B side)
47, 46 20, 21	$1\overline{OEAB}$ / $1\overline{OEBA}$ $2\overline{OEAB}$ / $2\overline{OEBA}$	Output enable inputs
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL	OPERATING
nAx or nBx	nCPXX	$n\overline{CEXX}$	Q	MODE
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

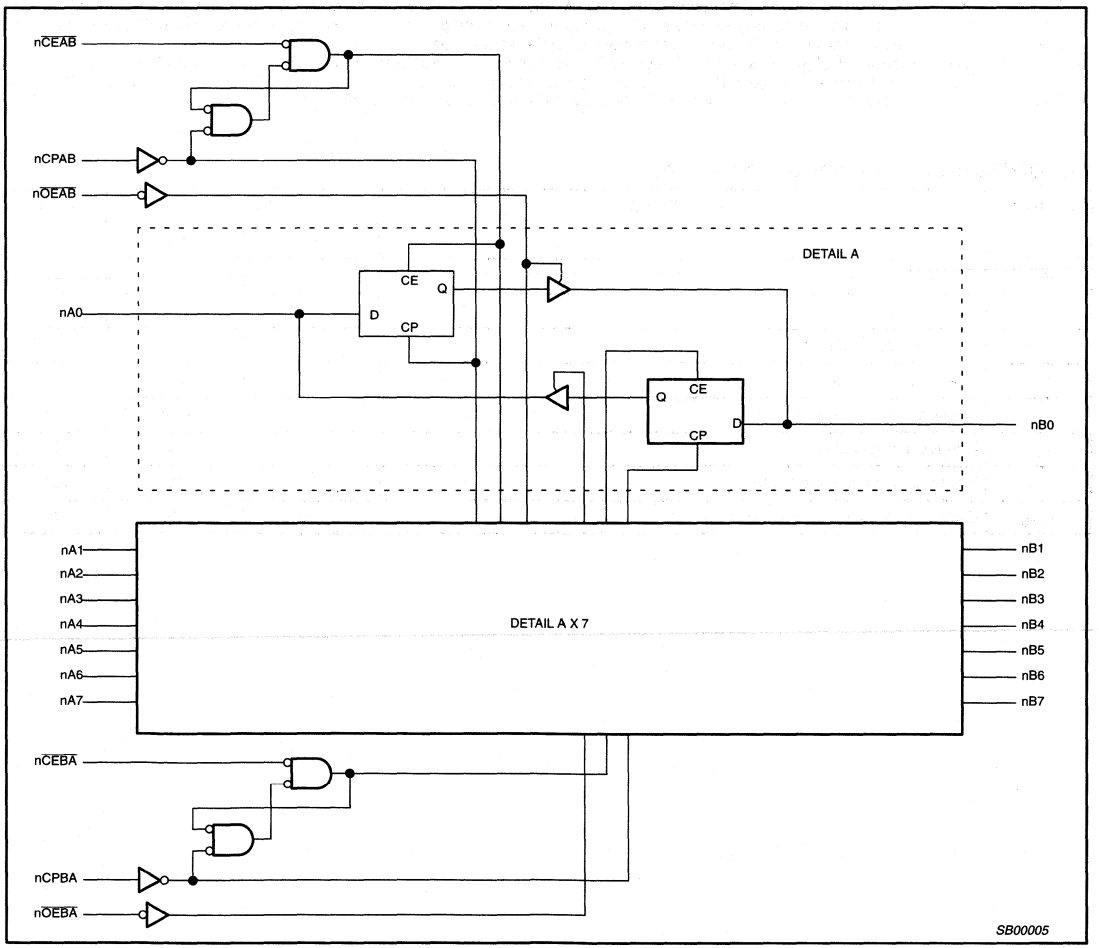
H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	nAx or nBx	OPERATING
$n\overline{OEXX}$	Q	OUTPUTS	MODE
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5V; I_{OL} = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		5	100		100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = Don't care		±5.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{cc}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	−50	−70	−180	−50	−180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		39	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

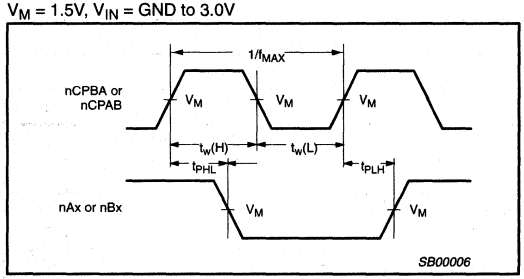
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	200	250		200		MHz
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx, nCPAB to nBx	1	2.1 2.6	3.7 4.1	4.9 5.3	2.1 2.6	5.4 5.8	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OEBA}$ to nAx, $n\overline{OEAB}$ to nBx	3 4	1.2 2.0	2.9 3.7	4.1 5.0	1.2 2.0	4.8 5.8	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OEBA}$ to nAx, $n\overline{OEAB}$ to nBx	3 4	1.0 1.5	3.5 3.0	4.7 4.1	1.0 1.5	5.2 4.6	ns

AC SETUP REQUIREMENTS

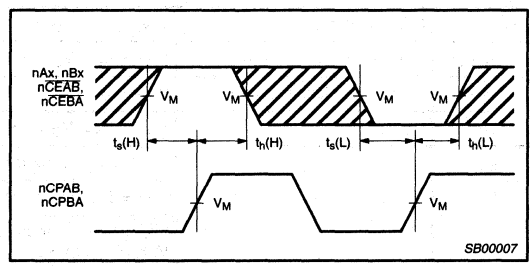
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time nAx to nCPAB or nBx to nCPBA	2	2.5 01.5	0.8 0.0	2.5 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nCPAB or nBx to nCPBA	2	1.5 0.5	0.0 –0.8	1.5 0.5	ns
$t_s(H)$ $t_s(L)$	Setup time n$\overline{CEAB}$ to nCPAB, n$\overline{CEBA}$ to nCPBA	2	3.0 2.0	1.4 0.7	3.0 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time n$\overline{CEAB}$ to nCPAB, n$\overline{CEBA}$ to nCPBA	2	0.5 0.0	–0.7 –1.3	0.5 0.0	ns
$t_w(H)$ $t_w(L)$	nCPAB or nCPBA pulse width, High or Low	1	2.5 3.5	1.4 2.1	2.5 3.5	ns

AC WAVEFORMS

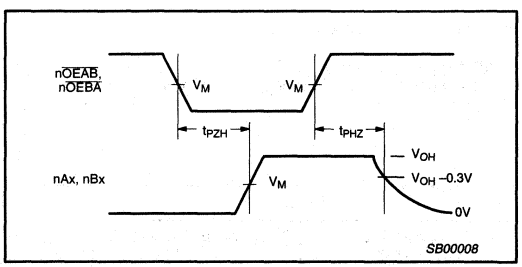
V_M = 1.5V, V_{IN} = GND to 3.0V



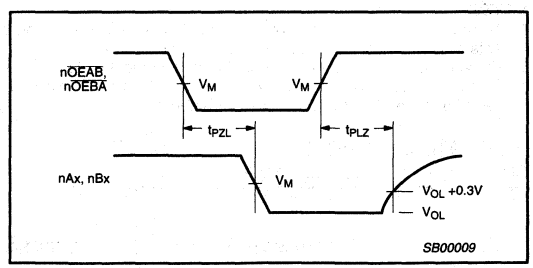
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

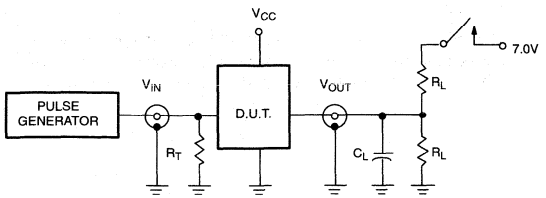


Waveform 2. Data Setup and Hold Times

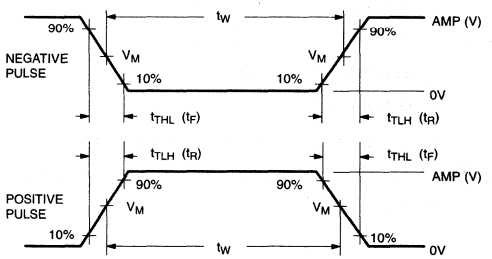


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

16-bit inverting buffer/line driver (3-State) MB2240

FEATURES

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Live insertion/extraction permitted
- Output capability: +64 mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The MB2240 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2240 device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

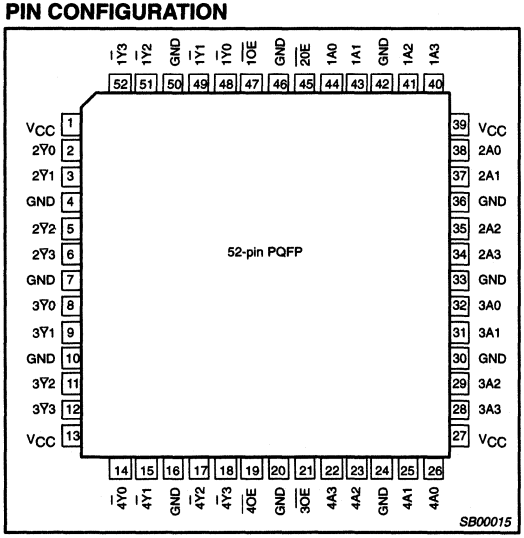
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 5V	3.1 3.5	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC} 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	65	µA

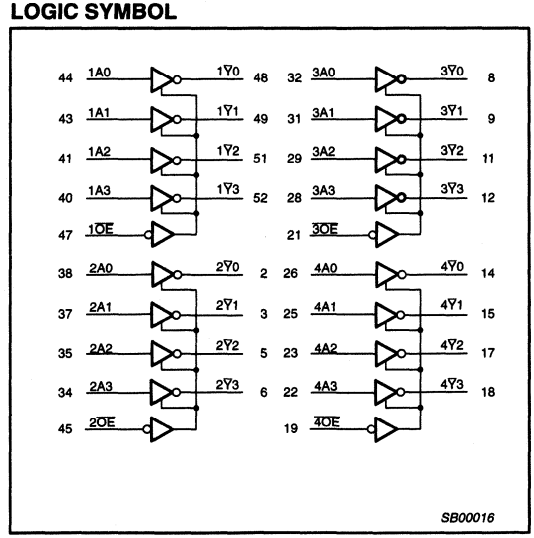
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2240 BB	MB2240 BB	SOT379-1

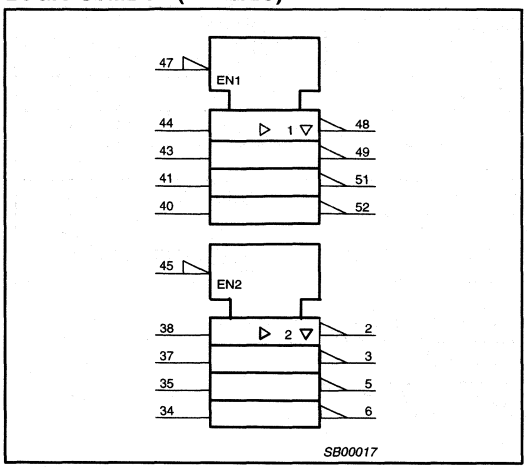
PIN CONFIGURATION

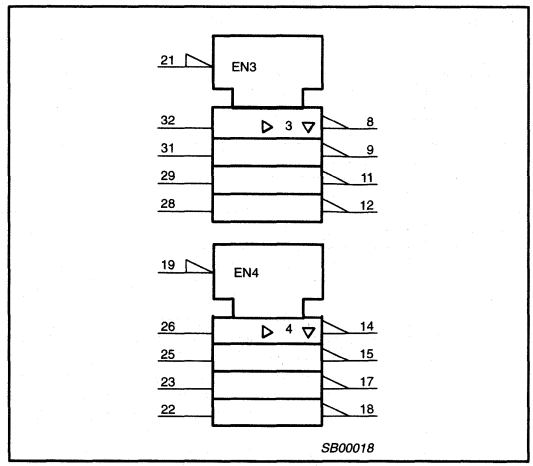


LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)





PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
14, 15, 17, 18, 8, 9, 11, 12, 2, 3, 5, 6, 48, 49, 51, 52	$4\overline{Y}0 - 4\overline{Y}3$, $3\overline{Y}0 - 3\overline{Y}3$, $2\overline{Y}0 - 2\overline{Y}3$, $1\overline{Y}0 - 1\overline{Y}3$	Data outputs
47, 45, 21, 19	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	$n\overline{Y}x$
L	L	H
L	H	L
H	X	Z

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PU}	Power-up/down 3-state output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}, V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3–State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3–State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−70	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		65	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		65	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

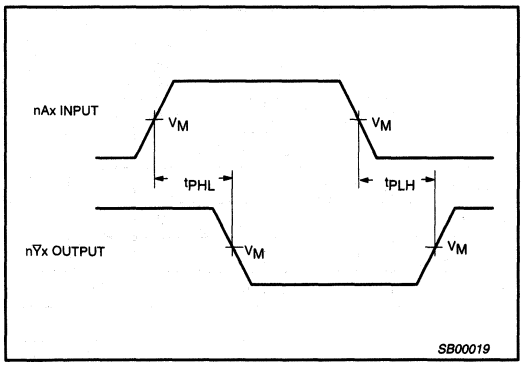
NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10µsec from V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

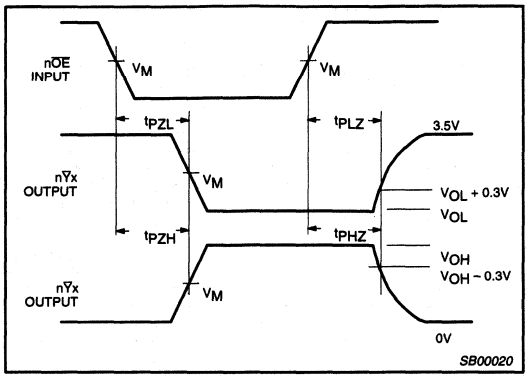
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1.0 1.4	3.1 3.5	4.5 4.5	1.0 1.4	5.1 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.4	3.2 4.1	4.3 5.2	1.1 1.4	5.2 6.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.2 1.3	4.0 3.6	5.1 4.8	1.2 1.3	5.8 5.5	ns

AC WAVEFORMS

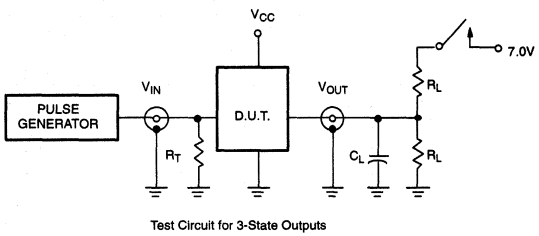


Waveform 1. Waveforms Showing the Input (An) to Output (Ȳn) Propagation Delays

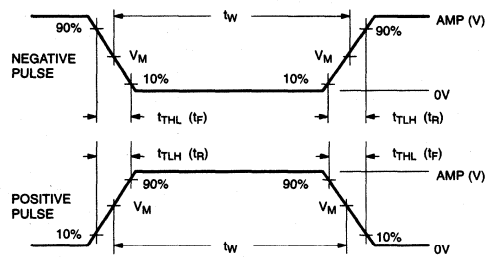


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



VM = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

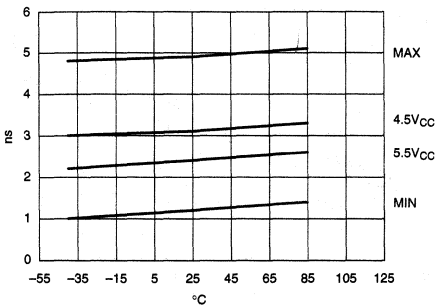
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

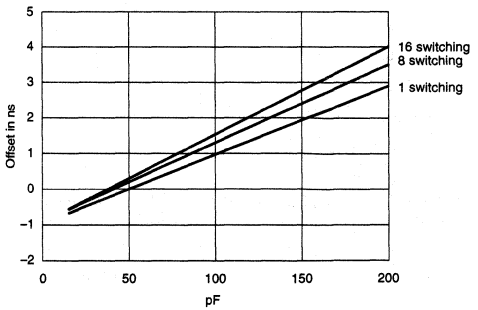
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

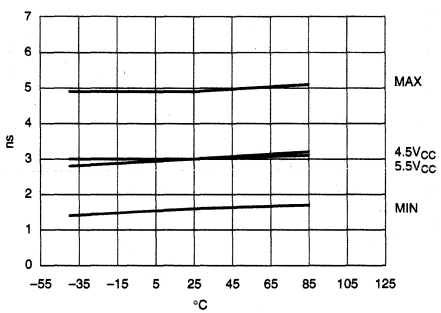
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to n$\overline{Y}$x



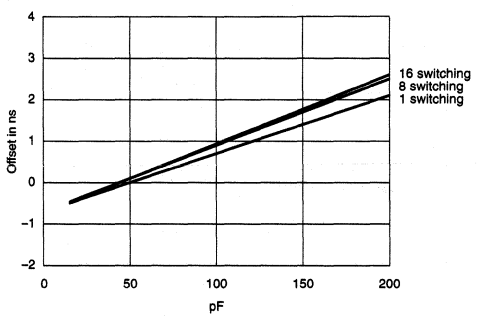
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nAx to n$\overline{Y}$x



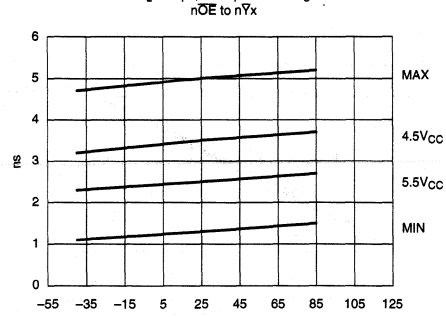
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to n$\overline{Y}$x



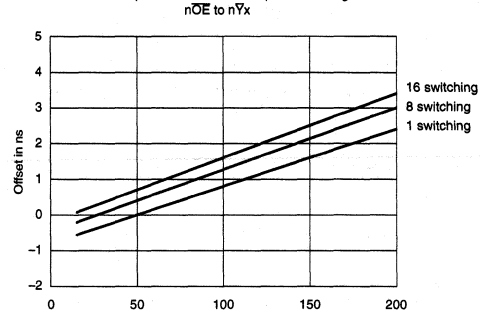
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nAx to n$\overline{Y}$x



t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to n$\overline{Y}$x

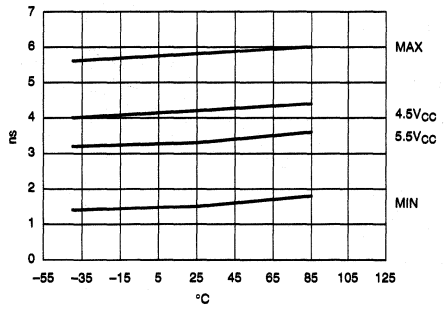


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to n$\overline{Y}$x

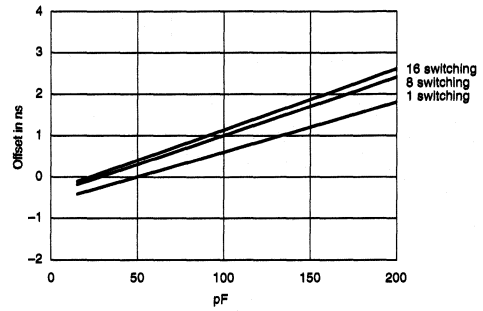


SB00021

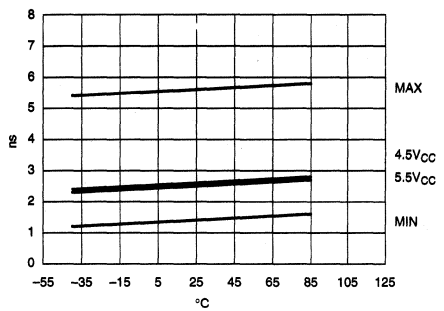
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to $n\overline{Y}x$



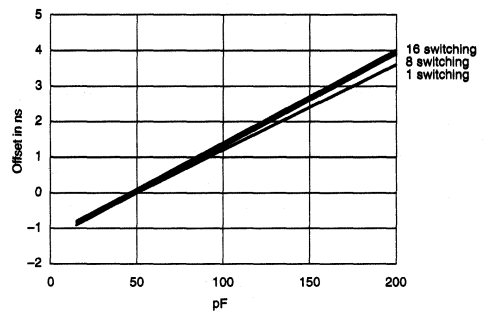
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to $n\overline{Y}x$



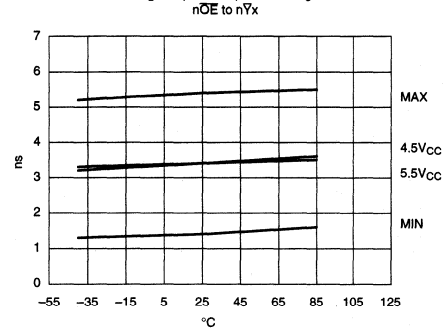
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to $n\overline{Y}x$



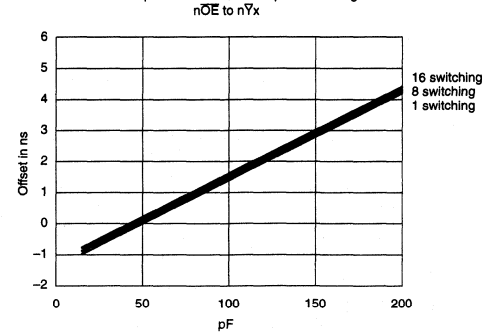
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to $n\overline{Y}x$



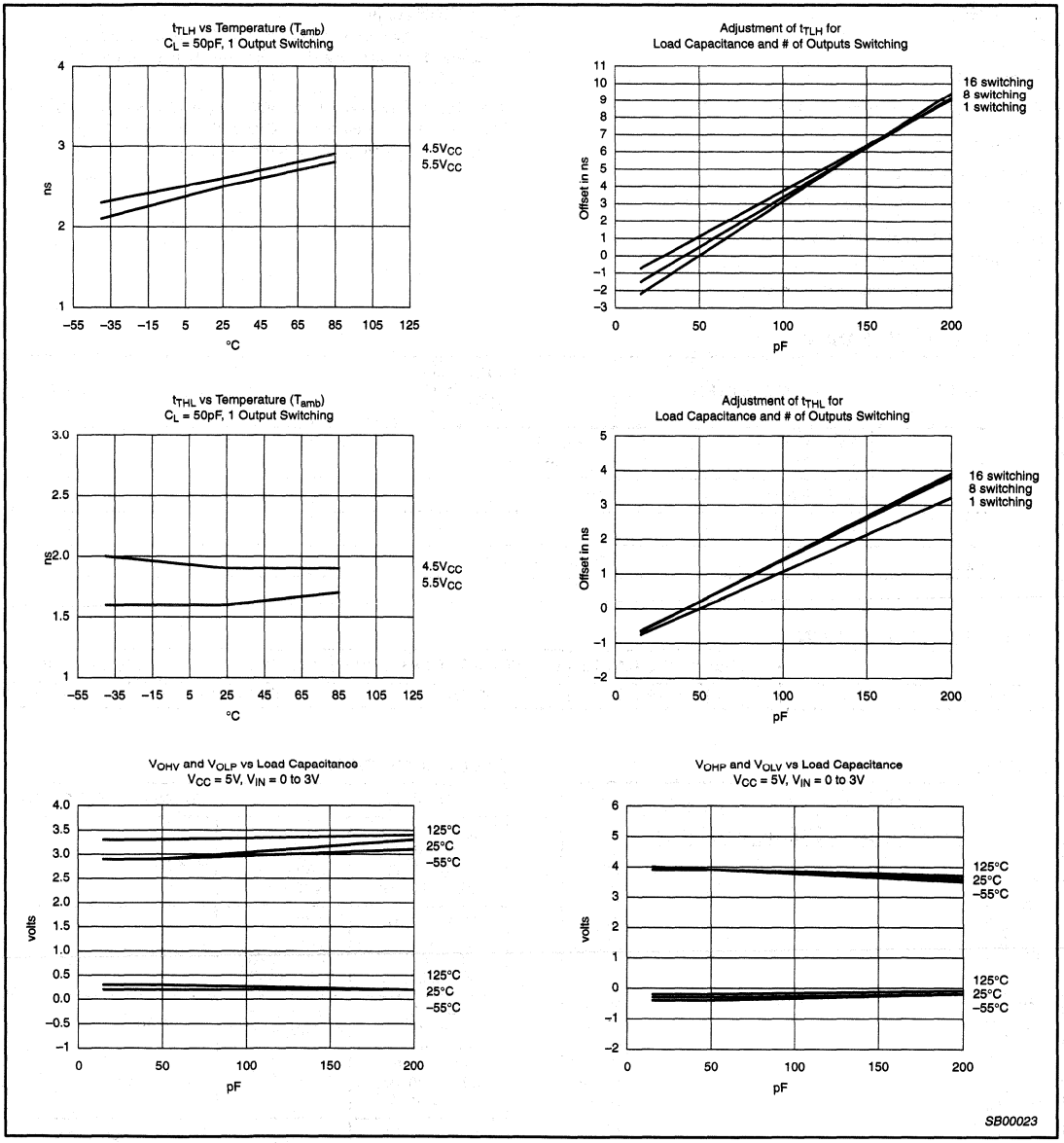
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to $n\overline{Y}x$



Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to $n\overline{Y}x$



SB00022


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
SB00023

16-bit buffer/line driver (3-State) MB2241

FEATURES

- 16–bit bus interface
- Power 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Inputs are disabled during 3-State mode

DESCRIPTION

The MB2241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2241 device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, 2OE, $3\overline{OE}$, 4OE), each controlling four of the 3-State outputs.

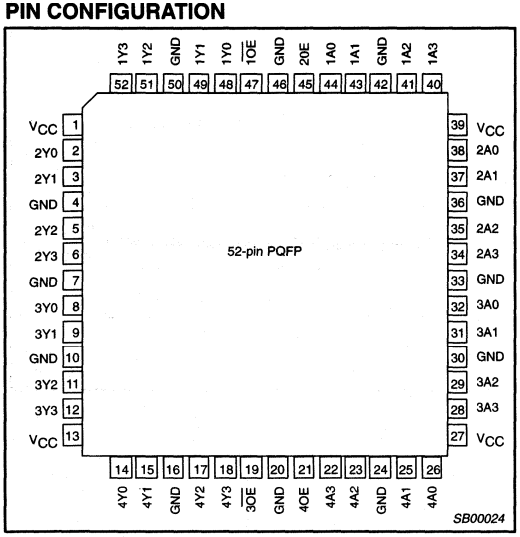
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	3.0 3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	65	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2241 BB	MB2241 BB	SOT379-1

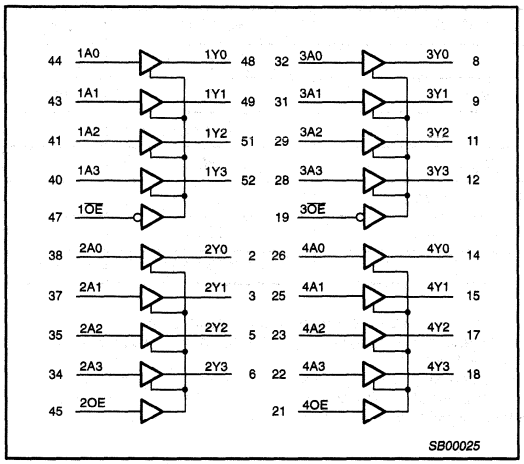
PIN CONFIGURATION



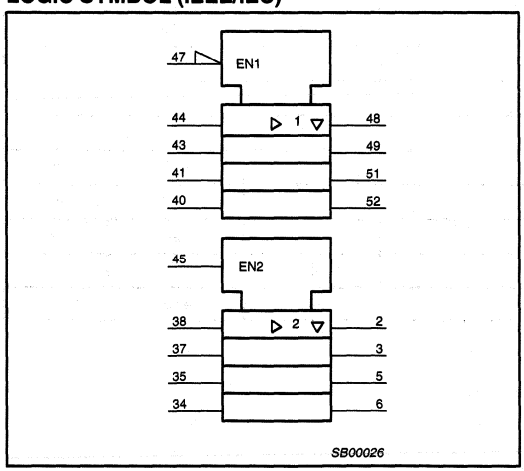
PIN DESCRIPTION

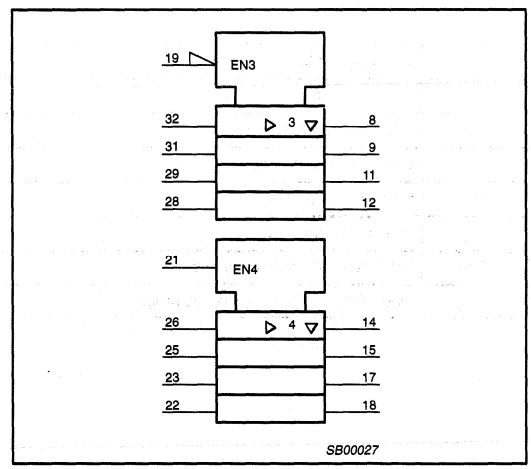
PIN NUMBER	SYMBOL	NAME AND FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
14, 15, 17, 18, 8, 9, 11, 12, 2, 3, 5, 6, 48, 49, 51, 52	4Y0 – 4Y3, 3Y0 – 3Y3, 2Y0 – 2Y3, 1Y0 – 1Y3	Data outputs
47, 45, 21, 19	$1\overline{OE}$, 2OE, $3\overline{OE}$, 4OE	Output enables
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)





FUNCTION TABLE

INPUTS				OUTPUTS	
1$\overline{OE}$ or 3$\overline{OE}$	1An or 3An	2OE or 4OE	2An or 4An	1Yn or 3Yn	2Yn or 4Yn
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
Z = High voltage level-impedance "OFF" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PU}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}; V_{OE} = GND		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		65	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		65	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

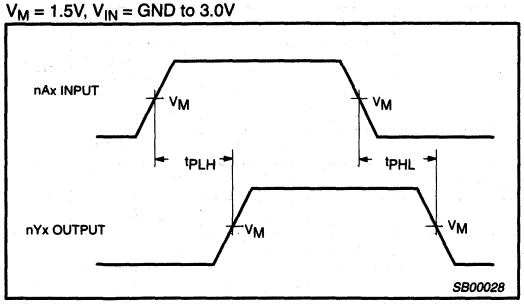
AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

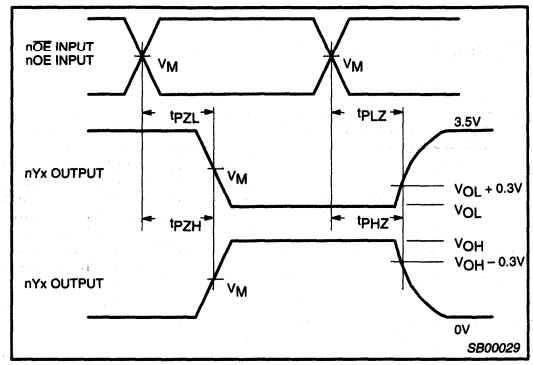
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.2 1.2	3.0 3.1	4.5 4.5	1.2 1.2	5.1 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 1.8	3.7 4.8	6.3 6.8	1.3 1.8	6.9 7.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.3 1.2	3.9 3.4	5.9 5.2	1.3 1.2	6.7 5.8	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

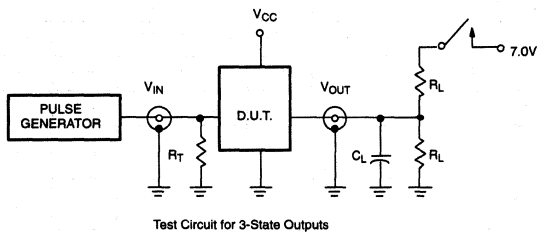


Waveform 1. Waveforms Showing the Input (nAx) to Output (nYx) Propagation Delays

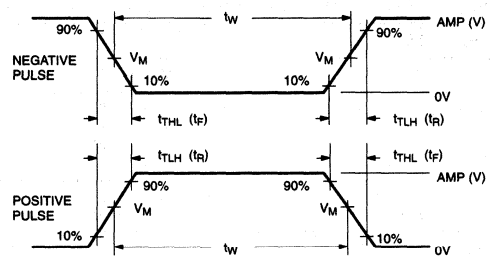


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

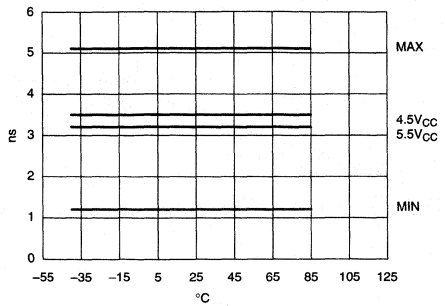
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

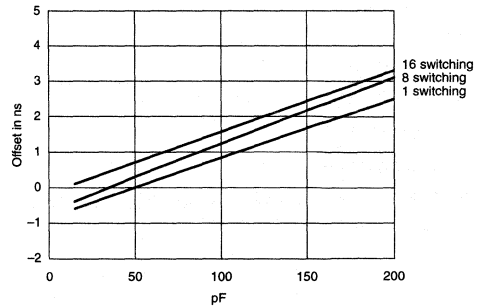
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

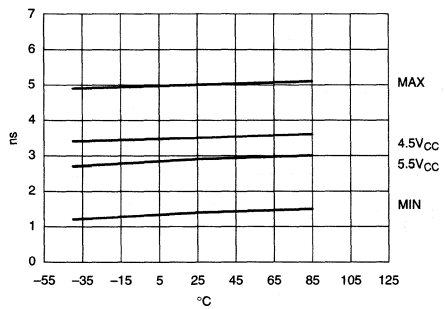
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nYx



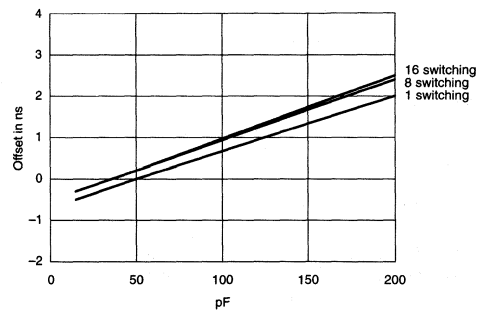
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nAx to nYx



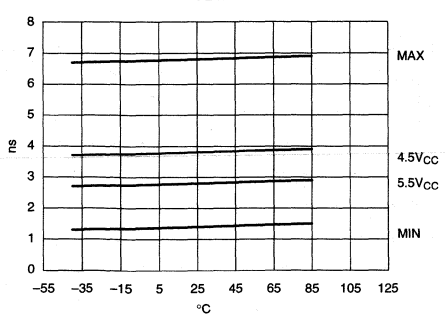
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nYx



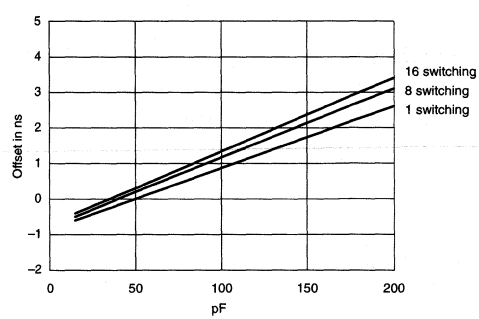
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nAx to nYx



t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nYx

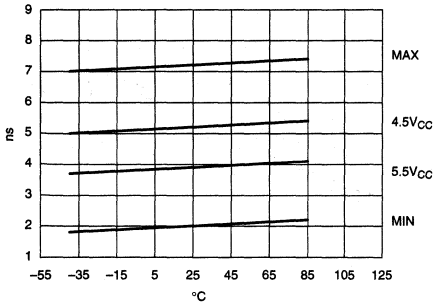


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nYx

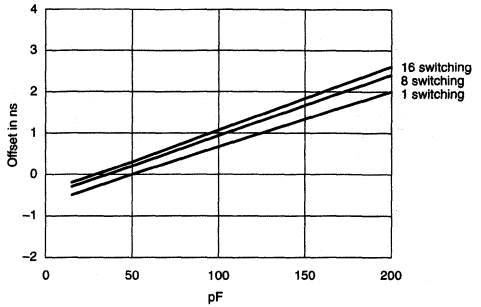


SB00030

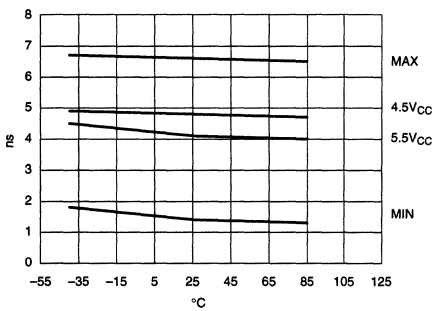
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nYx



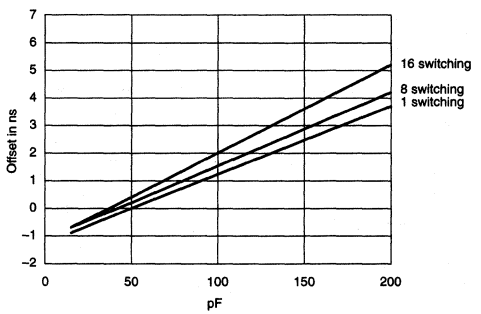
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nYx



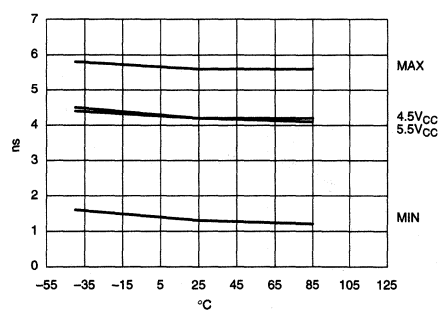
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nYx



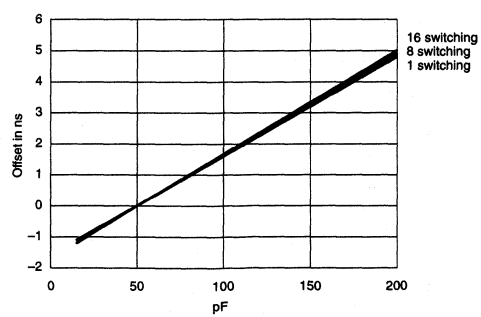
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nYx



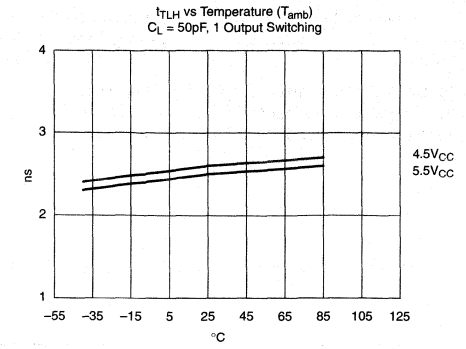
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nYx

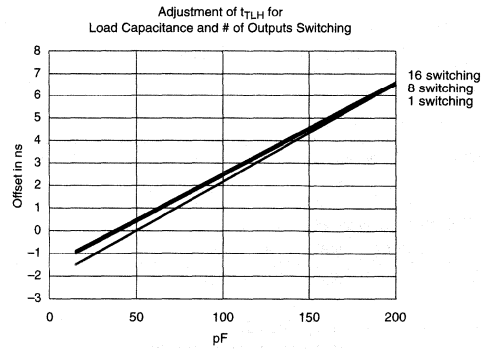


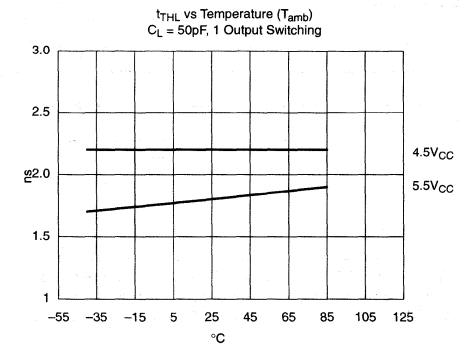
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nYx

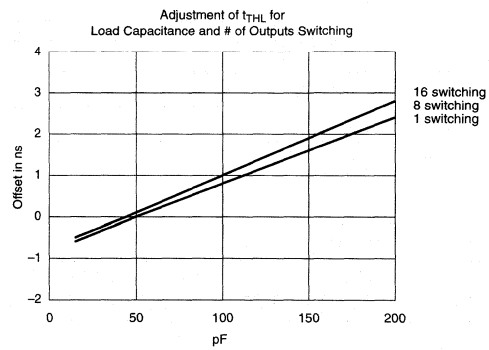


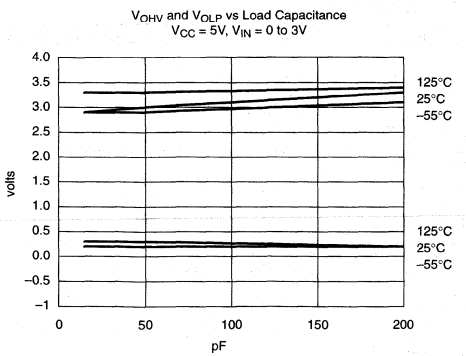
SB00031

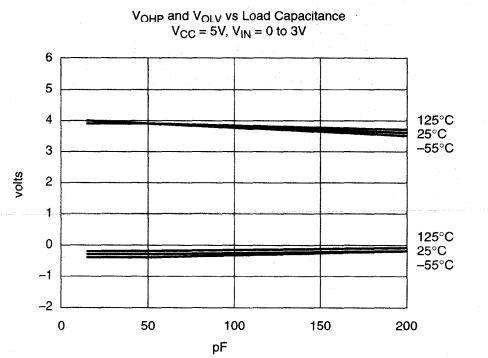

t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}


Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching


t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}


Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching


V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C


V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C

SB00032

16-bit buffer/line driver (3-State) — MB2244

FEATURES

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- 3-State buffers
- Output capability: +64 mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Inputs are disabled during 3-State mode

DESCRIPTION

The MB2244 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2244 device is an 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

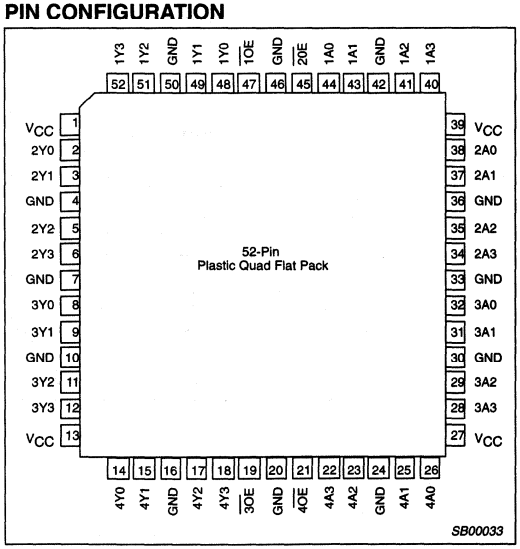
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	3.2 3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2244 BB	MB2244 BB	SOT379-1

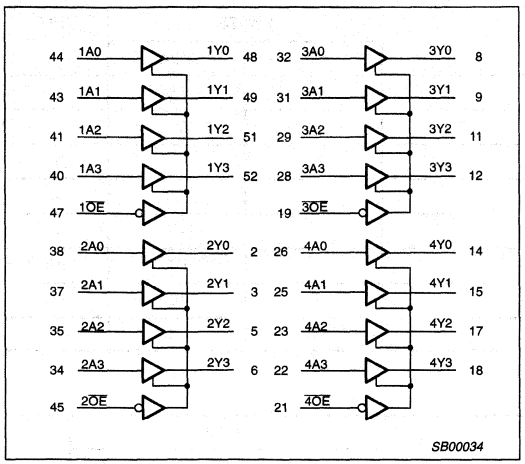
PIN CONFIGURATION



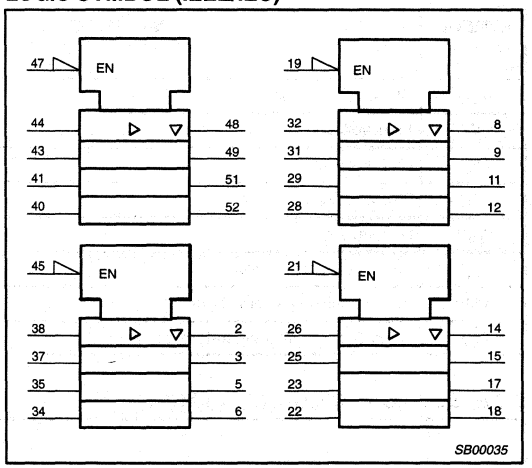
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1Y0 – 1Y3, 2Y0 – 2Y3, 3Y0 – 3Y3, 4Y0 – 4Y3	Data outputs
47, 45, 19, 21	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

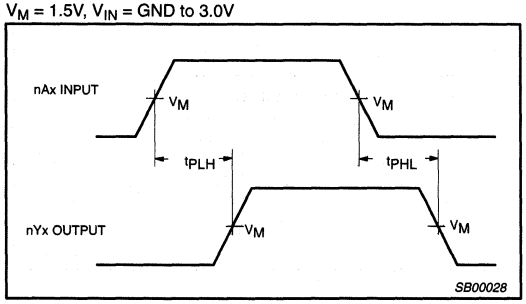
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

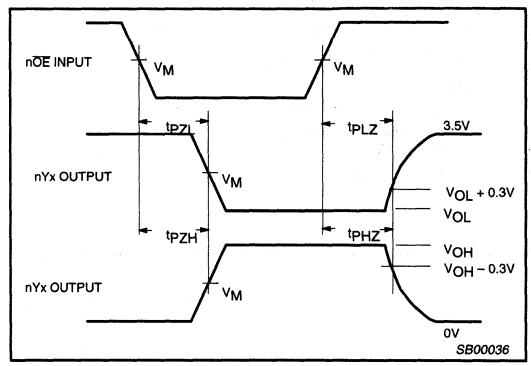
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.2 1.2	3.2 3.1	4.5 4.5	1.2 1.2	5.1 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.8	3.0 4.0	4.4 5.4	1.1 1.8	5.1 6.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.6 1.7	4.0 3.4	5.6 5.0	1.6 1.7	6.2 5.6	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

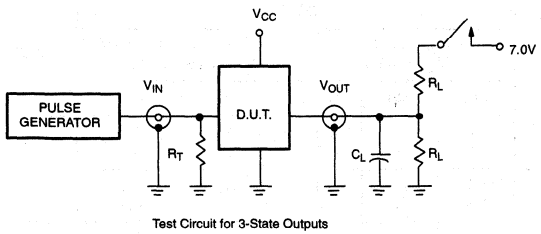


Waveform 1. Input (An) to Output (Yn) Propagation Delays

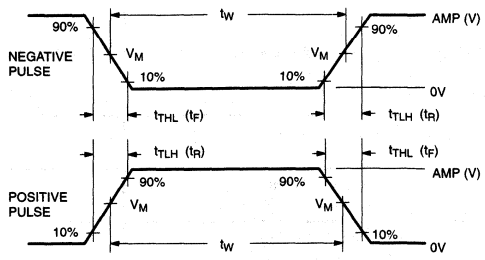


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

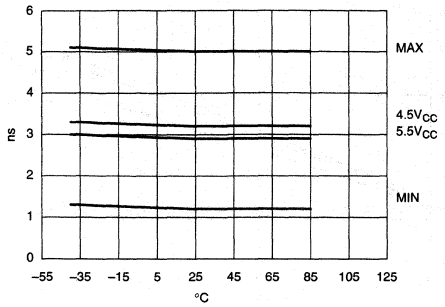
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

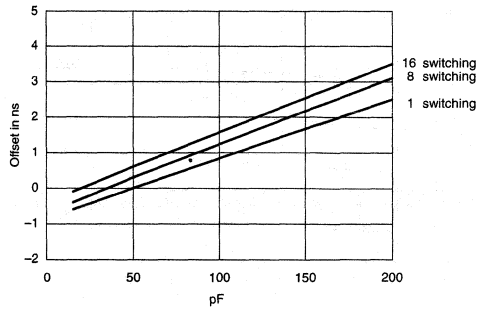
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

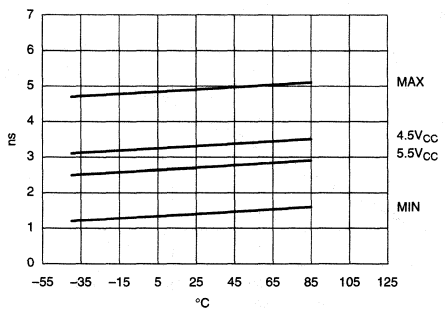
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nYx



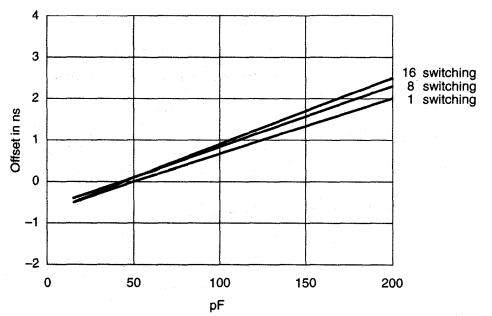
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nAx to nYx



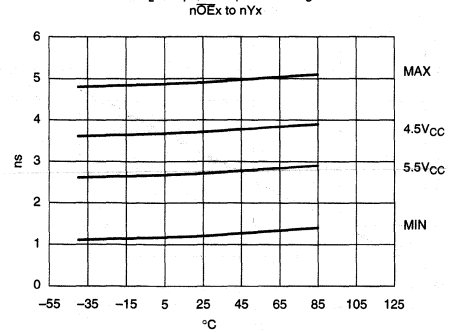
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nYx



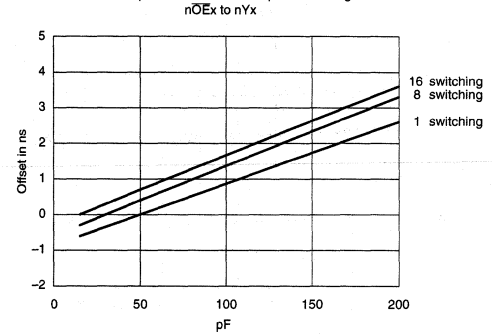
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nAx to nYx



t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}x$ to nYx

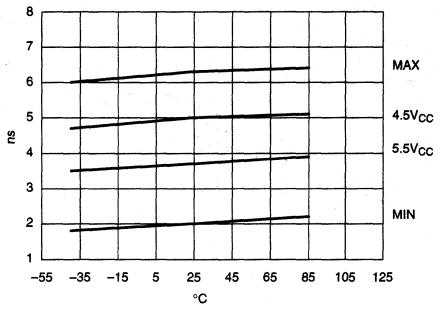


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}x$ to nYx

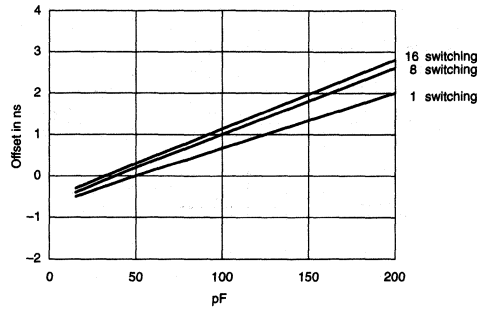


SB00037

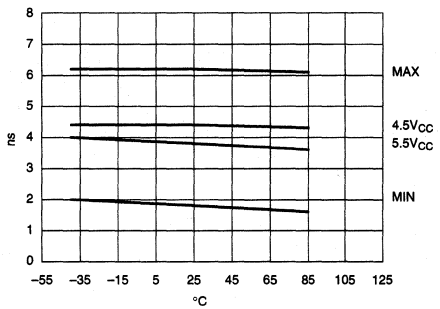
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$x to nYx



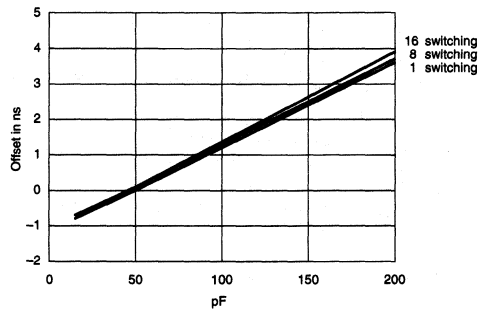
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$x to nYx



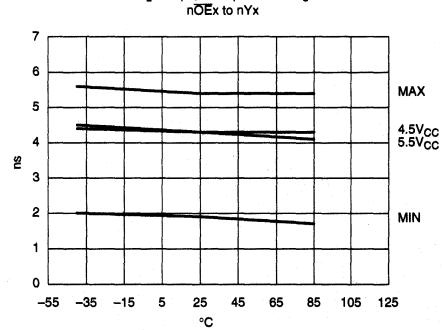
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$x to nYx



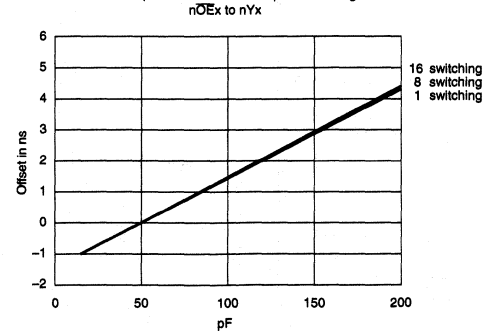
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$x to nYx



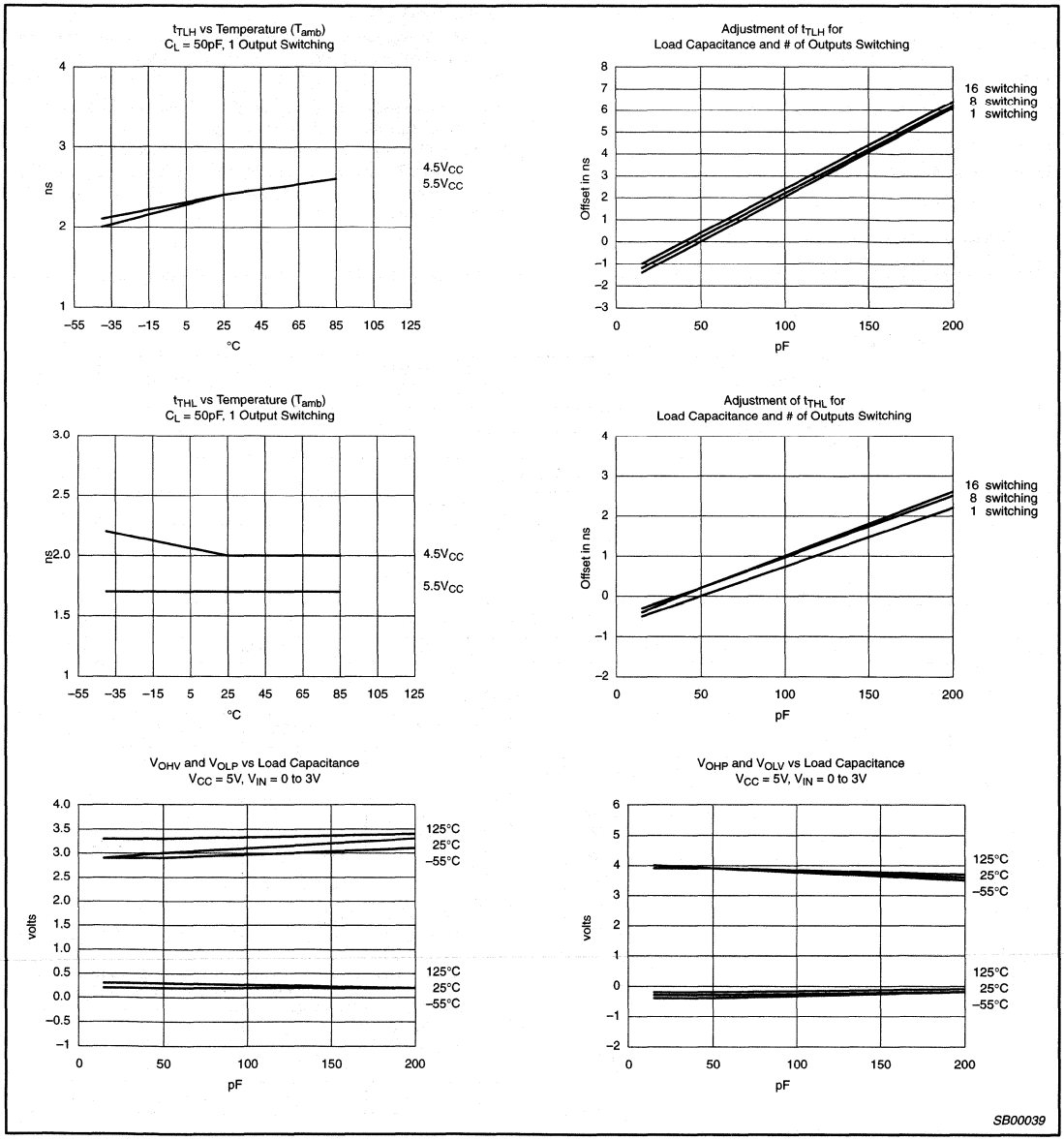
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$x to nYx



Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$x to nYx



SB00038


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
SB00039

16-bit transceiver with direction pins (3-State) — MB2245

FEATURES

- 16-bit bidirectional bus interface
- Power–up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64 mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200V per Machine Model
- Inputs are disabled during 3-State mode

DESCRIPTION

The MB2245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2245 device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable ($1\overline{OE}$, $2\overline{OE}$) inputs for easy cascading and two Direction (1DIR, 2DIR) inputs for direction control.

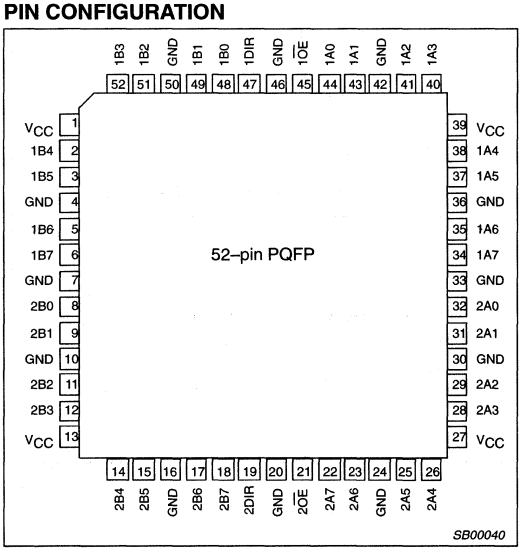
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 5V	3.2 3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	65	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2245 BB	MB2245 BB	SOT379-1

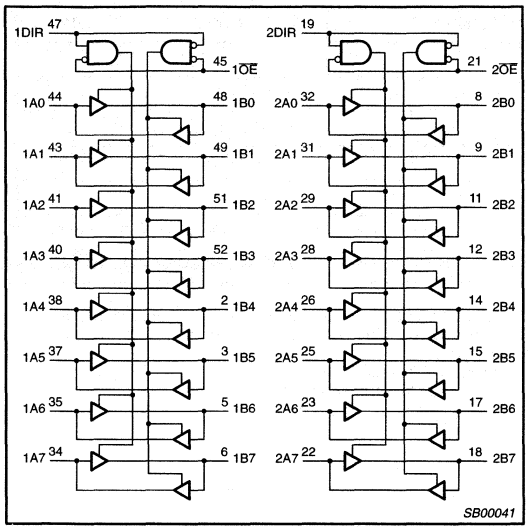
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 19	1DIR, 2DIR	Direction control inputs (Active-High)
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1B0 – 1B7, 2B0 – 2B7	Data outputs/outputs (B side)
45, 21	$1\overline{OE}$, $2\overline{OE}$	Output enable (Active-Low)
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

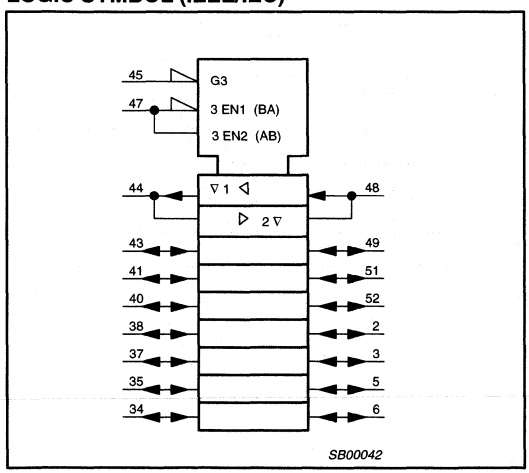
LOGIC SYMBOL

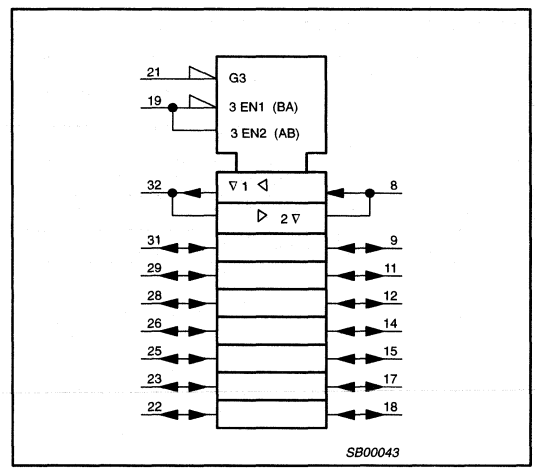


FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
nOE	**nDIR**	**nAx**	**nBx**
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

LOGIC SYMBOL (IEEE/IEC)





ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PU}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		65	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		65	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

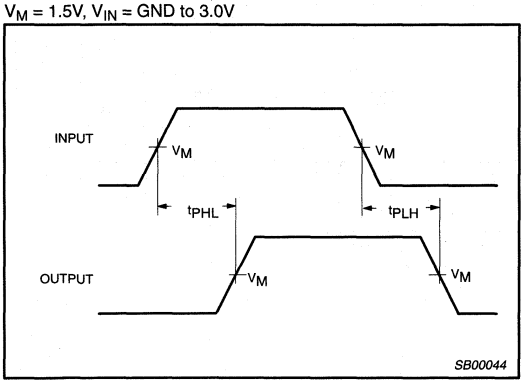
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

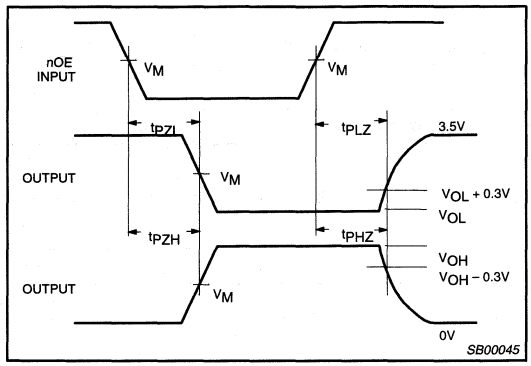
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.2 1.2	3.2 3.1	4.5 4.5	1.2 1.2	5.1 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	2.1 2.4	3.8 4.7	5.2 6.1	2.1 2.4	5.8 7.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.1 2.1	4.5 4.0	5.8 5.3	2.1 2.1	6.4 5.9	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

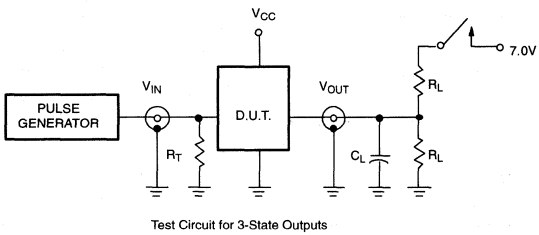


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

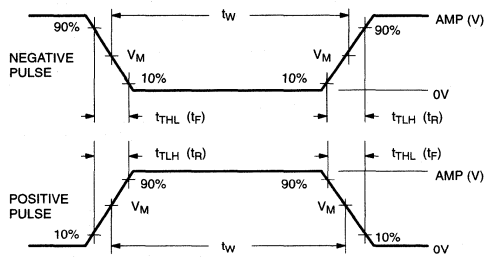


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

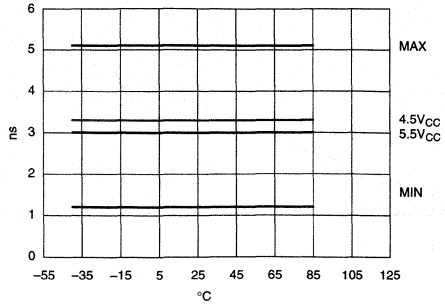
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

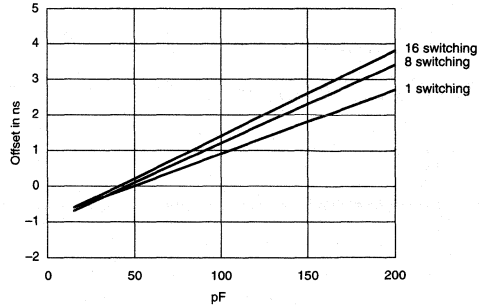
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

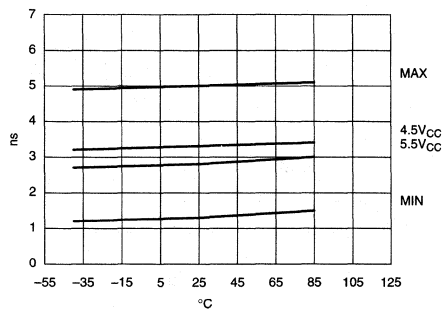
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx



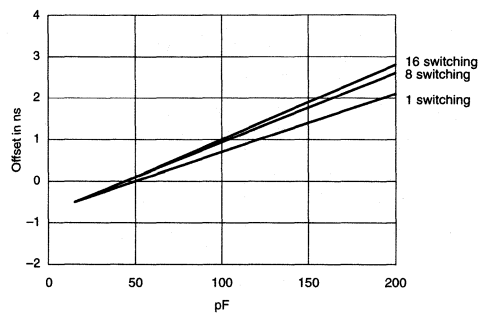
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nAx to nBx



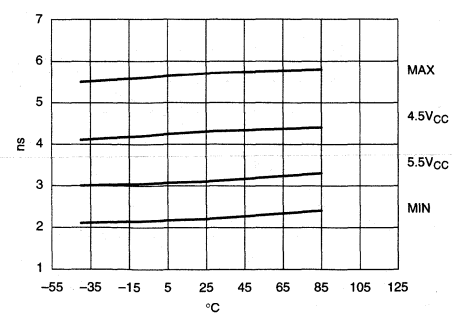
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx



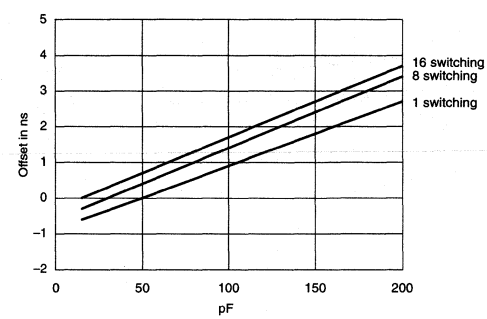
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nAx to nBx



t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$x to nBx

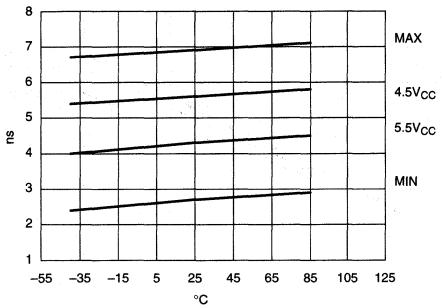


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$x to nBx

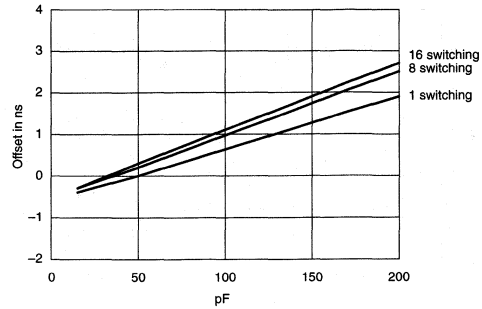


SB00046

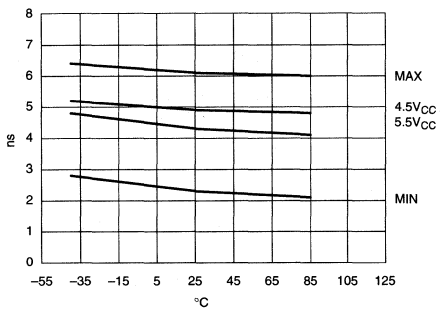
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}x$ to nBx



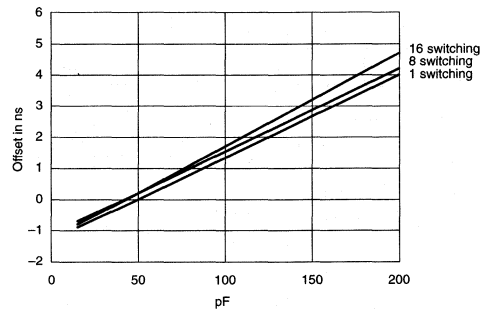
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}x$ to nBx



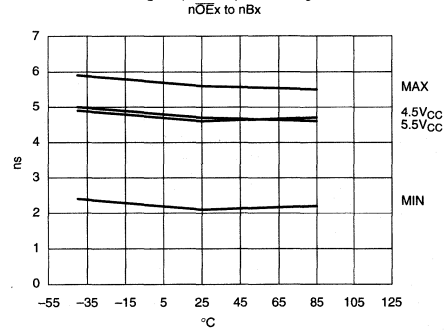
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}x$ to nBx



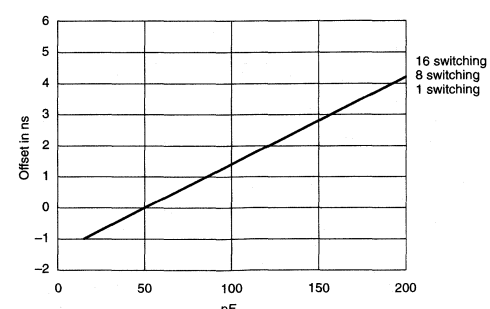
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}x$ to nBx



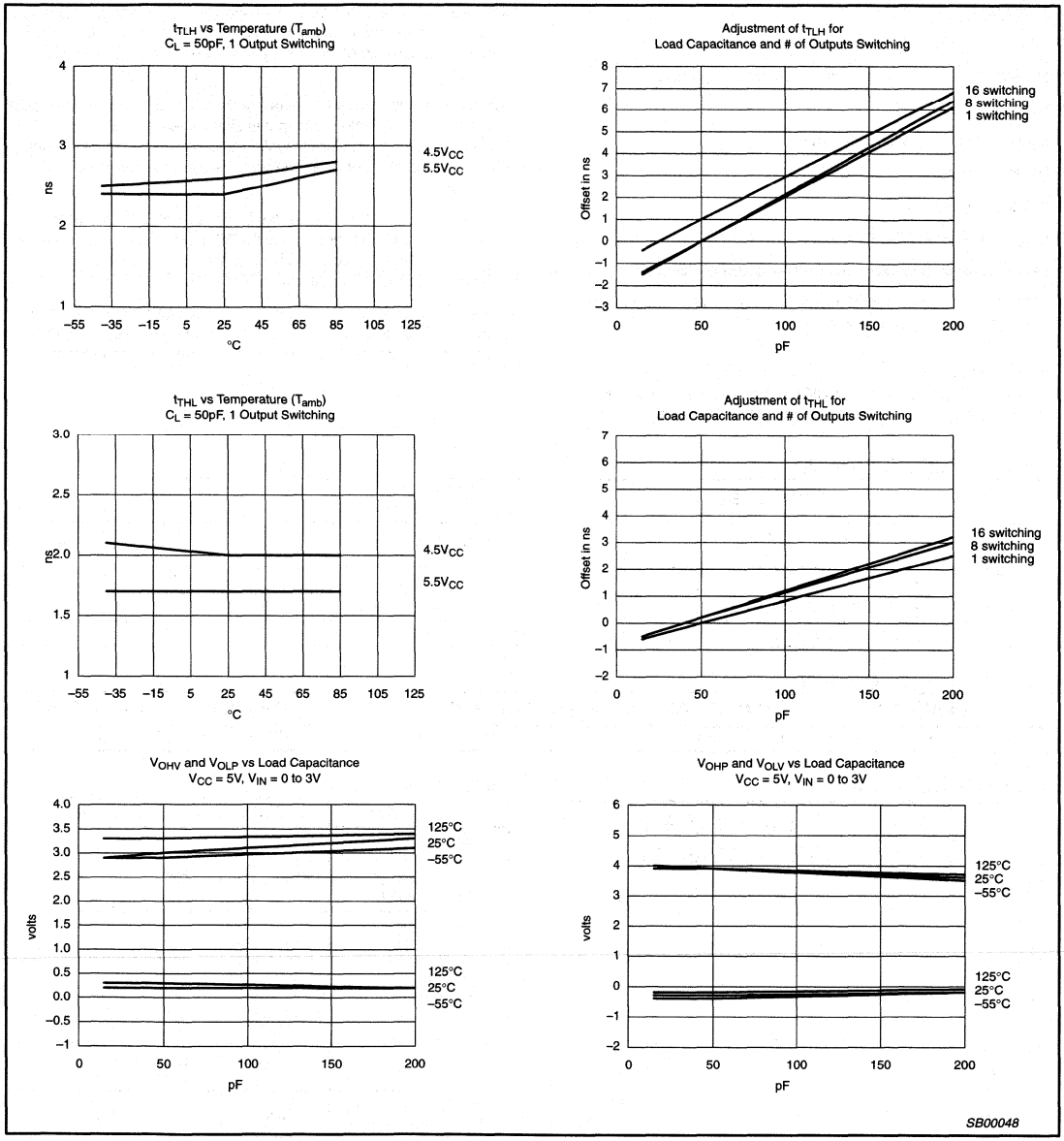
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}x$ to nBx



Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}x$ to nBx



SB00047


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
SB00048

16-bit transparent latch (3-State) — MB2373

FEATURES

- 16-bit transparent latch
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- Live insertion/extraction permitted
- Power-up reset
- 3-State output buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2373 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2373 device is a 16-bit transparent latch coupled to two sets of eight 3-State output buffers. The two sections of the device are controlled independently by Enable (nE) and Output Enable ($n\overline{OE}$) control gates.

The data on each set of D inputs are transferred to the latch outputs when the Latch Enable (nE) input is High. The latch remains transparent to the data inputs while nE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-Low Output Enable ($n\overline{OE}$) controls eight 3-State buffers independent of the latch operation.

When $n\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $n\overline{OE}$ is High, the outputs are in the High–impedance "OFF" state, which means they will neither drive nor load the bus.

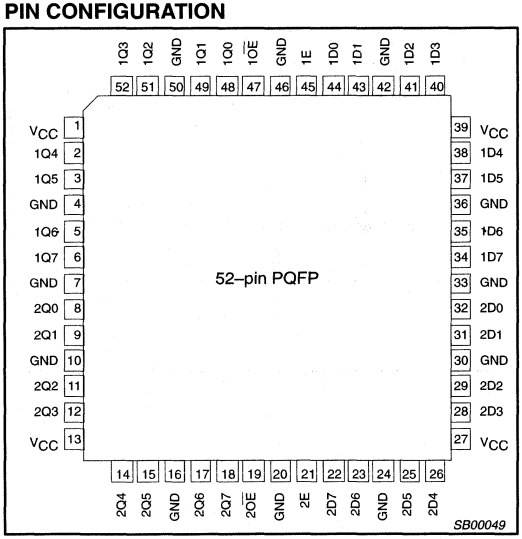
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 5V	2.8 2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2373 BB	MB2373 BB	SOT379-1

PIN CONFIGURATION

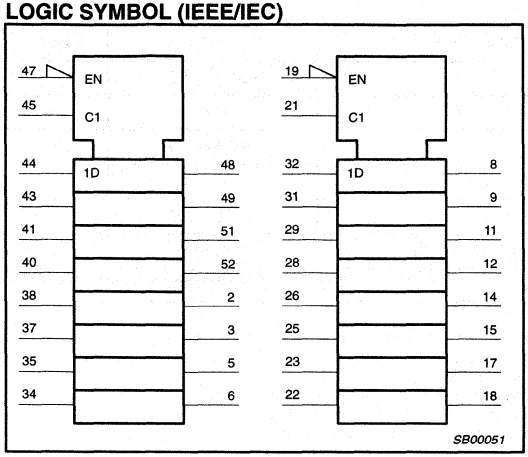


PIN DESCRIPTION

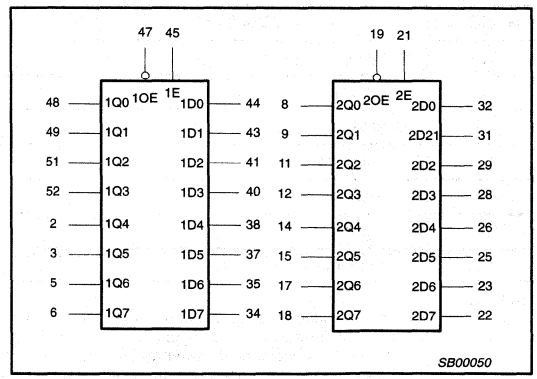
PIN NUMBER	SYMBOL	FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1D0 – 1D7 2D0 – 2D7	Data inputs
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
47, 19	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active–Low)
45, 21	1E, 2E	Enable inputs (active–High)
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

16-bit transparent latch (3-State) MB2373

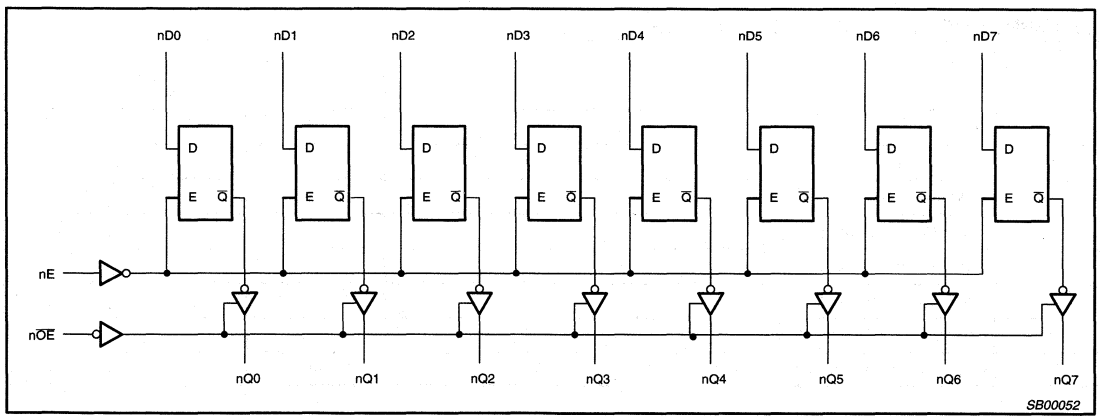
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
nOE	nE	nDx	REGISTER	nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = GND		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−70	−180	−50	−180	mA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		44	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

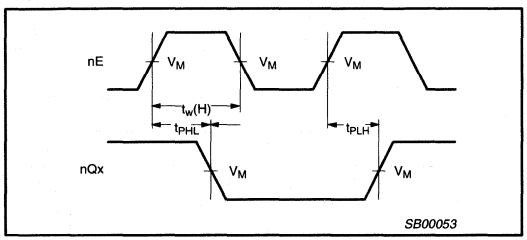
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.3 1.3	2.8 2.9	4.1 4.1	1.3 1.3	4.8 4.8	ns
t_{PLH} t_{PHL}	Propagation delay nE to nQx	1	1.8 2.0	3.5 3.5	4.9 4.9	1.8 2.0	5.7 5.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.2 2.1	2.9 3.8	4.1 5.3	1.2 2.1	5.1 6.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.4 2.0	3.7 3.6	5.0 4.6	1.4 2.0	5.5 5.1	ns

AC SETUP REQUIREMENTS

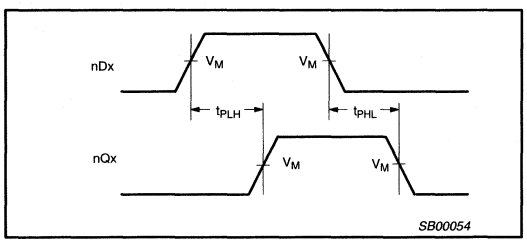
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nE	3	1.0 1.0	0.0 0.3	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nE	3	0.5 0.5	–0.2 0.0	0.5 0.5	ns
$t_w(H)$	Enable pulse width High	1	2.5	1.0	2.5	ns

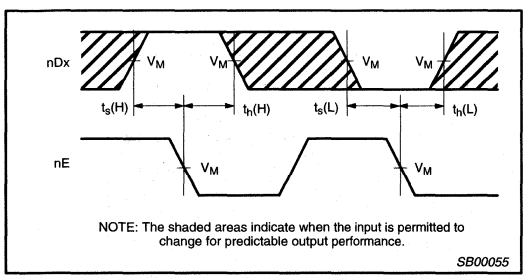
AC WAVEFORMS



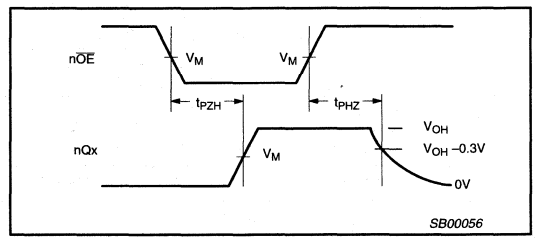
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



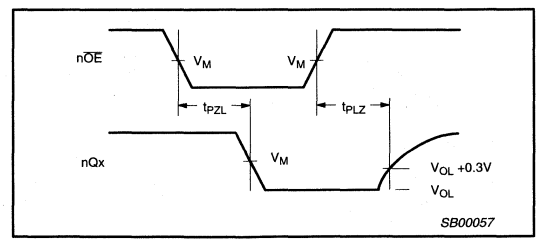
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

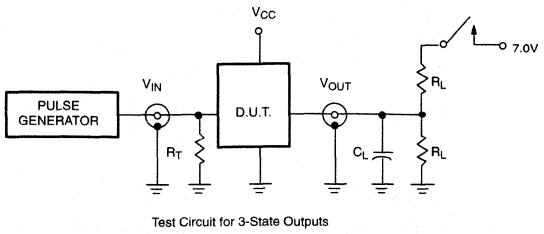


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

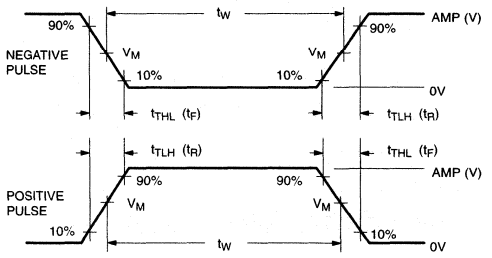


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

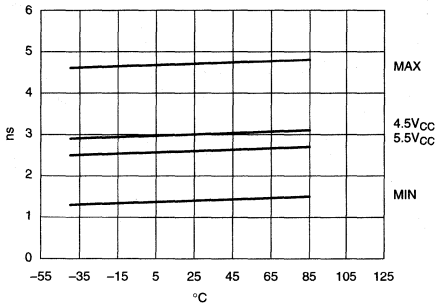
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

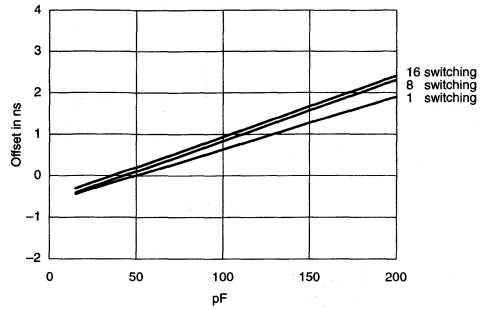
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

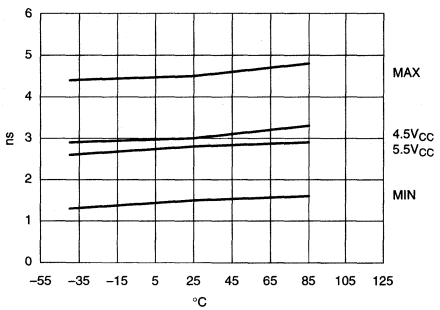
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nDx to nQx



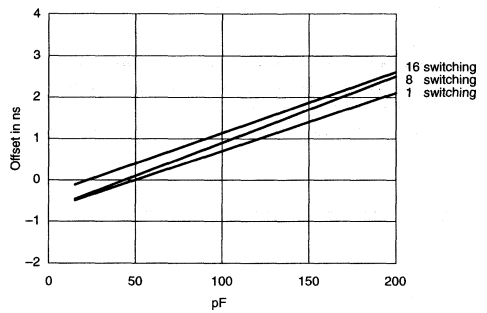
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nDx to nQx



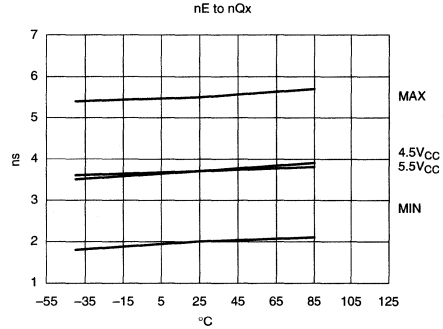
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nDx to nQx



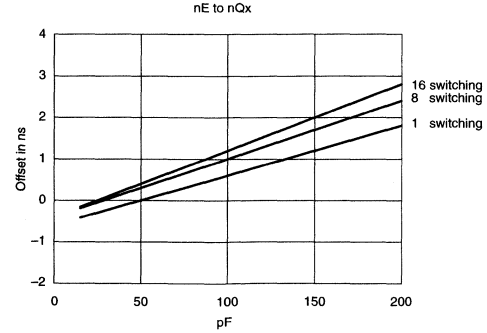
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nDx to nQx



t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nE to nQx

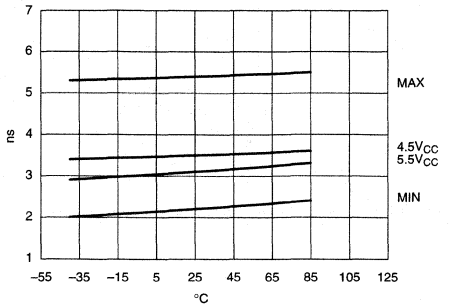


Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nE to nQx

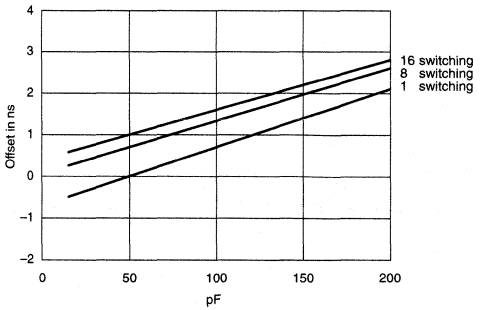


SB00058

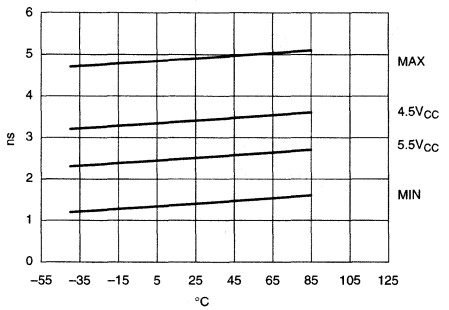
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nE to nQx



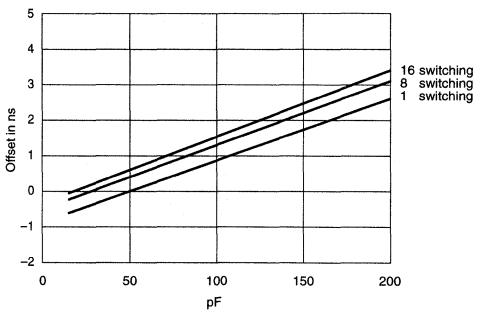
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nE to nQx



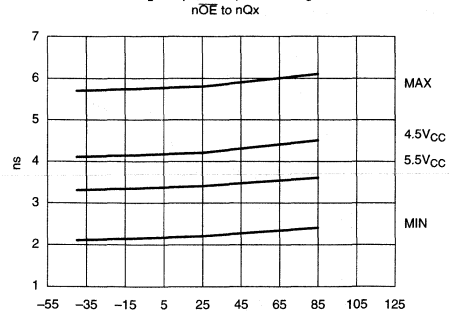
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx



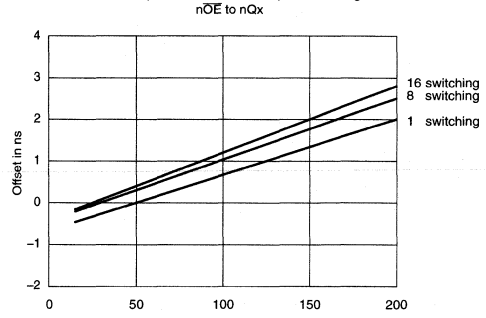
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx

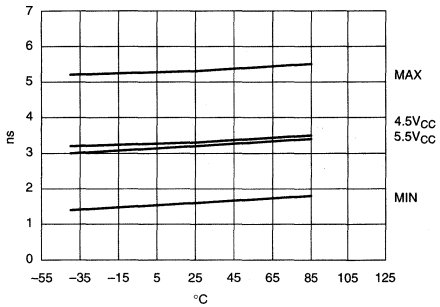


Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx

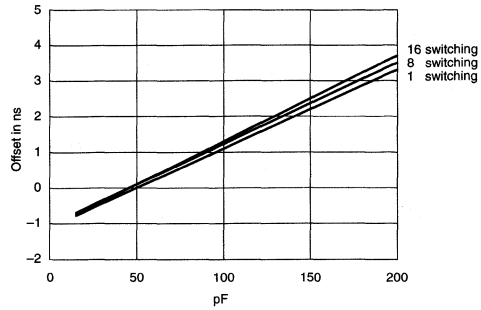


SB00059

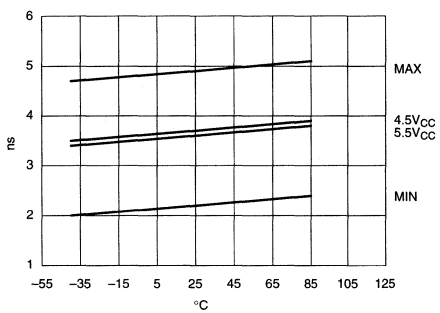
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



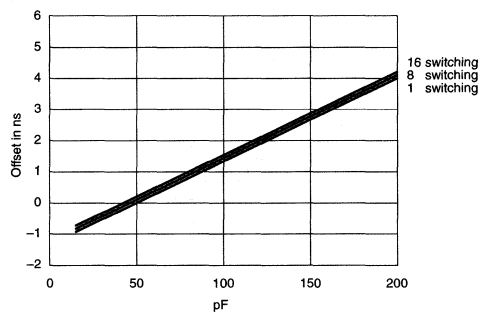
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



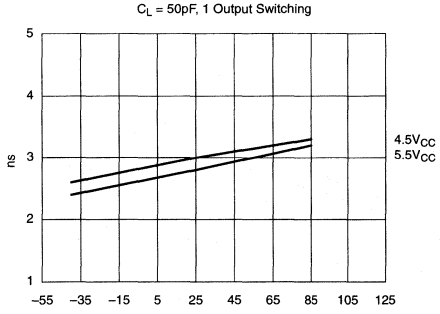
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



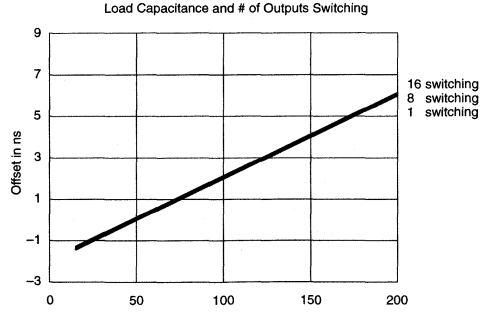
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



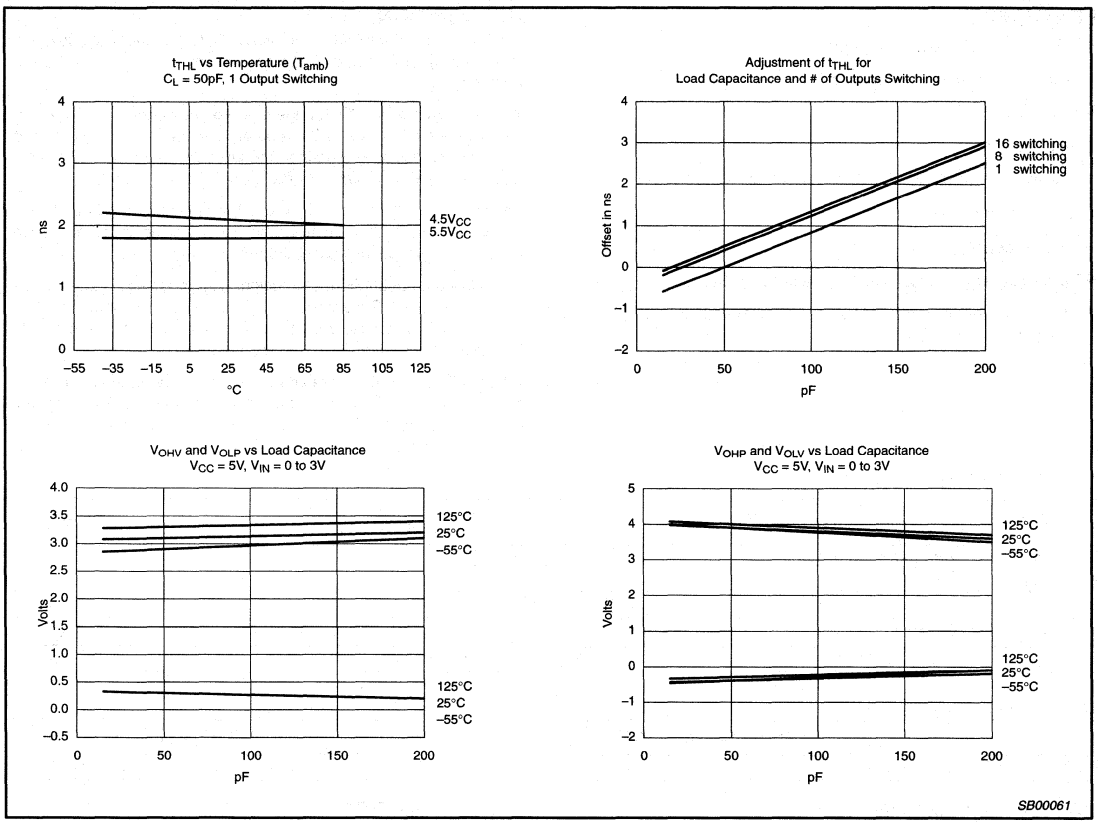
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching



SB00060


t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
–55°C
SB00061

16-bit D-type flip-flop; positive-edge trigger (3-State) MB2374

FEATURES

- Two 8-bit positive edge triggered registers
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State output buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2374 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2374 has two 8-bit, edge triggered registers, with each register coupled to eight 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-Low Output Enable ($n\overline{OE}$) controls all eight 3-State buffers for its register independent of the clock operation.

When $n\overline{OE}$ is Low, the stored data appears at the outputs for that register. When $n\overline{OE}$ is High, the outputs for that register are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

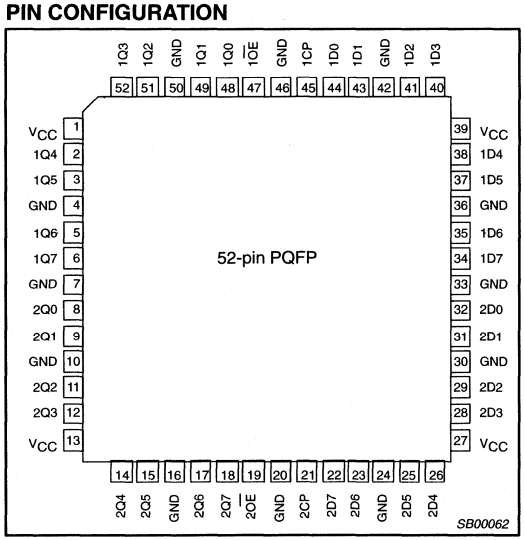
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	3.4 3.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2374 BB	MB2374 BB	SOT379-1

PIN CONFIGURATION

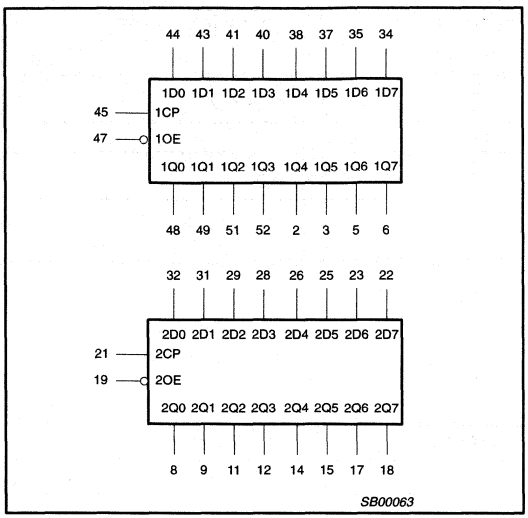


PIN DESCRIPTION

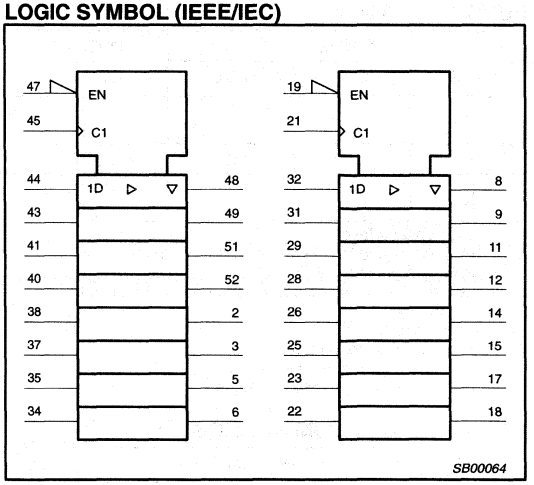
PIN NUMBER	SYMBOL	FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1D0 – 1D7 2D0 – 2D7	Data inputs
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
47, 19	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
45, 21	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

16-bit D-type flip-flop; positive-edge trigger (3-State) MB2374

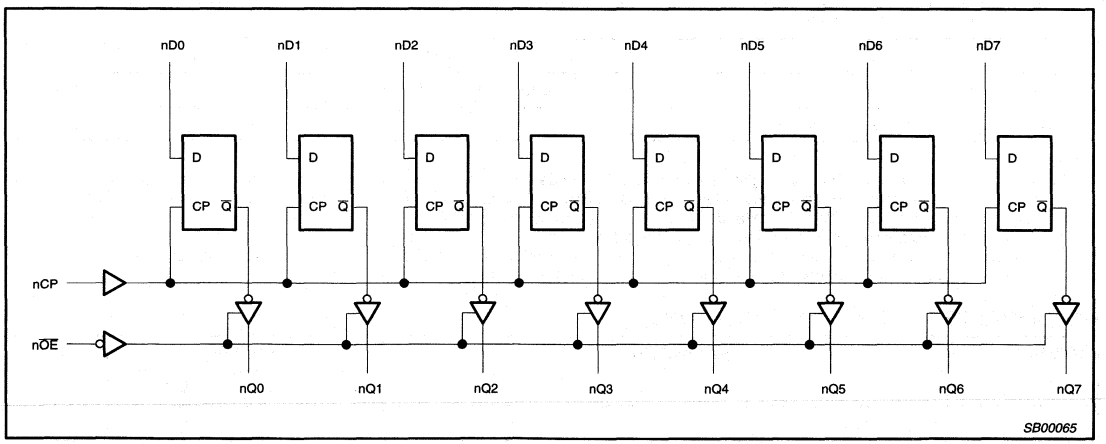
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx	REGISTER	nQ0 – nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}, V_{OE} = GND		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−70	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	180	260		180		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.8 1.8	3.4 3.6	4.6 4.6	1.8 1.8	5.1 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.2 2.1	3.0 4.0	4.1 5.5	1.2 2.1	4.8 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.2 1.8	3.4 3.6	4.6 5.0	1.2 1.8	5.1 5.5	ns

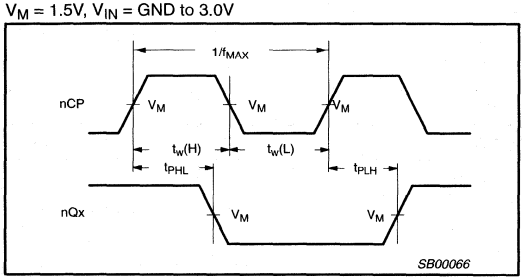
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

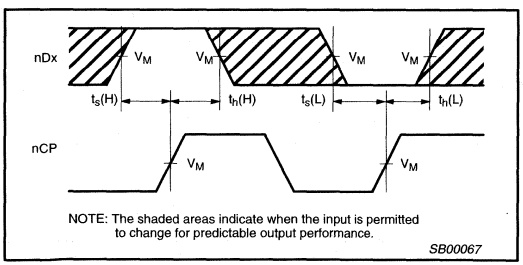
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nCP	2	1.0 1.0	0.3 0.1	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	2	1.0 1.0	–0.1 –0.3	1.0 1.0	ns
$t_w(H)$ $t_w(L)$	nCP pulse width High or Low	1	2.8 2.8	1.2 1.5	2.8 2.8	ns

AC WAVEFORMS

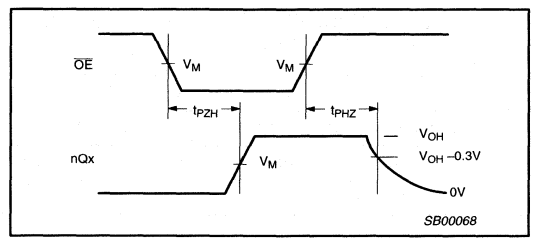
V_M = 1.5V, V_{IN} = GND to 3.0V



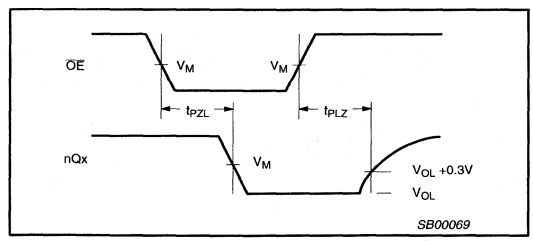
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

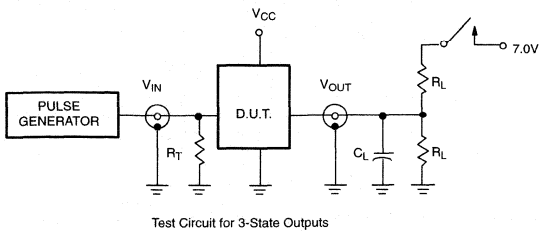


Waveform 3. 3–State Output Enable Time to High Level and Output Disable Time from High Level

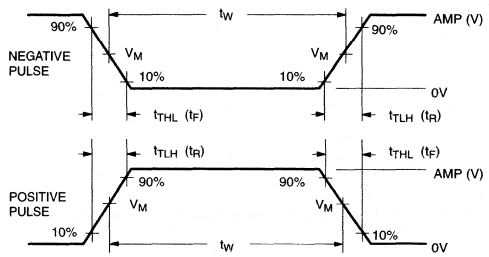


Waveform 4. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

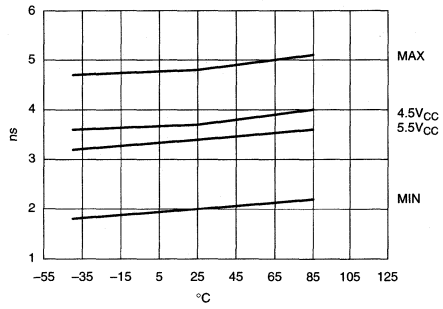
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

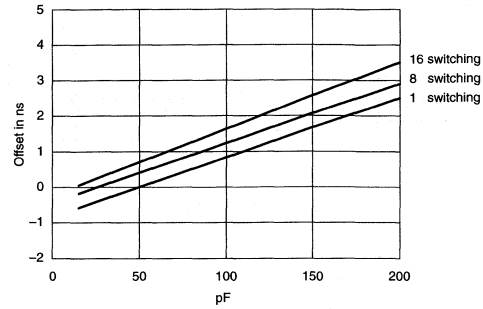
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

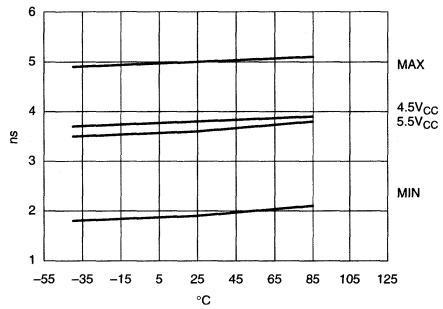
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCP to nQx



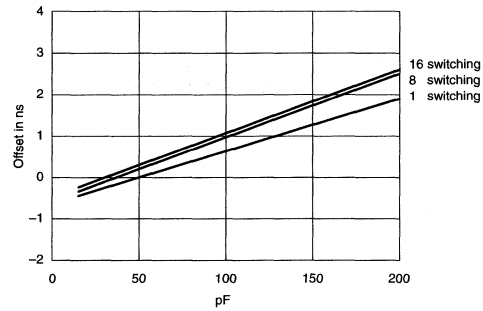
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nCP to nQx



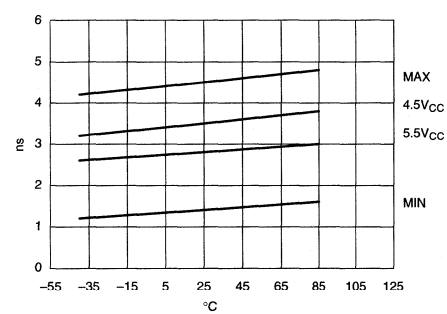
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCP to nQx



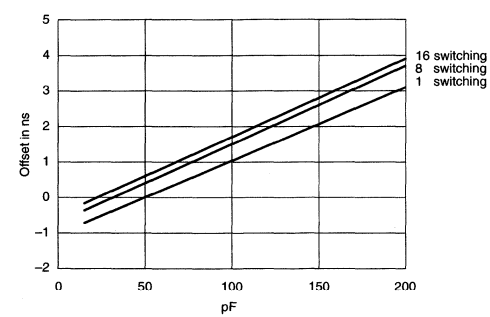
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nCP to nQx



t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx

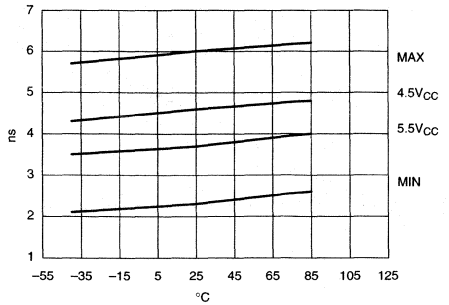


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx

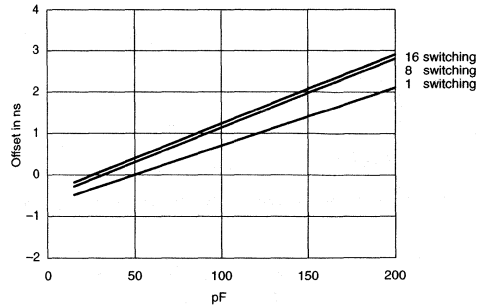


SB00070

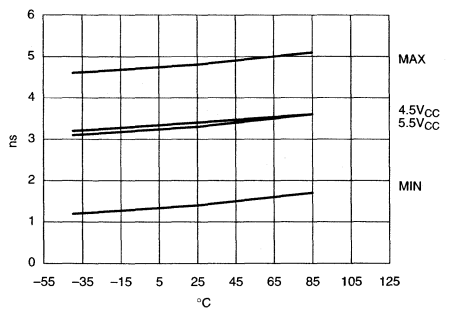
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



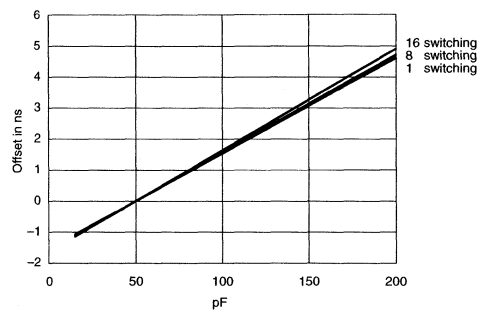
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



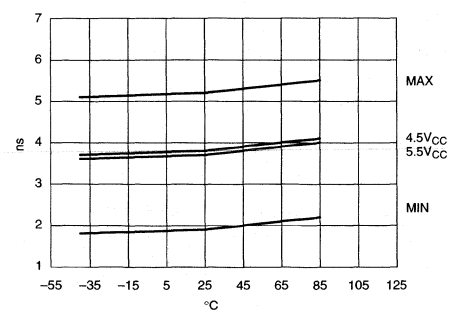
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



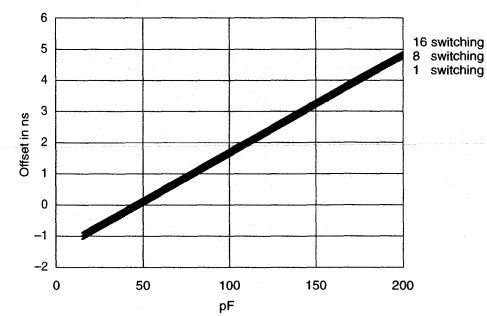
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



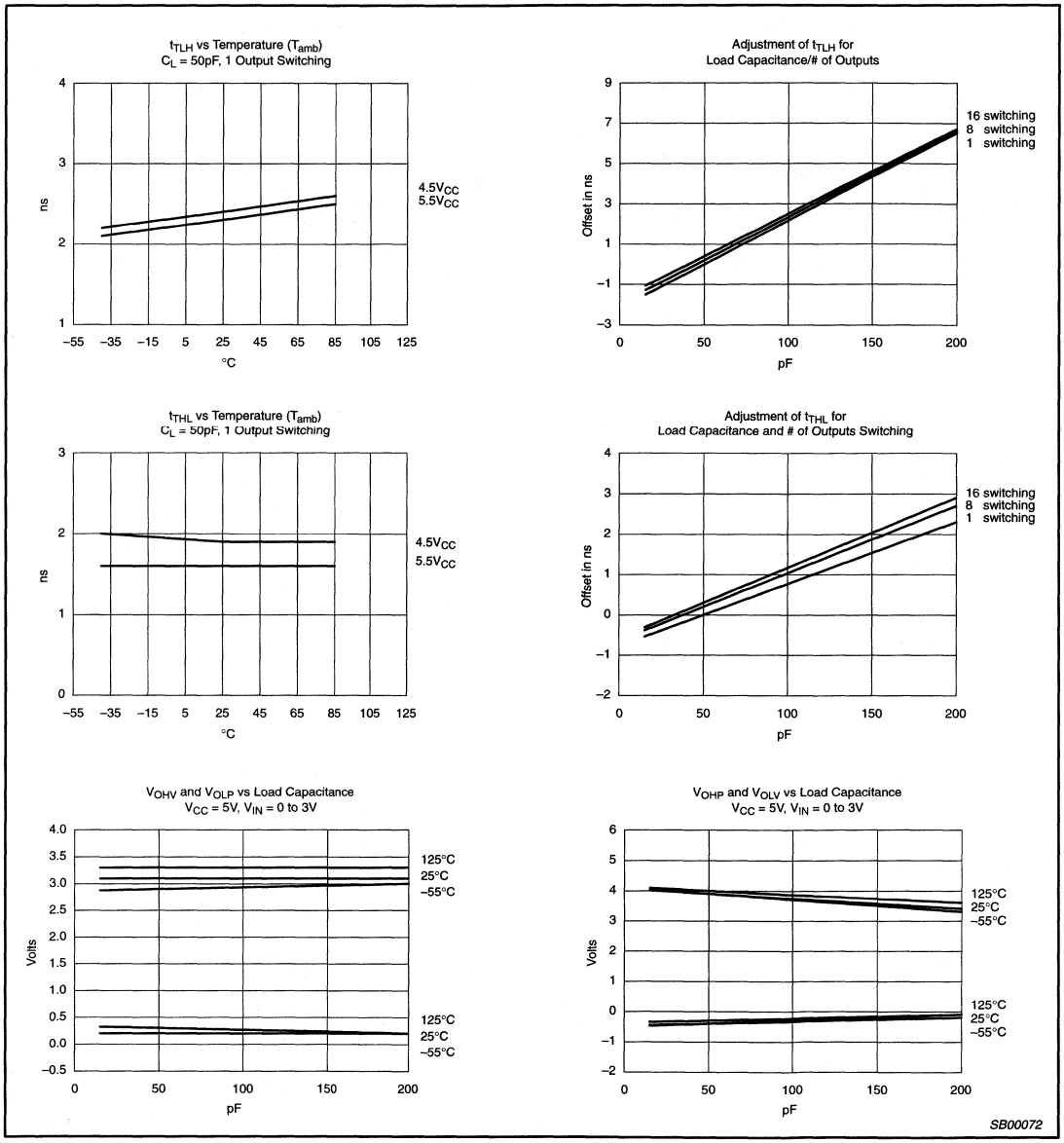
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



SB00071


tTLH vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
ns
°C
4.5VCC
5.5VCC
Adjustment of tTLH for
Load Capacitance/# of Outputs
Offset in ns
pF
16 switching
8 switching
1 switching
tTHL vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
ns
°C
4.5VCC
5.5VCC
Adjustment of tTHL for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
VOHV and VOLP vs Load Capacitance
VCC = 5V, VIN = 0 to 3V
Volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
VOHP and VOLV vs Load Capacitance
VCC = 5V, VIN = 0 to 3V
Volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
SB00072

16-bit D-type flip-flop with enable | MB2377

FEATURES

- Ideal for addressable register applications
- Two 8-bit positive edge-triggered registers
- Two Enable inputs for address and data synchronization applications
- Power-up reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The MB2377 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2377 has two 8-bit, edge triggered registers, with individual D inputs and Q outputs. The common buffered clock (1CP or 2CP) input will load a set of eight flip-flops simultaneously when the corresponding Enable ($1\overline{E}$ or $2\overline{E}$) input is Low.

The registers are fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The $n\overline{E}$ inputs must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

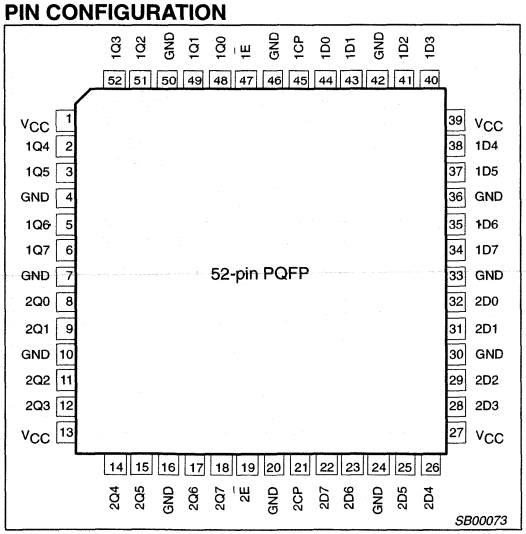
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	3.8 3.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52-pin plastic Quad Flat Pack	–40°C to +85°C	MB2377 BB	MB2377 BB	SOT379-1

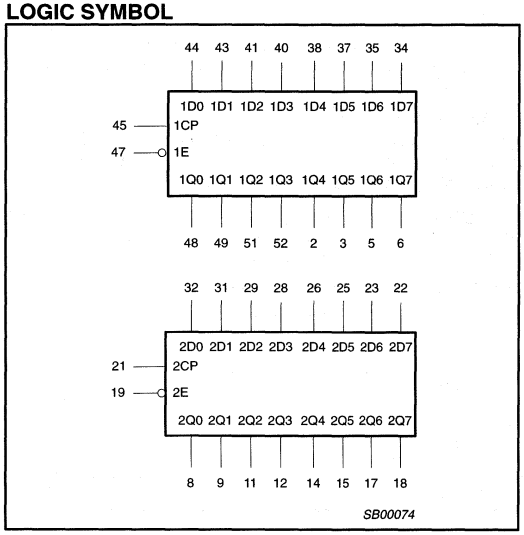
PIN CONFIGURATION



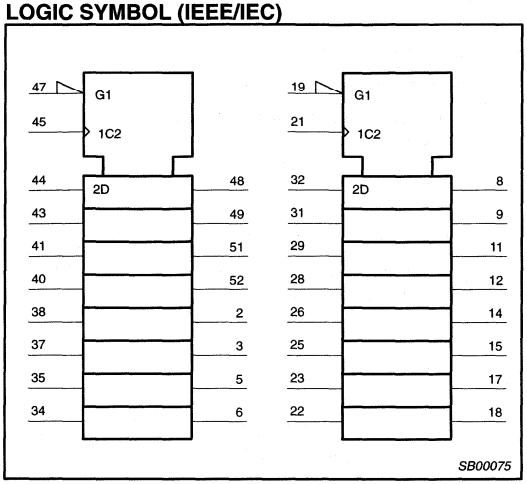
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1D0 – 1D7 2D0 – 2D7	Data inputs
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
47, 19	$1\overline{E}$, $2\overline{E}$	Enable inputs (active-Low)
45, 21	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

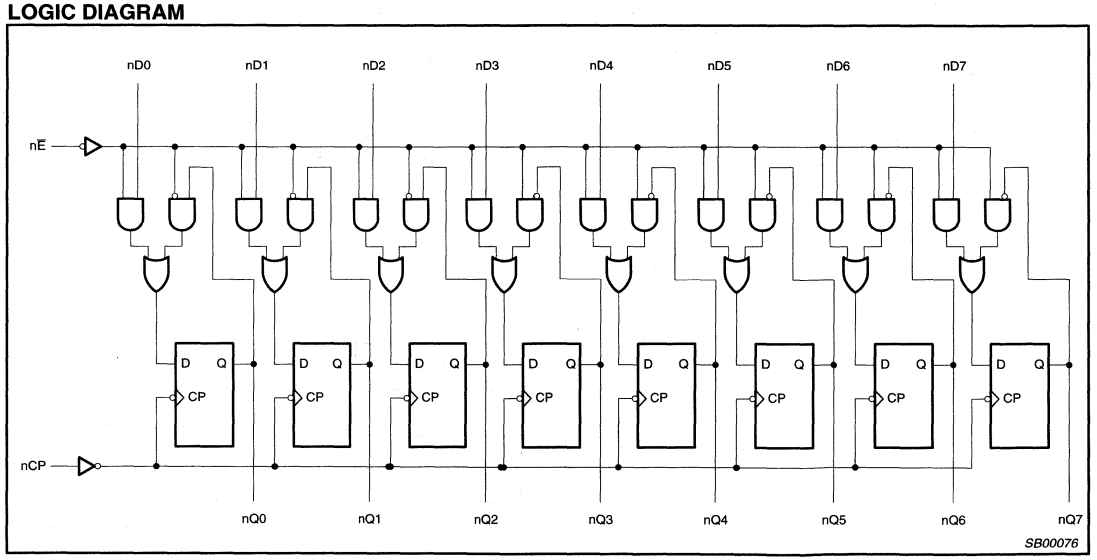
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$n\overline{E}$	nCP	nDx	nQx	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		48	60		60	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	180	230		180		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.8 1.8	3.8 3.8	5.3 5.3	1.8 1.8	5.8 5.8	ns

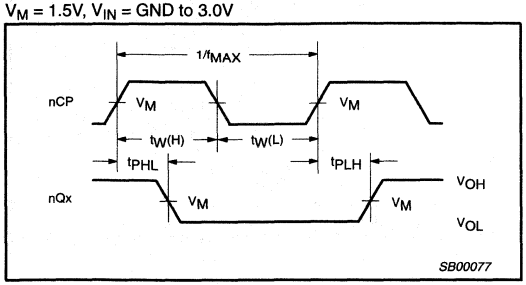
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

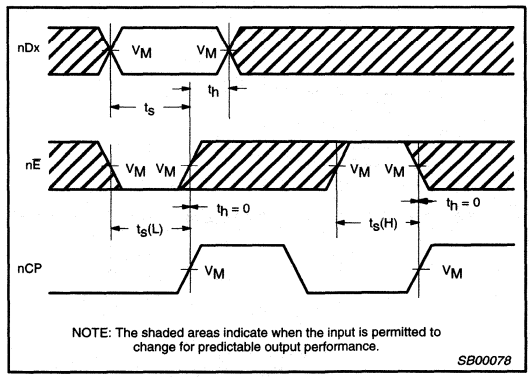
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C V_{CC} = +5.0V		T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	2	1.0 1.0	0.4 0.3	1.0 1.0	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	2	0.5 0.5	–0.3 –0.4	0.5 0.5	ns
t_s(H) t_s(L)	Setup time, High or Low $n\overline{E}$ to nCP	2	2.5 3.0	1.0 1.5	2.5 3.0	ns
t_h(H) t_h(L)	Hold time, High or Low $n\overline{E}$ to nCP	2	0.0 0.0	–1.5 –0.8	0.0 0.0	ns
t_w(H) t_w(L)	Clock Pulse width High or Low	1	2.8 2.8	1.2 1.5	2.8 2.8	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

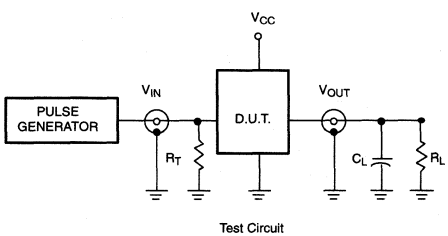


Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency

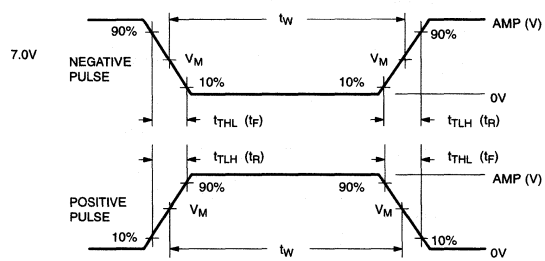


Waveform 2. Data and Enable Setup and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

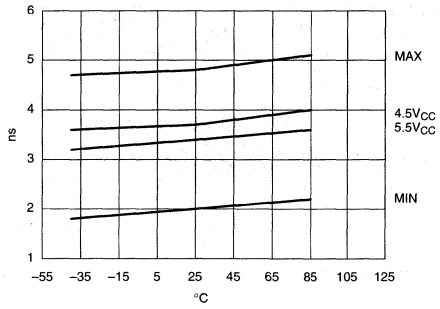
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

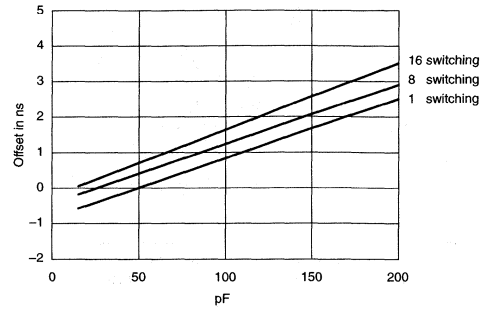
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00211

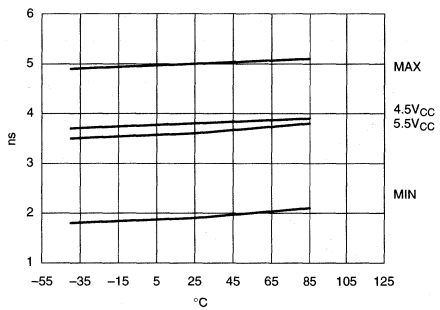
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCP to nQx



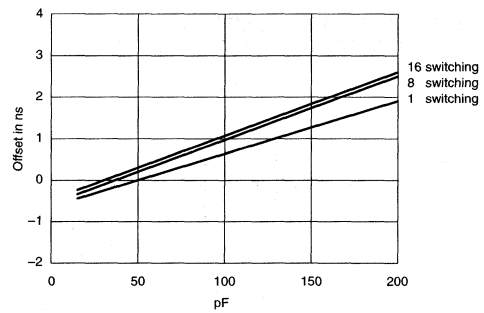
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nCP to nQx



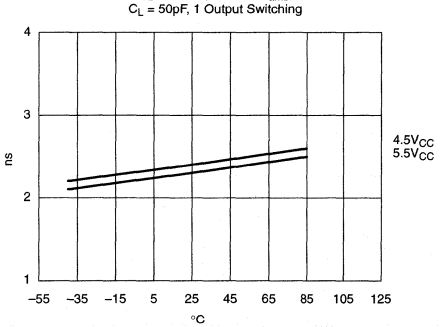
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCP to nQx



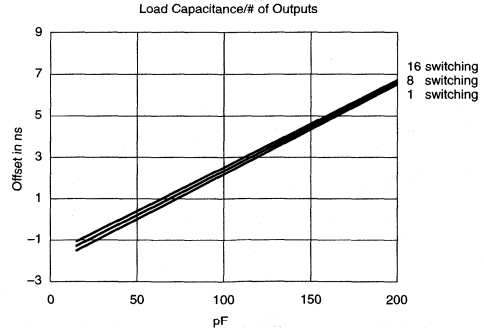
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nCP to nQx



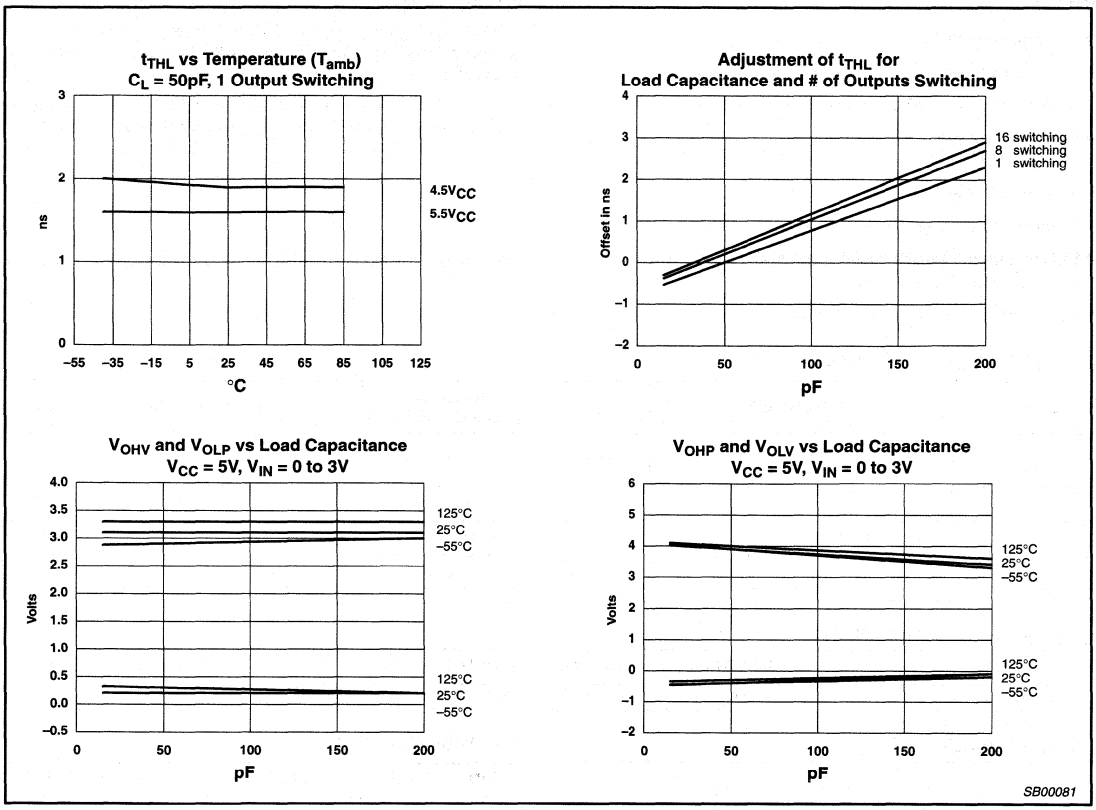
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{TLH} for
Load Capacitance/# of Outputs



SB00080


t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5VCC
5.5VCC
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
–55°C
SB00081

16-bit buffer/line drivers (3-State) MB2541

FEATURES

- Two 8-bit bus interfaces
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- Provides ideal interface and increases fan-out of MOS Microprocessors
- 3-State buffers sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Inputs are disabled during 3-State mode

DESCRIPTION

The MB2541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2541 has two 8-bit buffers that are ideal for driving bus lines. The outputs are all capable of sinking 64mA and sourcing 32mA.

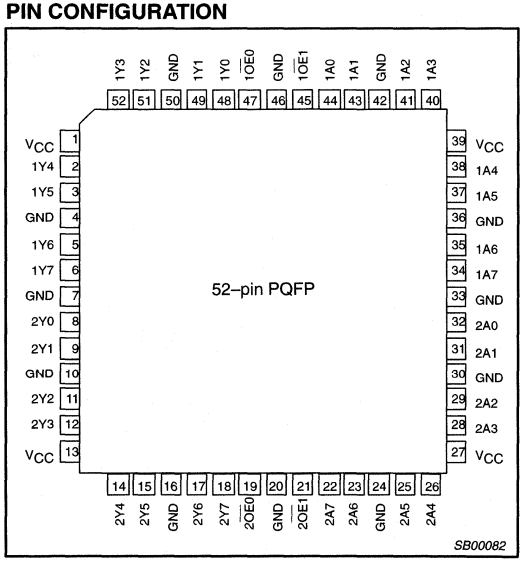
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nIx to nYx	C_L = 50pF; V_{CC} = 5V	3.0 3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	65	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2541 BB	MB2541 BB	SOT379-1

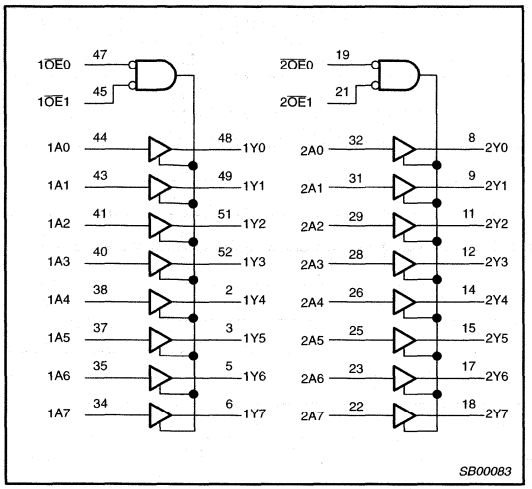
PIN CONFIGURATION



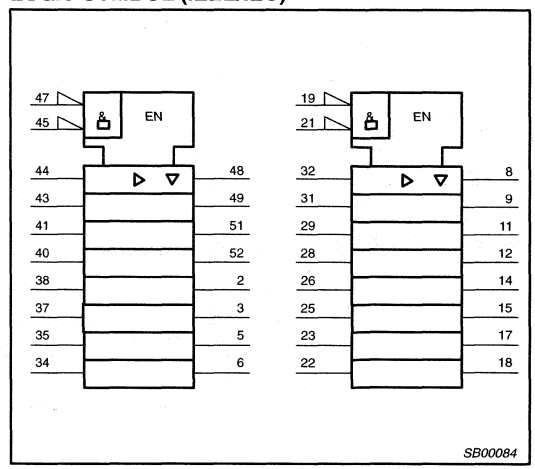
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1A0 – 1A7 2A0 – 2A7	Data inputs
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1Y0 – 1Y7, 2Y0 – 2Y7	Data outputs
47, 45, 19, 21	$1\overline{OE}0$, $1\overline{OE}1$, $2\overline{OE}0$, $2\overline{OE}1$	Output enables
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS			OUTPUTS
$n\overline{OE}0$	$n\overline{OE}1$	nIx	nYx
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		65	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		65	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

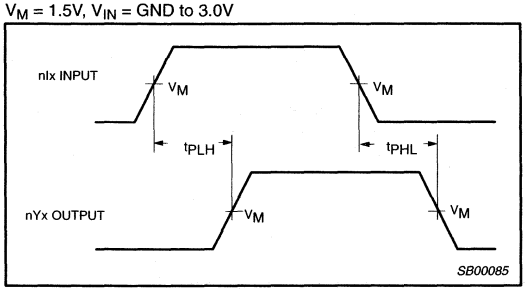
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

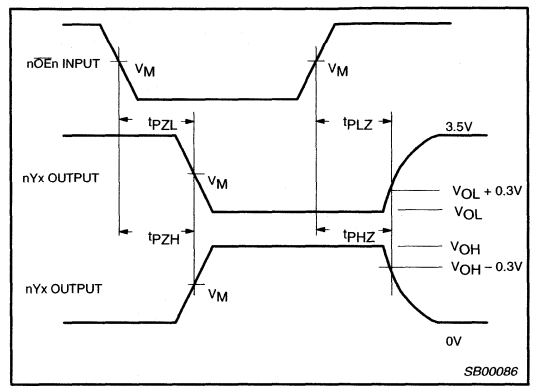
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nIx to nYx	1	1.2 1.2	3.0 3.1	4.5 4.5	1.2 1.2	5.1 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 2.1	3.6 4.7	5.2 6.1	1.3 2.1	5.8 7.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.8 1.7	4.3 4.0	6.2 5.4	1.8 1.7	6.8 5.9	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

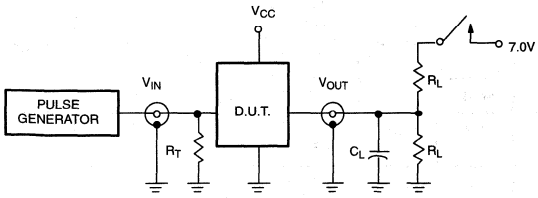


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

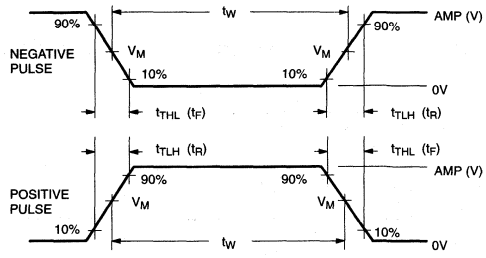


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

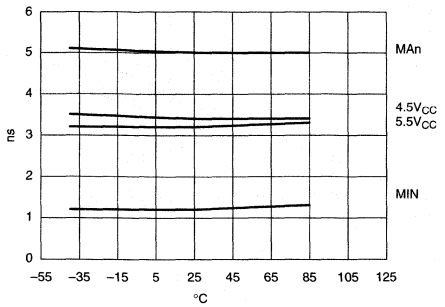
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

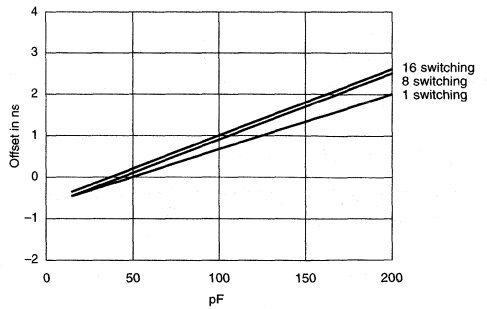
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

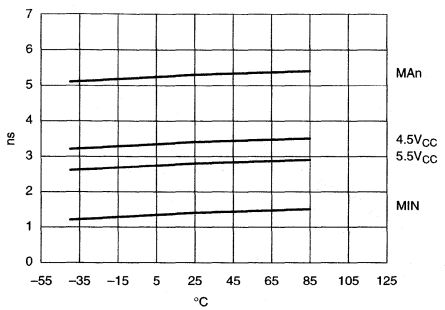
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nIx to nYx



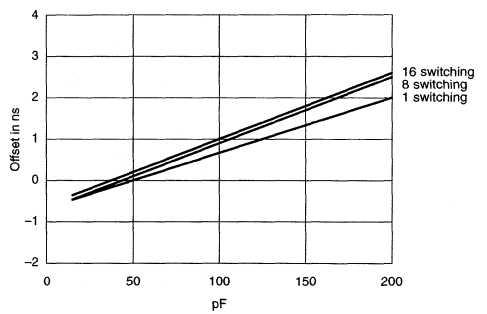
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nIx to nYx



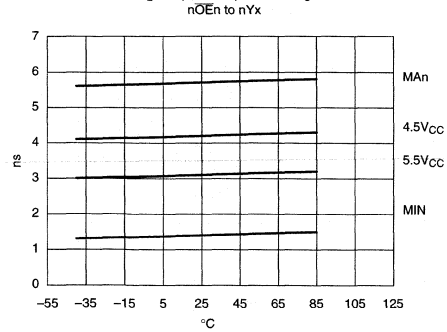
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nIx to nYx



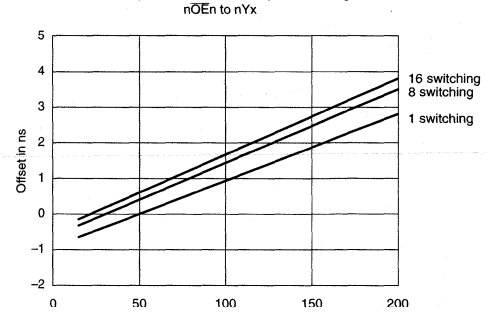
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nIx to nYx



t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$n to nYx

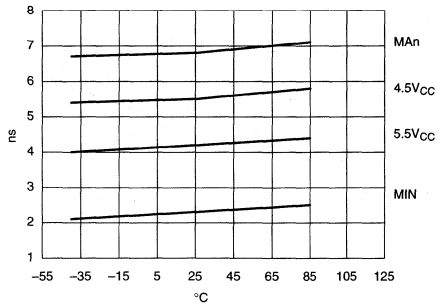


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$n to nYx

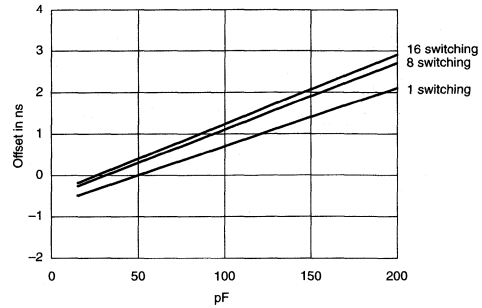


SB00087

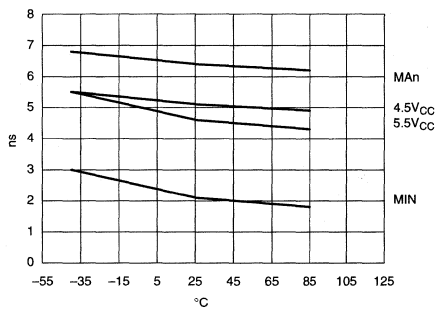
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}n$ to nYx



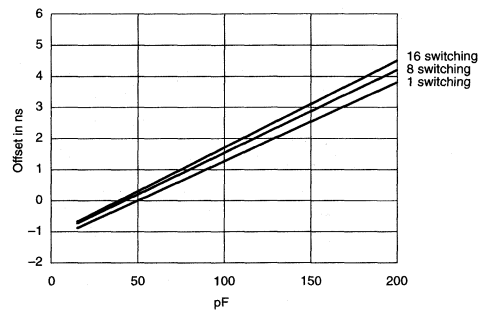
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}n$ to nYx



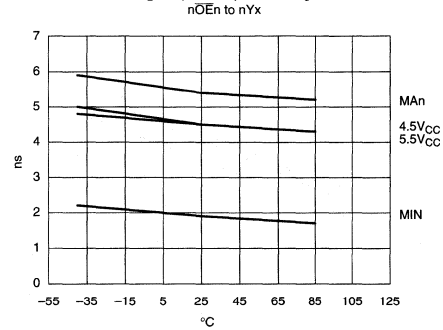
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}n$ to nYx



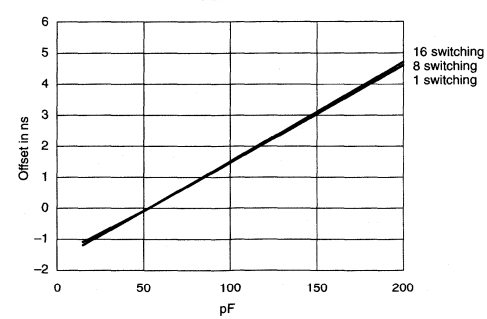
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}n$ to nYx



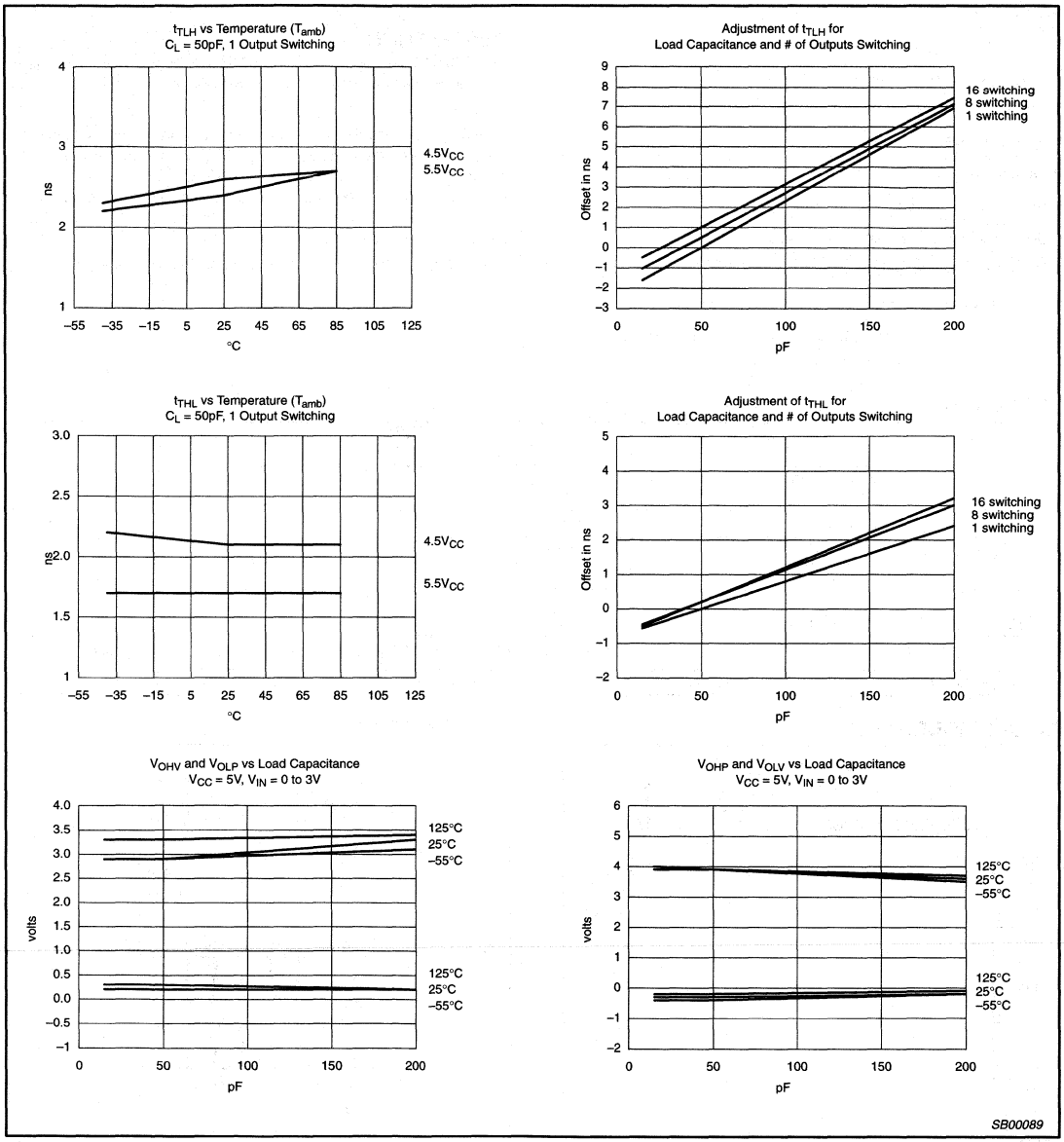
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}n$ to nYx



Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}n$ to nYx



SB00088


tTLH vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
ns
°C
4.5VCC
5.5VCC
Adjustment of tTLH for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
tTHL vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
ns
°C
4.5VCC
5.5VCC
Adjustment of tTHL for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
VOHV and VOLP vs Load Capacitance
VCC = 5V, VIN = 0 to 3V
volts
pF
125°C
25°C
−55°C
125°C
25°C
−55°C
VOHP and VOLV vs Load Capacitance
VCC = 5V, VIN = 0 to 3V
volts
pF
125°C
25°C
−55°C
125°C
25°C
−55°C
SB00089

16-bit latched transceiver with dual enable (3-State) MB2543

FEATURES

- Two 8-bit octal transceivers with D-type latch
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2543 16-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($n\overline{LEAB}$, $n\overline{LEBA}$) and Output Enable ($n\overline{OEAB}$, $n\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

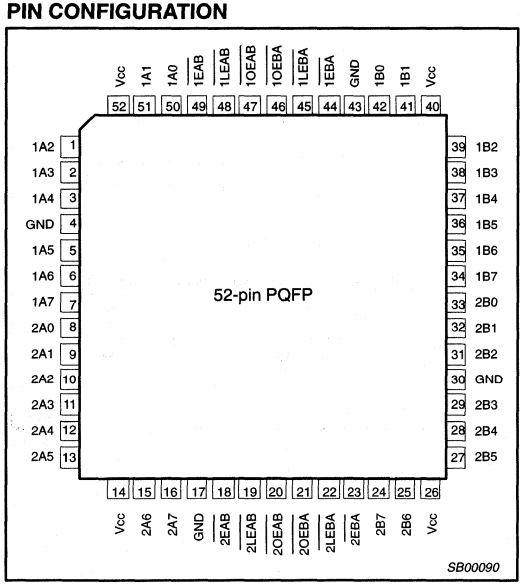
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	3.2 3.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

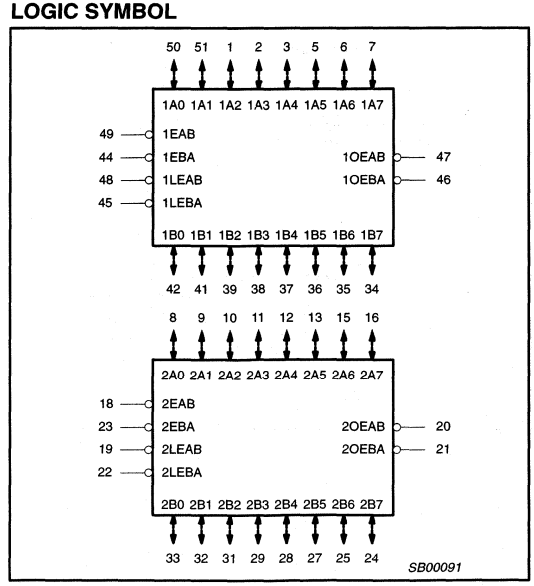
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2543 BB	MB2543 BB	SOT379-1

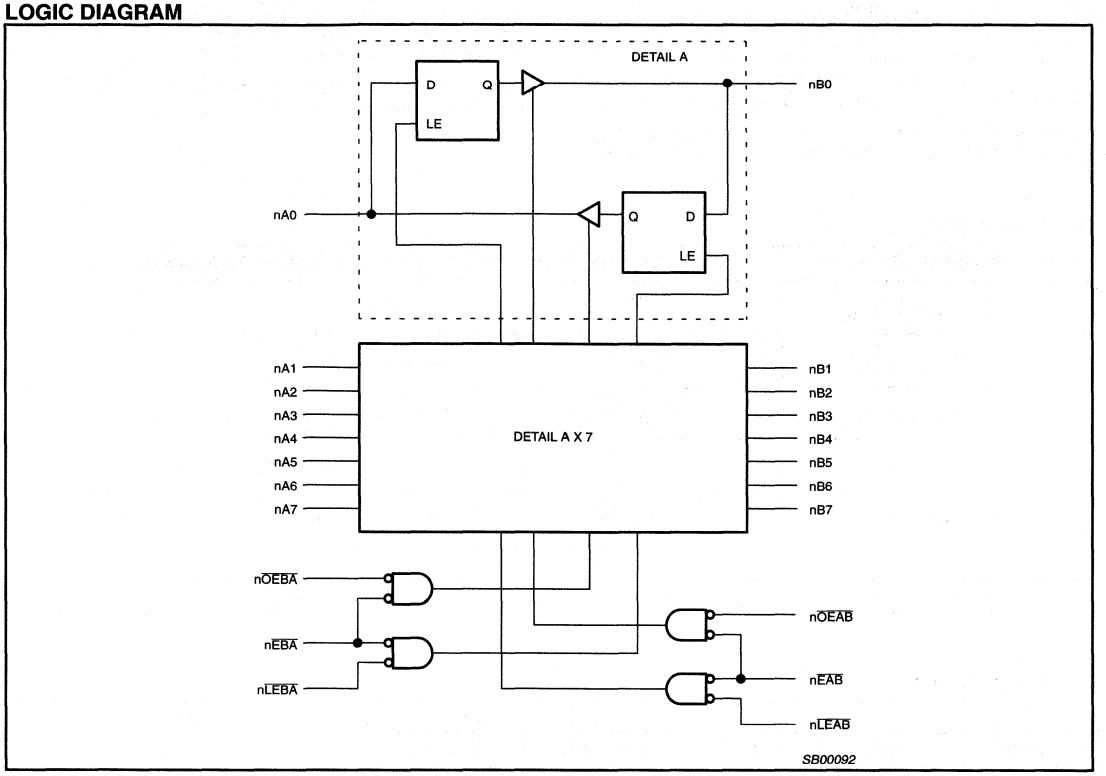
PIN CONFIGURATION



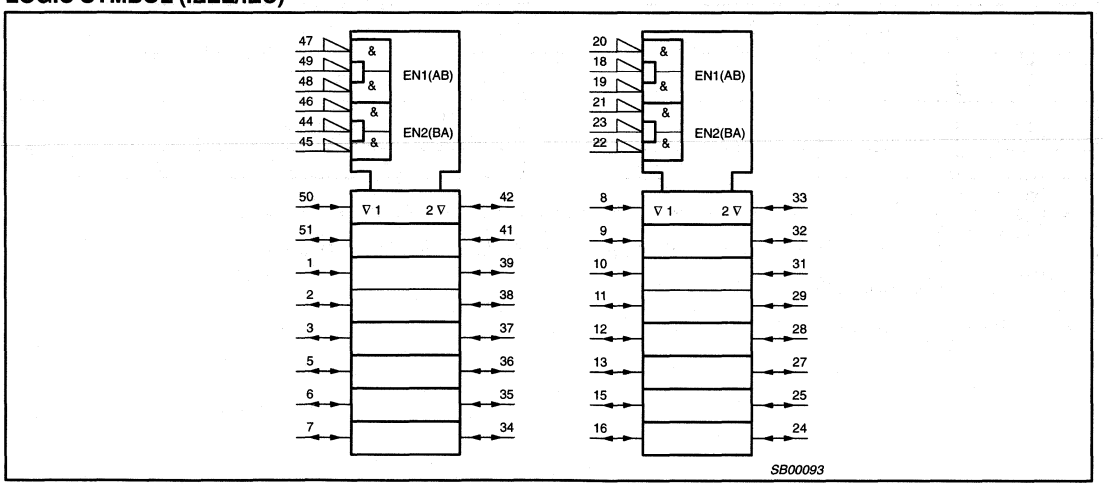
LOGIC SYMBOL



LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DESCRIPTION

The MB2543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are Low the A-to-B path is transparent.

A subsequent Low-to-High transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $n\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs
42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs
47, 46, 20, 21	$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	A to B / B to A Output Enable inputs (active-Low)
49, 44, 18, 23	$1\overline{EAB}$, $1\overline{EBA}$, $2\overline{EAB}$, $2\overline{EBA}$	A to B / B to A Enable inputs (active-Low)
48, 45, 19, 22	$1\overline{LEAB}$, $1\overline{LEBA}$, $2\overline{LEAB}$, $2\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-Low)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$n\overline{OEXX}$	$n\overline{EXX}$	$n\overline{LEXX}$	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]		V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		38	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, nBx to nAx	2	1.5 1.6	3.2 3.3	4.6 4.6	1.5 1.6	5.2 5.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to nAx, $\overline{LEAB}$ to nBx	1, 2	1.9 2.1	3.9 4.1	5.3 5.5	1.9 2.1	6.1 6.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to nAx, $\overline{OEAB}$ to nBx	4 5	1.6 2.3	3.6 4.5	5.0 5.9	1.6 2.3	5.8 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to nAx, $\overline{OEAB}$ to nBx	4 5	1.0 1.4	3.6 3.2	5.0 4.6	1.0 1.4	5.7 5.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to nAx, $\overline{EAB}$ to nBx	4 5	1.6 2.3	3.6 4.5	5.0 5.9	1.6 2.3	5.8 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to nAx, $\overline{EAB}$ to nBx	4 5	1.0 1.4	3.6 3.2	5.0 4.6	1.0 1.4	5.7 5.2	ns

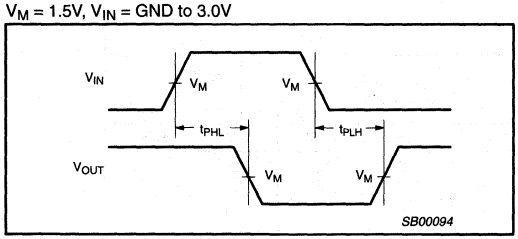
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

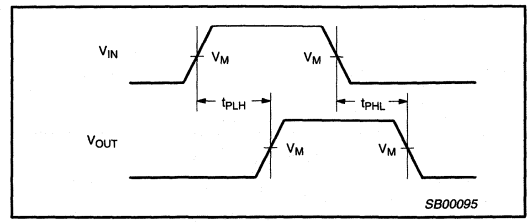
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time nAx to $\overline{LEAB}$, nBx to $\overline{LEBA}$	3	1.0 0.5	0.4 –0.1	1.0 0.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to $\overline{LEAB}$, nBx to $\overline{LEBA}$	3	1.0 0.5	0.2 –0.3	1.0 0.5	ns
$t_s(H)$ $t_s(L)$	Setup time nAx to $\overline{EAB}$, nBx to $\overline{EBA}$	3	1.0 0.5	0.2 –0.3	1.0 0.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to $\overline{EAB}$, nBx to $\overline{EBA}$	3	1.0 0.5	0.3 –0.2	1.0 0.5	ns
$t_w(L)$	Latch enable pulse width, Low	3	4.0	3.1	4.0	ns

AC WAVEFORMS

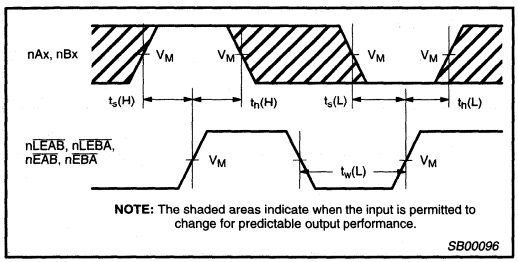
V_M = 1.5V, V_{IN} = GND to 3.0V



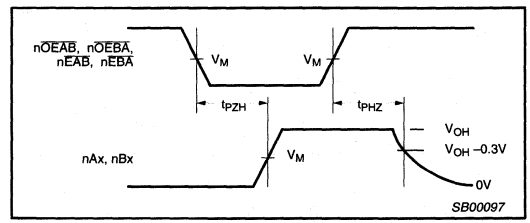
Waveform 1. Propagation Delay For Inverting Output



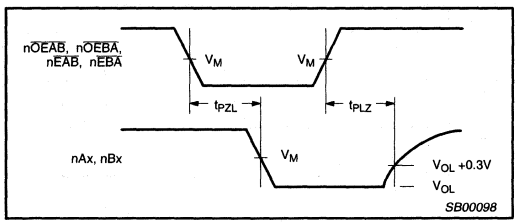
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width

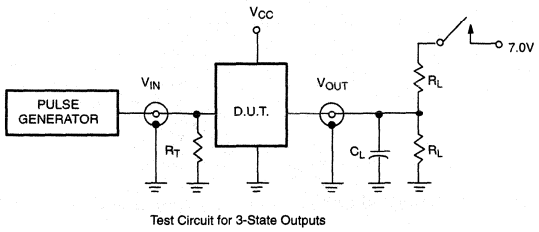


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

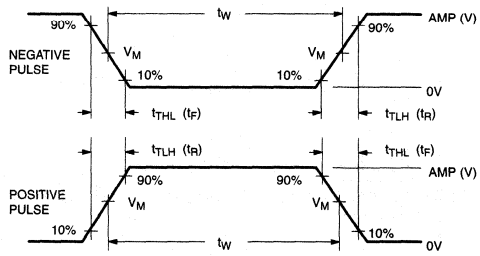


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

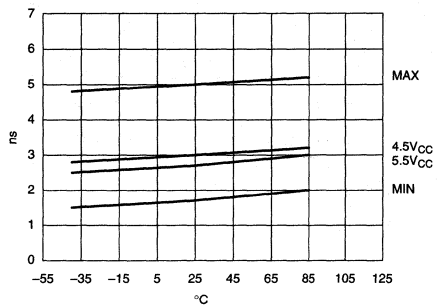
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

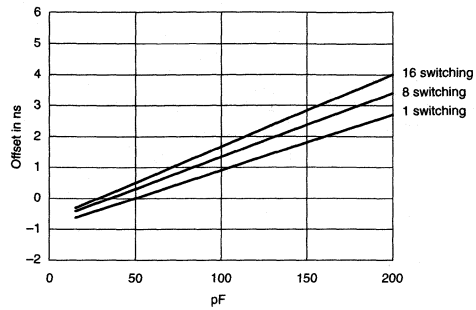
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

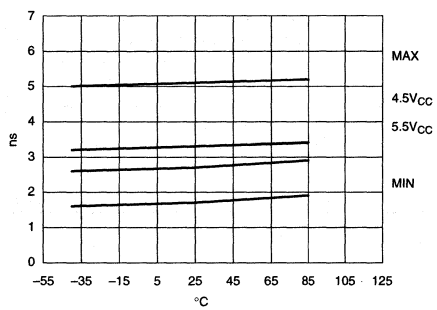
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx or nBx to nAx



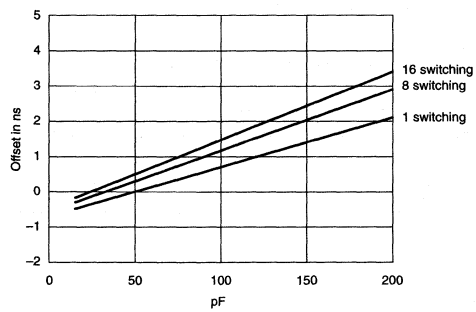
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nAx to nBx or nBx to nAx



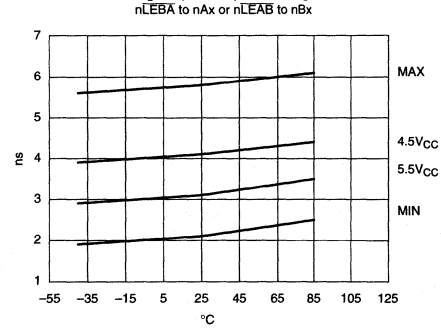
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx or nBx to nAx



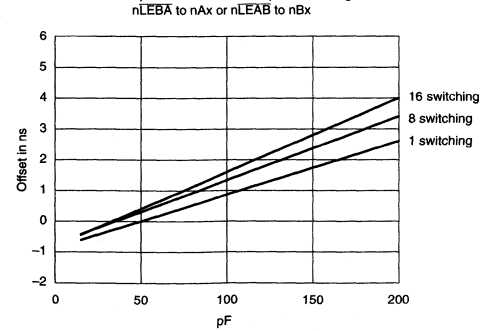
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nAx to nBx or nBx to nAx



t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{LEBA}$ to nAx or n$\overline{LEAB}$ to nBx

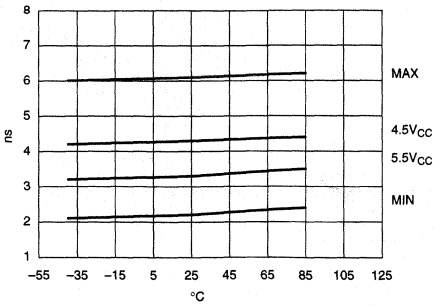


Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
n$\overline{LEBA}$ to nAx or n$\overline{LEAB}$ to nBx

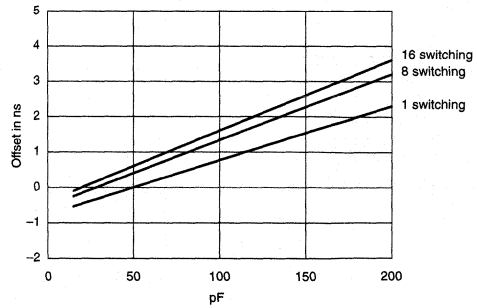


SB00099

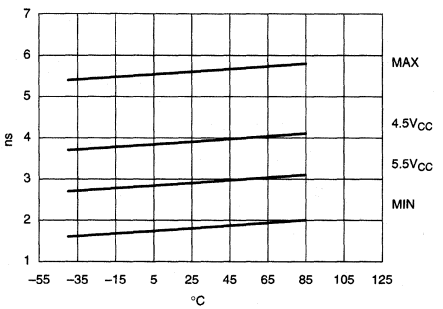
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{LEBA}$ to nAx or n$\overline{LEAB}$ to nBx



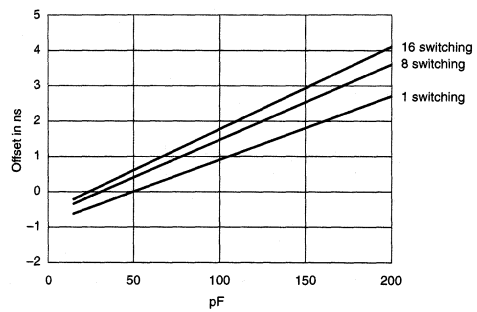
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
n$\overline{LEBA}$ to nAx or n$\overline{LEAB}$ to nBx



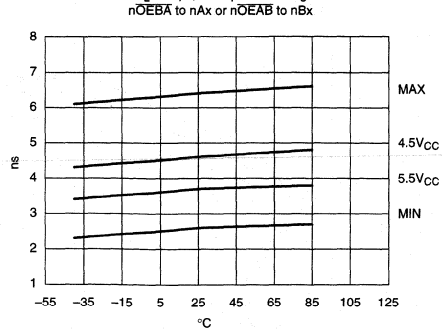
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OEBA}$ to nAx or n$\overline{OEAB}$ to nBx



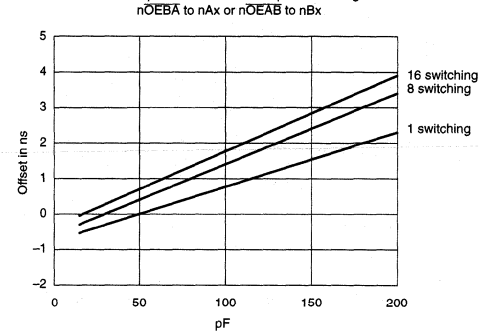
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OEBA}$ to nAx or n$\overline{OEAB}$ to nBx



t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OEBA}$ to nAx or n$\overline{OEAB}$ to nBx

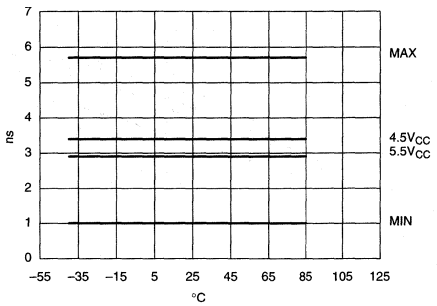


Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
n$\overline{OEBA}$ to nAx or n$\overline{OEAB}$ to nBx

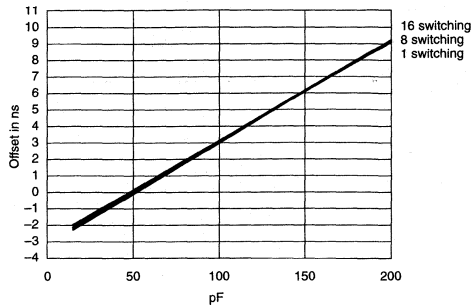


SB00100

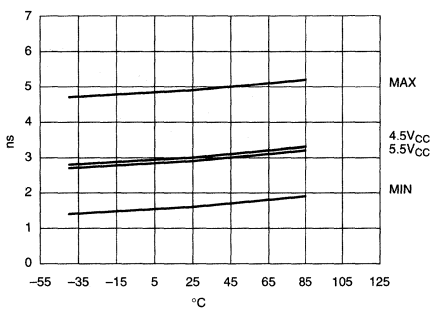
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OEBA}$ to nAx or $n\overline{OEAB}$ to nBx



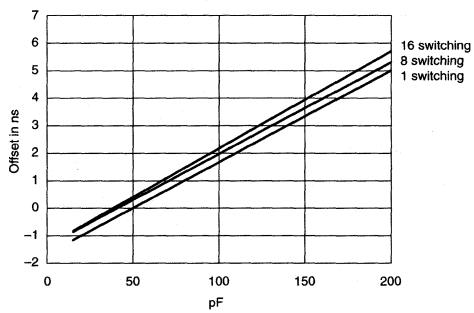
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OEBA}$ to nAx or $n\overline{OEAB}$ to nBx



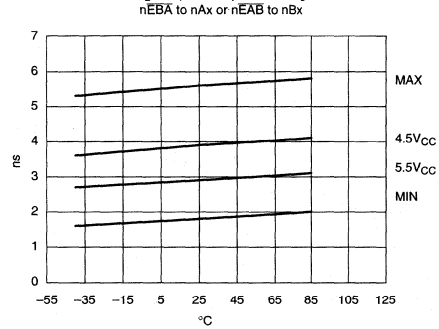
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OEBA}$ to nAx or $n\overline{OEAB}$ to nBx



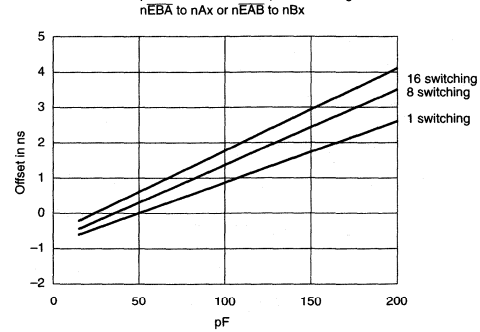
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OEBA}$ to nAx or $n\overline{OEAB}$ to nBx



t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{EBA}$ to nAx or $n\overline{EAB}$ to nBx

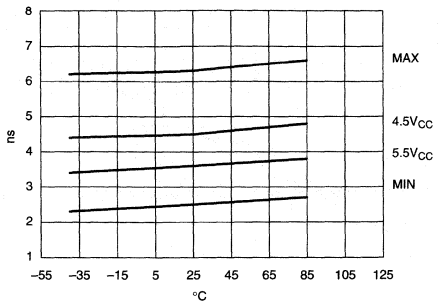


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$n\overline{EBA}$ to nAx or $n\overline{EAB}$ to nBx

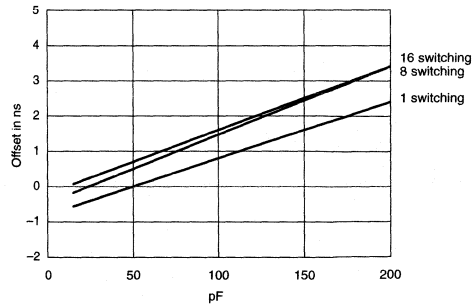


SB00101

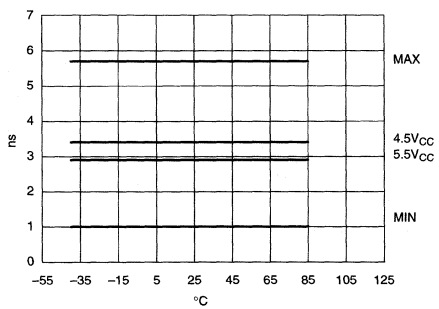
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{EBA}$ to nAx or $n\overline{EAB}$ to nBx



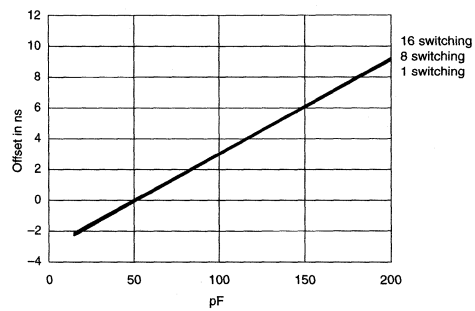
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$n\overline{EBA}$ to nAx or $n\overline{EAB}$ to nBx



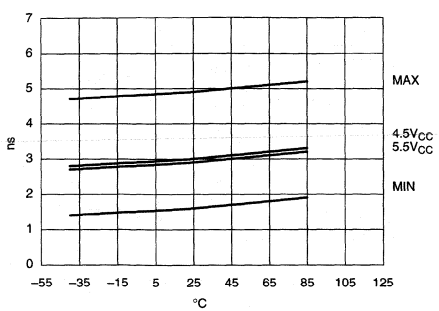
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{EBA}$ to nAx or $n\overline{EAB}$ to nBx



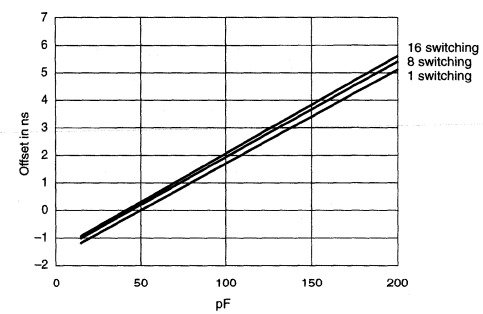
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{EBA}$ to nAx or $n\overline{EAB}$ to nBx



t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{EBA}$ to nAx or $n\overline{EAB}$ to nBx

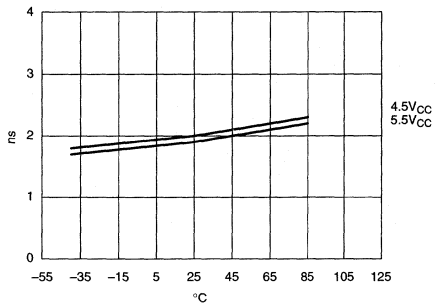


Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{EBA}$ to nAx or $n\overline{EAB}$ to nBx

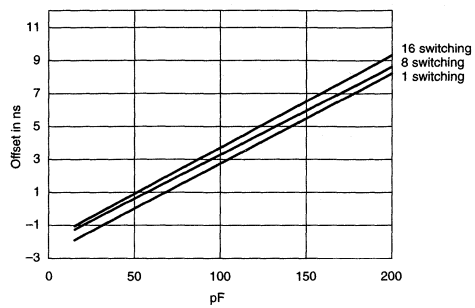


SB00102

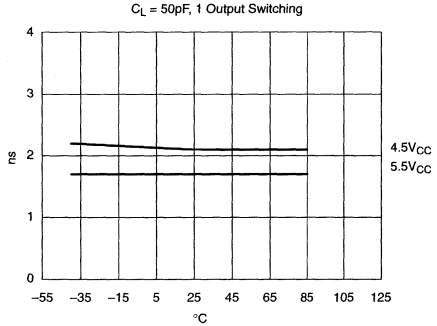
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



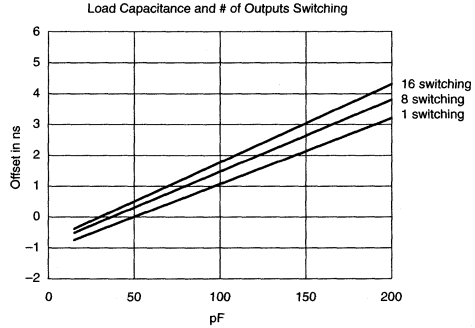
Adjustment of t_{TLH} for
Load Capacitance/# of Outputs



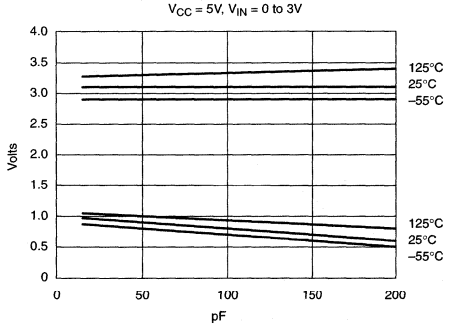
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



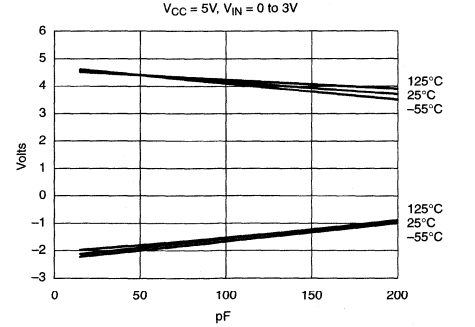
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V



SB00103

16-bit transceiver with dual enable, non-inverting (3-State)

MB2623

FEATURES

- Two 8-bit bidirectional bus interfaces
- 3-State buffers
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Inputs are disabled during 3-State mode

DESCRIPTION

The MB2623 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2623 is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The MB2623 is designed for asynchronous two-way communication between data buses.

The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($n\overline{OEBA}$ and nOEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

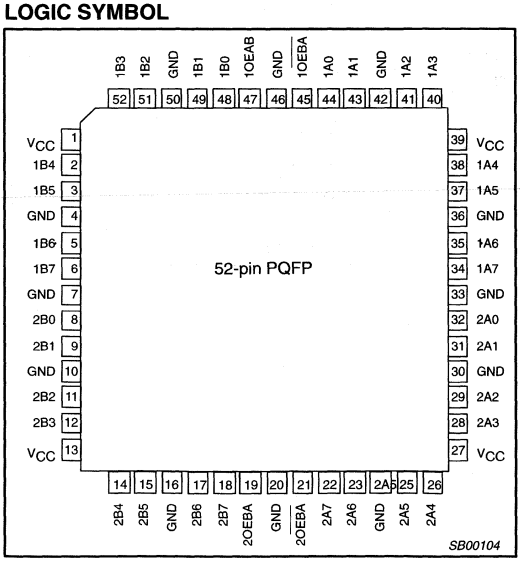
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, or nBx to nAx	C_L = 50pF; V_{CC} = 5V	3.2 3.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2623 BB	MB2623 BB	SOT379-1

LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1A0 – 1A7 2A0 – 2A7	Data inputs/outputs (A side)
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1B0 – 1B7 2B0 – 2B7	Data inputs/outputs (B side)
47, 19	1OEAB, 2OEAB	Output enable inputs (active-High)
45, 21	$1\overline{OEBA}$, $2\overline{OEBA}$	Output enable inputs (active-Low)
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

16-bit transceiver with dual enable, non-inverting (3-State)

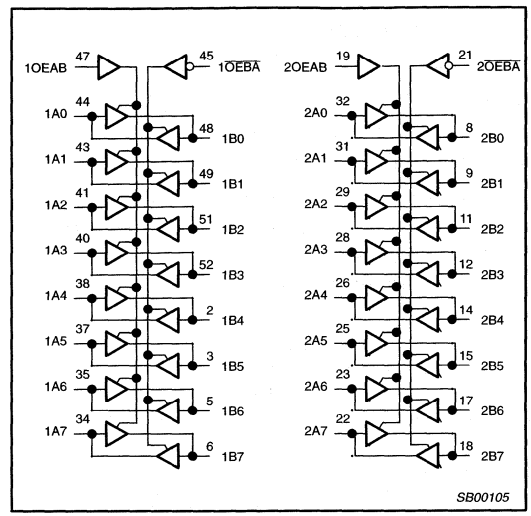
MB2623

FUNCTION TABLE

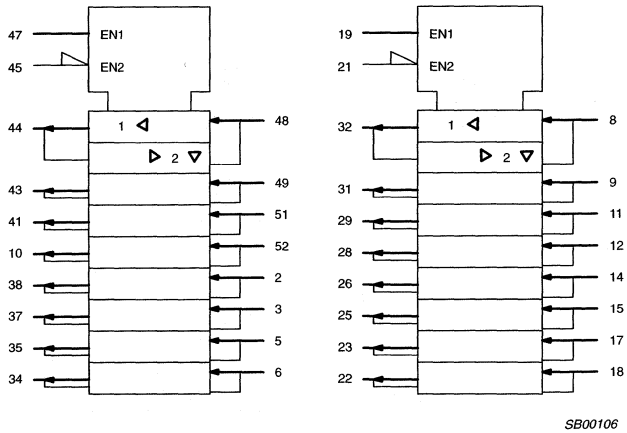
INPUTS		OUTPUTS	
$\overline{nOEBA}$	nOEAB	nAx	nBx
L	L	A = B	Inputs
H	H	Inputs	B = A
H	L	Z	Z
L	H	A = B	B = A

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±50		±50	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current		V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}; V_{OE} = GND		±5.0	±100		±100	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	100		100	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		48	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		50	100		100	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

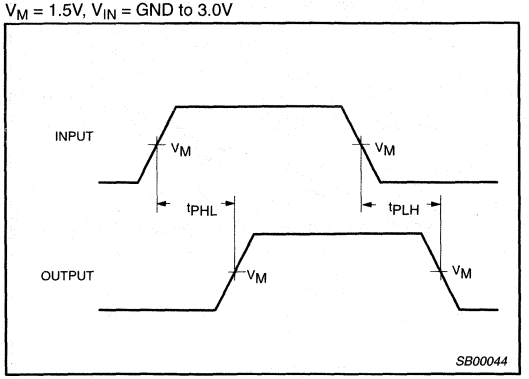
AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

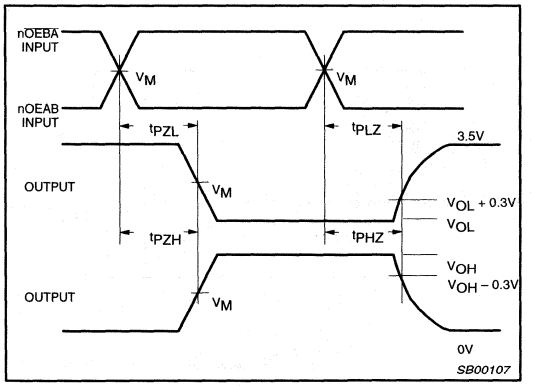
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.2 1.2	3.2 3.1	4.5 4.5	1.2 1.2	5.1 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.7	4.8 5.4	6.5 6.8	1.5 1.7	7.2 7.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.4	4.7 4.2	6.5 5.8	1.5 1.4	7.2 6.5	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

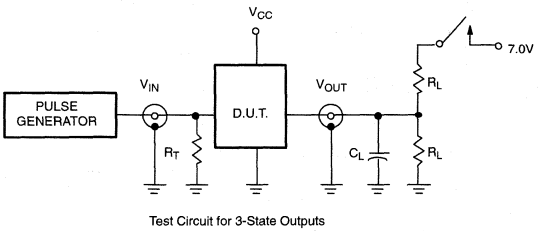


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

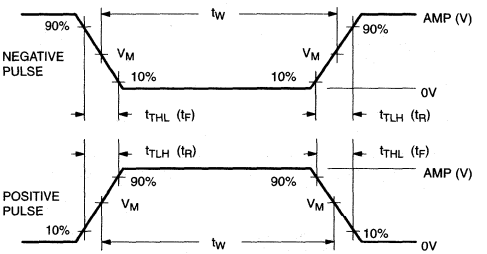


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

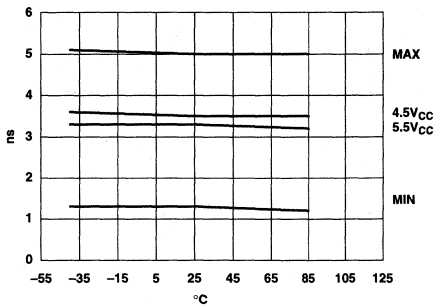
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

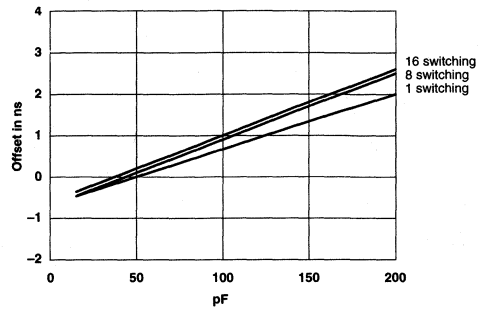
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

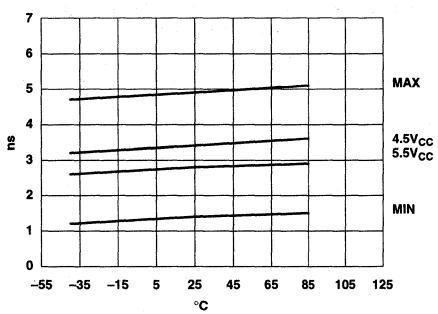
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx



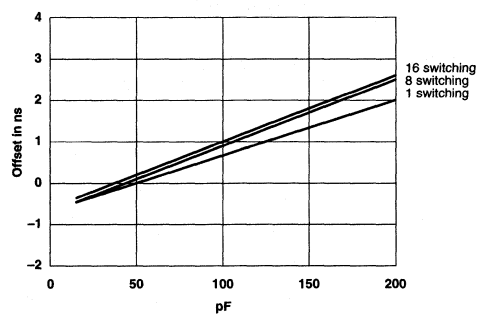
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nAx to nBx



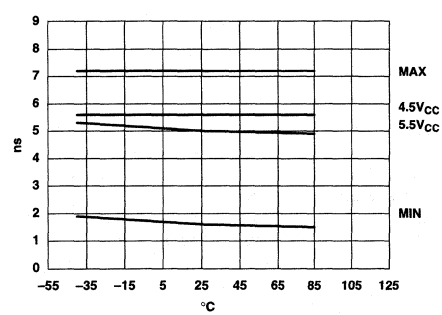
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx



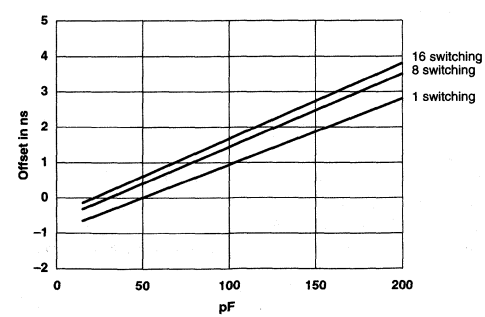
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nAx to nBx



t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nOEAB to nBx or $n\overline{OEBA}$ to nAx

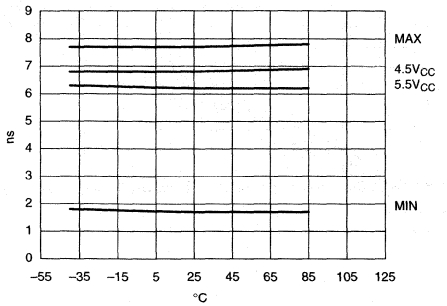


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
nOEAB to nBx or $n\overline{OEBA}$ to nAx

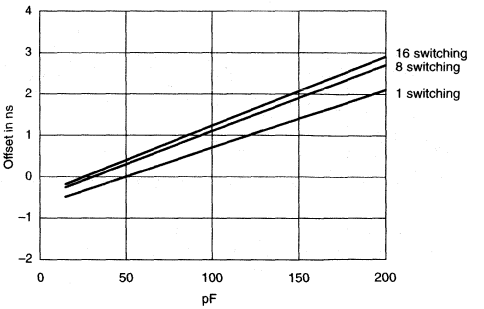


SB00108

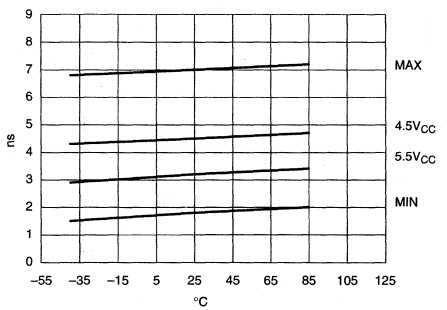
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nOEAB to nBx or $n\overline{OEBA}$ to nAx



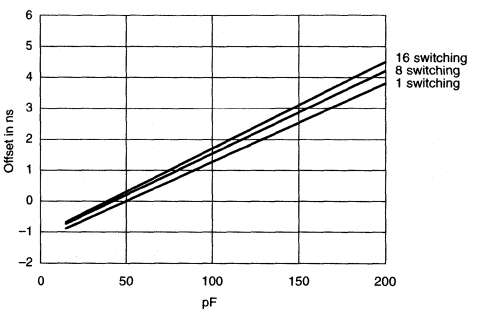
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
nOEAB to nBx or $n\overline{OEBA}$ to nAx



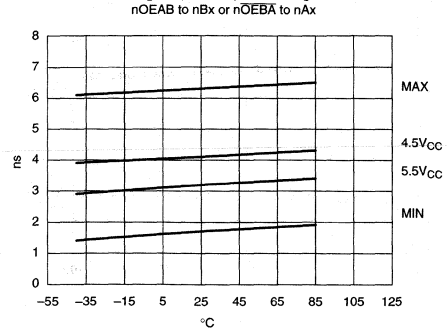
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nOEAB to nBx or $n\overline{OEBA}$ to nAx



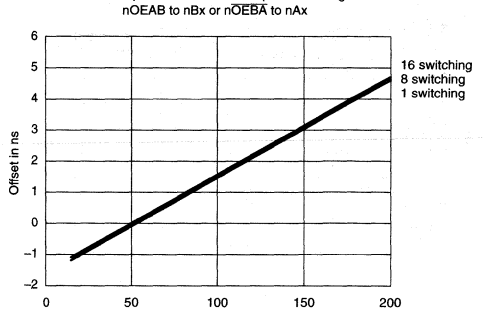
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
nOEAB to nBx or $n\overline{OEBA}$ to nAx



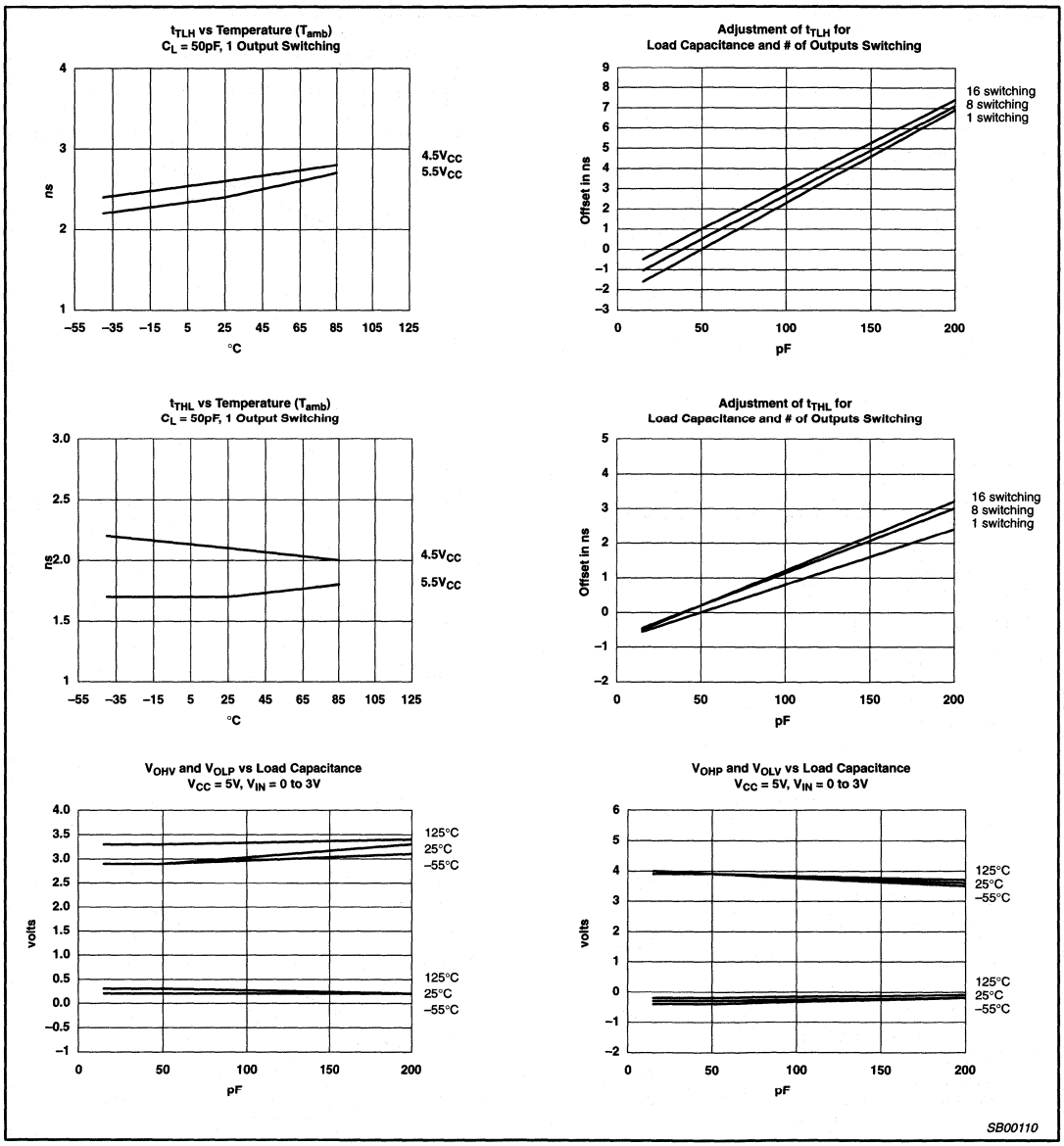
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nOEAB to nBx or $n\overline{OEBA}$ to nAx



Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
nOEAB to nBx or $n\overline{OEBA}$ to nAx



SB00109


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
SB00110

16-bit bus transceiver/register (3-State) MB2646

FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiplexed real-time and stored data
- Outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2646 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2646 16-bit transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($n\overline{OE}$) and Direction (nDIR) pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

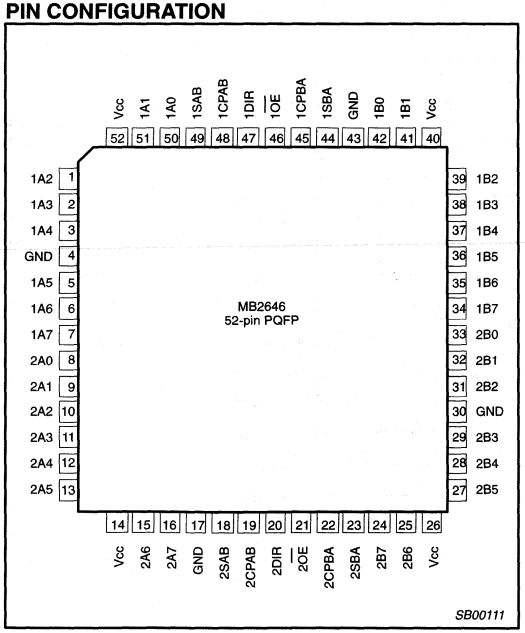
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	3.9 4.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2646 BB	MB2646 BB	SOT379-1

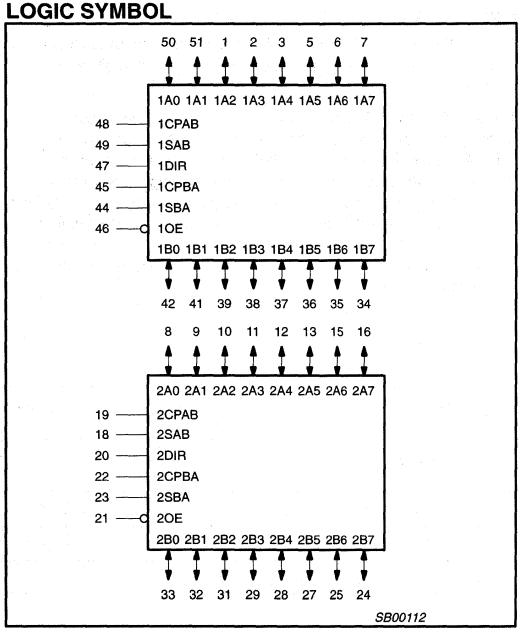
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
48, 45, 19, 22	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
49, 44, 18, 23	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
47, 20	1DIR, 2DIR	Direction control inputs
50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
46, 21	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

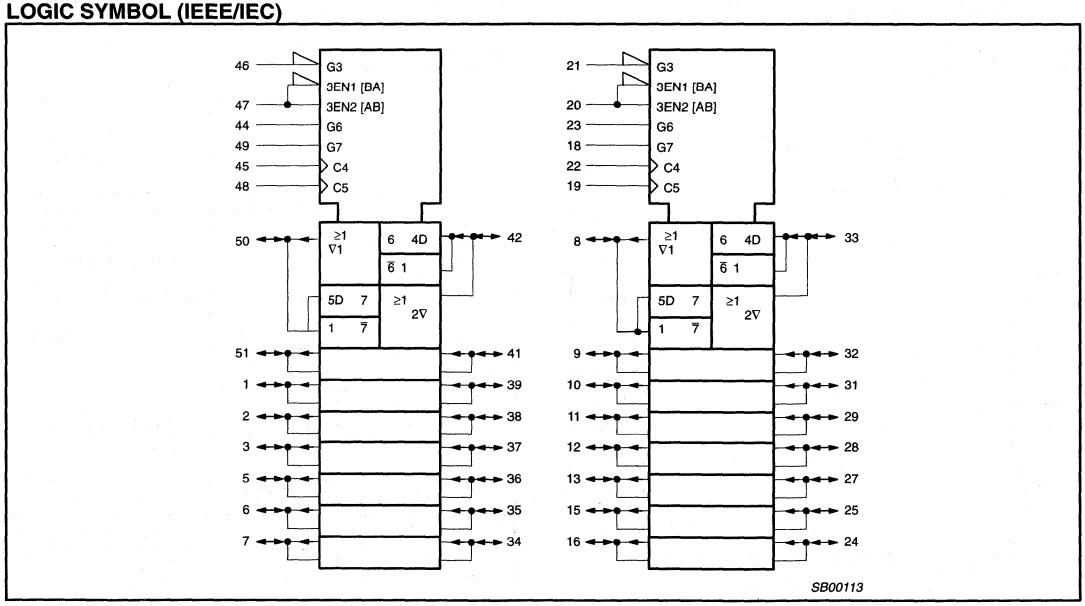
LOGIC SYMBOL



DESCRIPTION (continued)

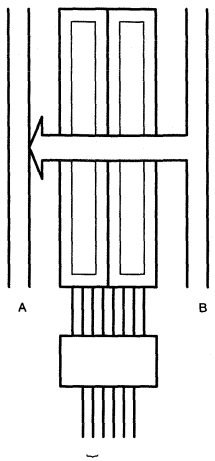
The select (nSAB, nSBA) pins determine whether data is stored or transferred through the device in real-time. The nDIR determines which bus will receive data when the $n\overline{OE}$ is active Low. In the isolation mode ($n\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

LOGIC SYMBOL (IEEE/IEC)



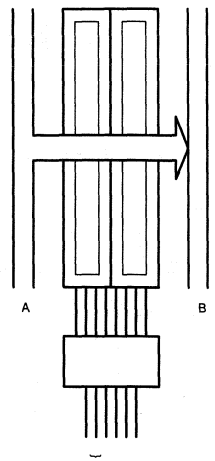
The following examples demonstrate the four fundamental bus-management functions that can be performed with the MB2646.

REAL TIME BUS TRANSFER
BUS B TO BUS A



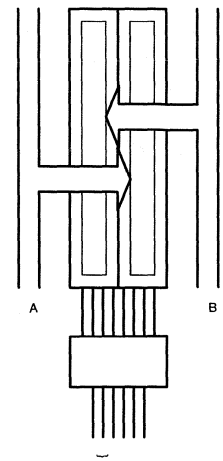
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER
BUS A TO BUS B



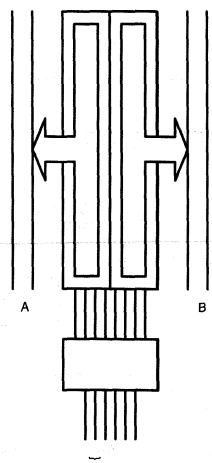
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	X	X	L	X

STORAGE FROM
A, B, OR A AND B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	↑	X	X	X
L	L	X	↑	X	X
H	X	↑	↑	X	X

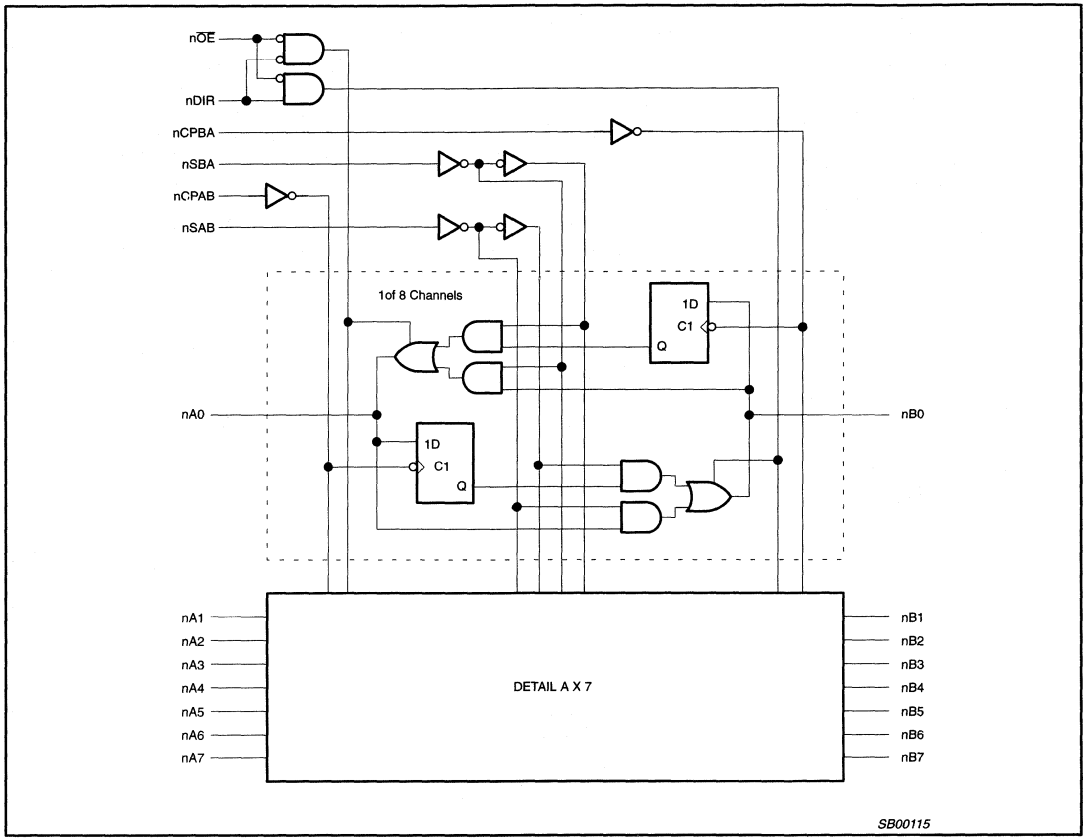
TRANSFER STORED DATA
TO A OR B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	H/L	X	H
L	H	H/L	X	H	X

SB00114

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOE	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOE input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low–level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]		V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3–State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3–State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		37	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	130	190		130		MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	2.2 2.4	3.9 4.6	5.1 5.4	2.2 2.4	5.6 5.9	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.5 1.5	3.1 3.3	4.3 4.5	1.5 1.5	4.8 5.0	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	2, 3	1.5 1.8	3.7 3.9	4.8 4.9	1.5 1.8	5.5 5.6	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OE}$ to nAx or nBx	5 6	1.5 2.1	3.5 4.4	4.8 5.6	1.5 2.1	5.6 6.4	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OE}$ to nAx or nBx	5 6	2.1 1.5	3.8 3.1	5.0 4.2	2.1 1.5	5.7 4.7	ns
t_{PZH} t_{PZL}	Output enable time nDIR to nAx or nBx	5 6	1.5 2.3	4.2 4.9	5.4 6.2	1.5 2.3	6.2 6.9	ns
t_{PHZ} t_{PLZ}	Output disable time nDIR to nAx or nBx	5 6	2.1 1.5	3.8 3.2	5.0 4.3	2.1 1.5	5.7 5.0	ns

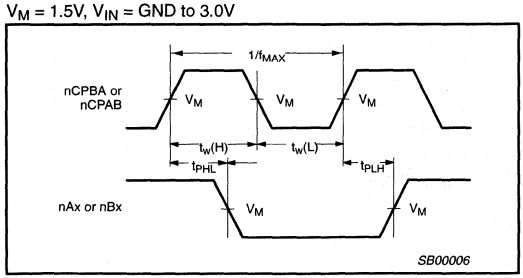
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

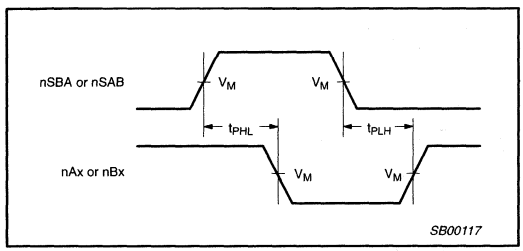
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time nAx to nCPAB, nBx to nCPBA	4	2.0 1.5	0.7 0.0	2.0 1.5	ns
t_h(H) t_h(L)	Hold time nAx to nCPAB, nBx to nCPBA	4	1.5 1.0	0.0 –0.7	1.5 1.0	ns
t_w(H) t_w(L)	Pulse width, High or Low nCPAB or nCPBA	1	4.5 3.0	2.5 2.0	4.5 3.0	ns

AC WAVEFORMS

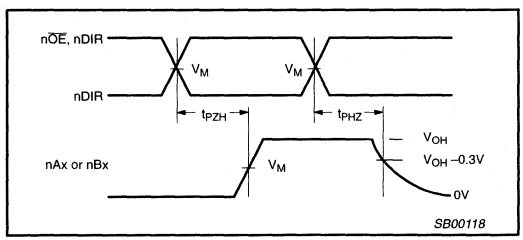
V_M = 1.5V, V_{IN} = GND to 3.0V



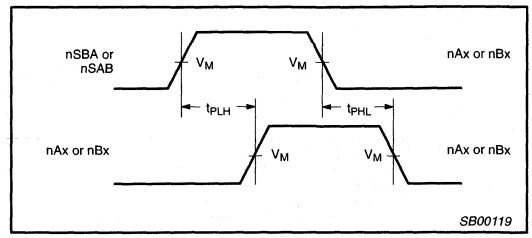
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



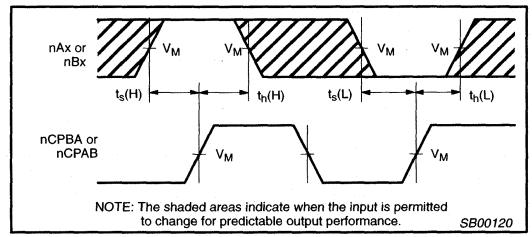
Waveform 2. Propagation Delay, nSBA to nAx or nSAB to nBx



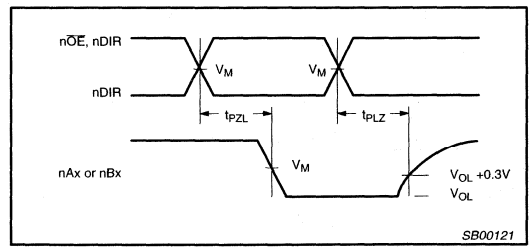
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



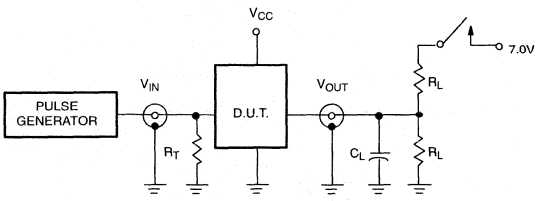
Waveform 4. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx



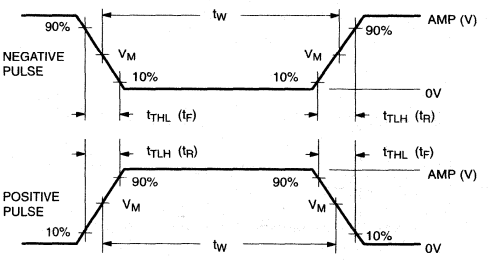
Waveform 5. Data Setup and Hold Times



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

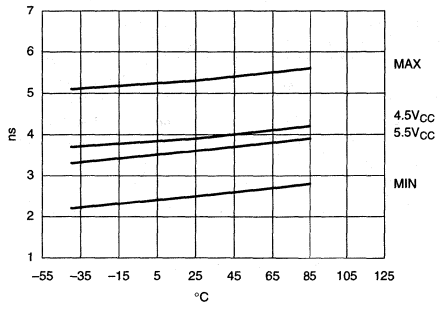
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

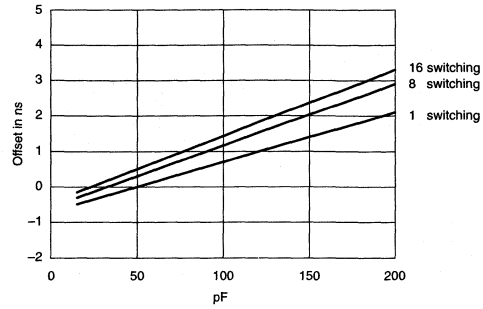
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

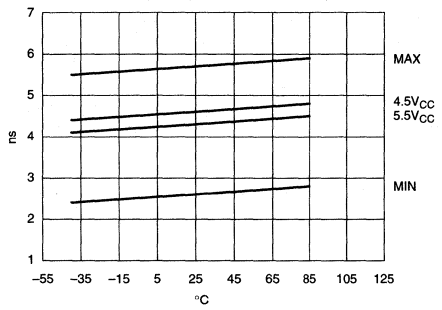
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCPAB to nBx or nCPBA to nAx



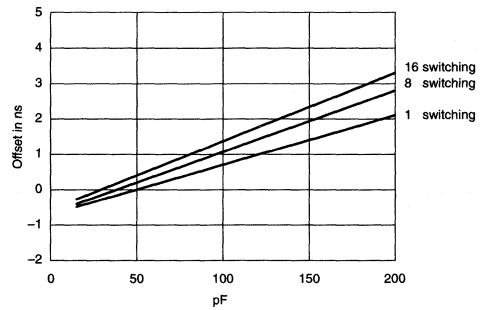
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nCPAB to nBx or nCPBA to nAx



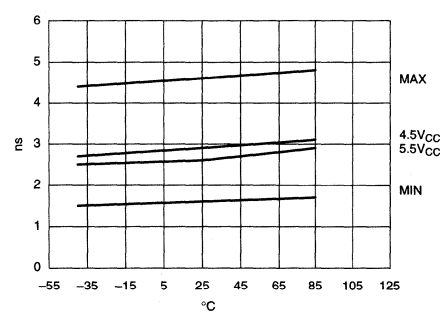
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCPAB to nBx or nCPBA to nAx



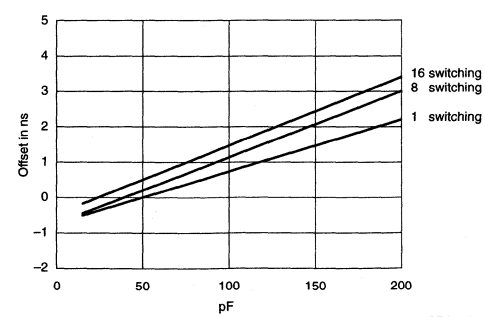
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nCPAB to nBx or nCPBA to nAx



t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx or nBx to nAx

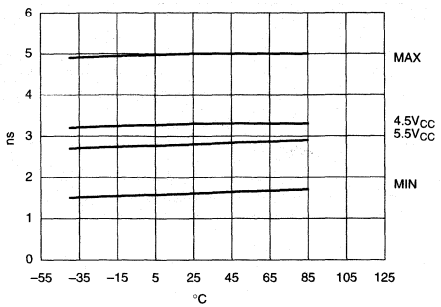


Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nAx to nBx or nBx to nAx

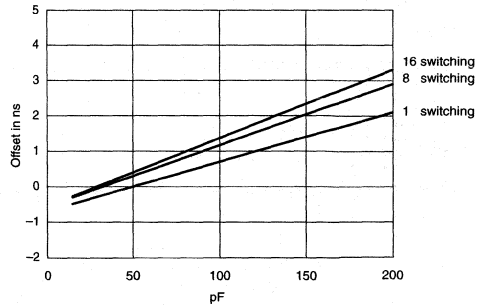


SB00122

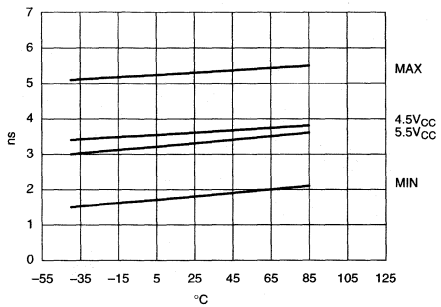
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx or nBx to nAx



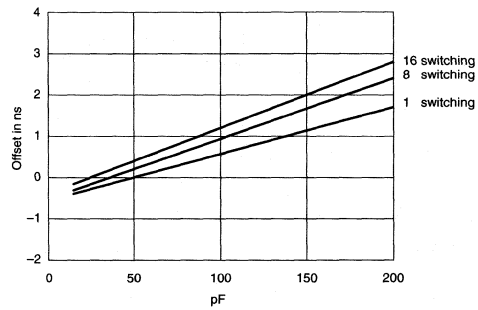
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nAx to nBx or nBx to nAx



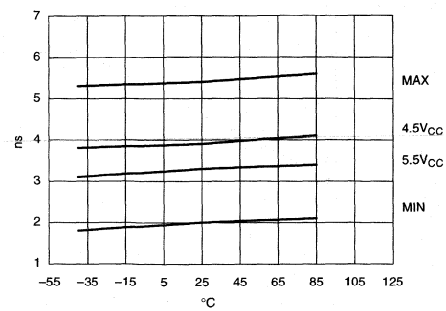
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nSAB to nBx or nSBA to nAx



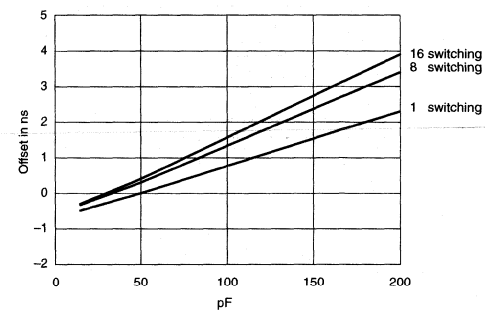
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nSAB to nBx or nSBA to nAx



t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nSAB to nBx or nSBA to nAx

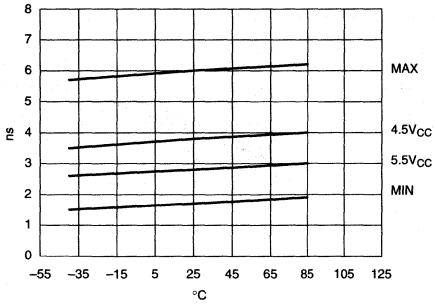


Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nSAB to nBx or nSBA to nAx

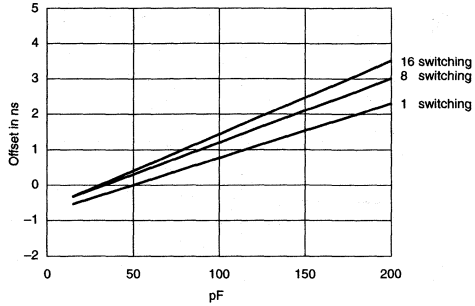


SB00123

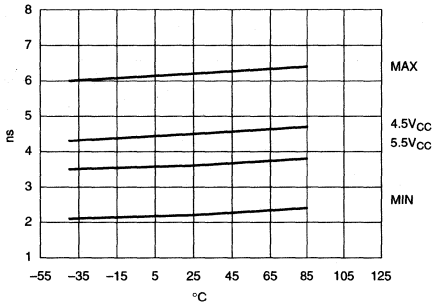
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nAx or nBx



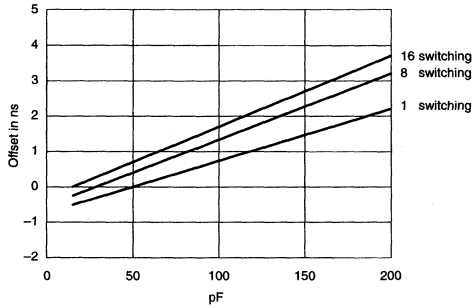
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nAx or nBx



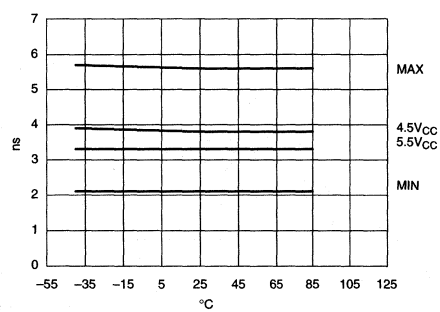
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nAx or nBx



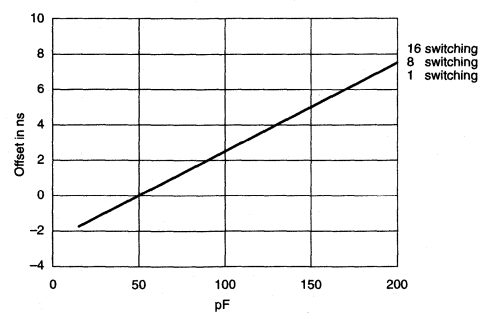
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nAx or nBx



t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nAx or nBx

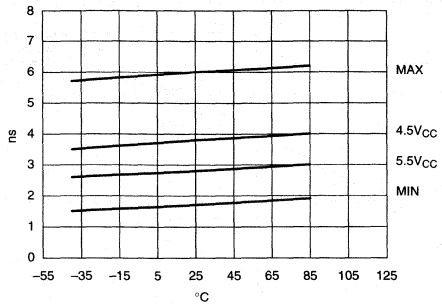


Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nAx or nBx

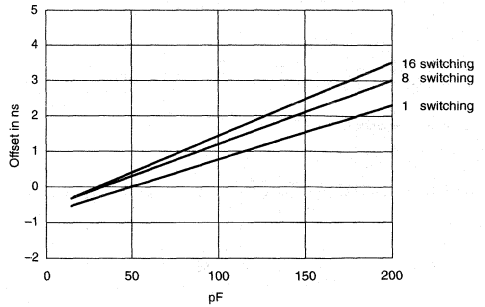


SB00124

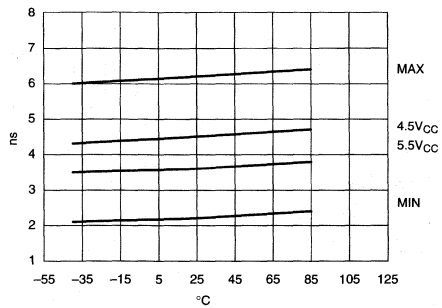
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nAx or nBx



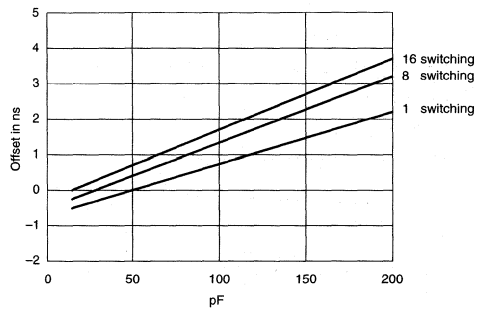
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nAx or nBx



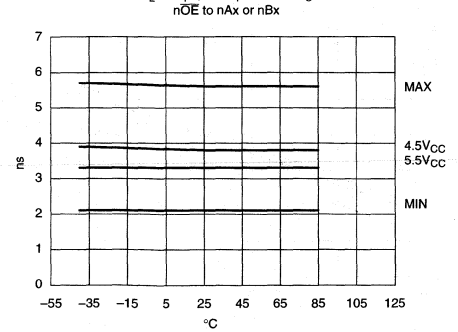
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nAx or nBx



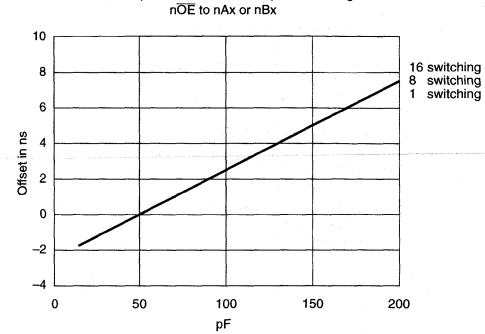
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nAx or nBx



t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nAx or nBx

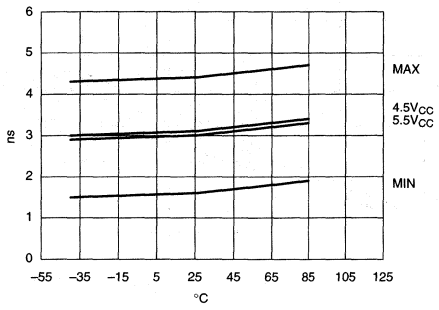


Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nAx or nBx

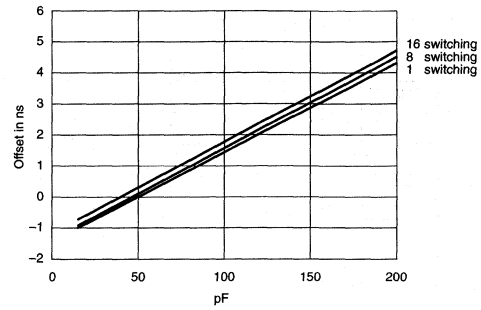


SB00125

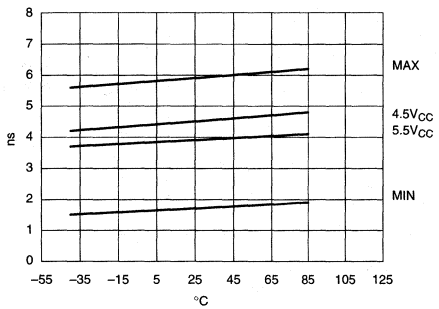
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nAx or nBx



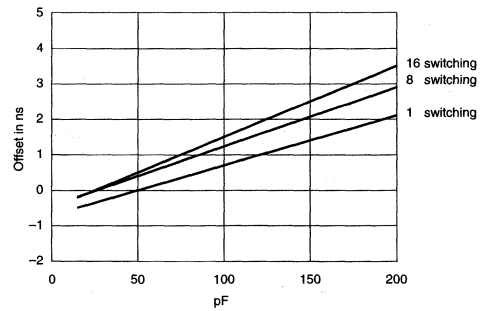
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nAx or nBx



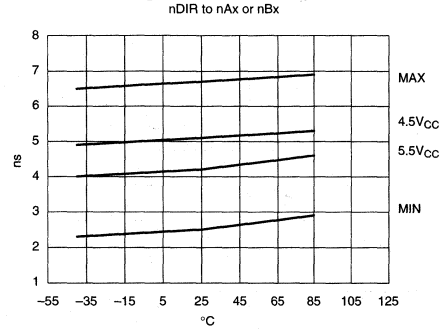
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nDIR to nAx or nBx



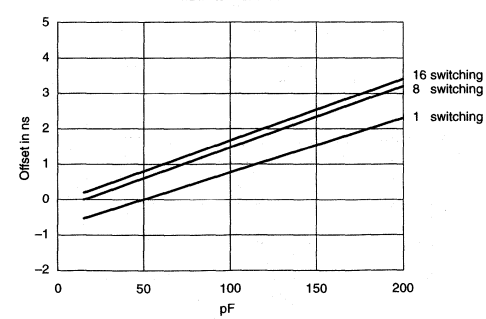
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
nDIR to nAx or nBx



t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nDIR to nAx or nBx



Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
nDIR to nAx or nBx



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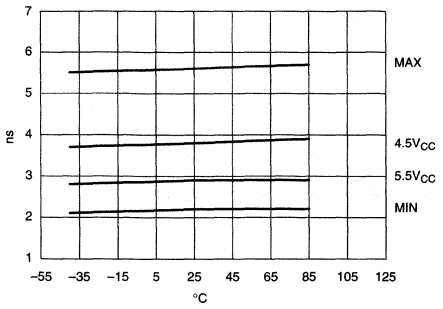
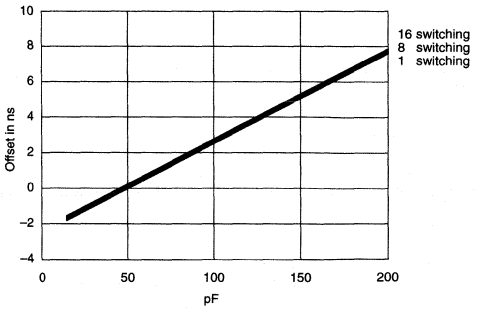
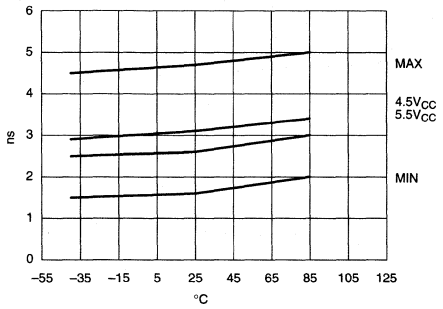
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nDIR to nAx or nBx



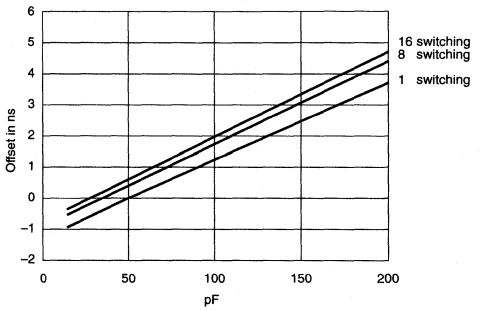
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
nDIR to nAx or nBx



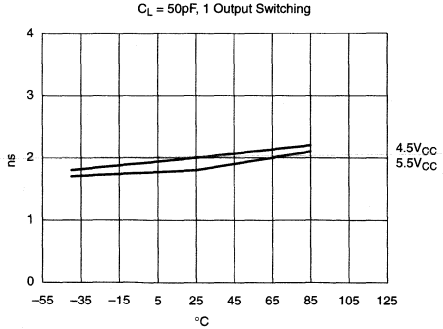
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nDIR to nAx or nBx



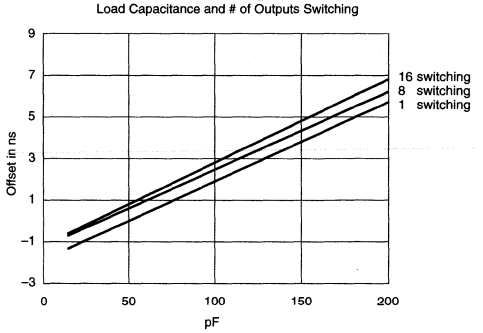
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
nDIR to nAx or nBx



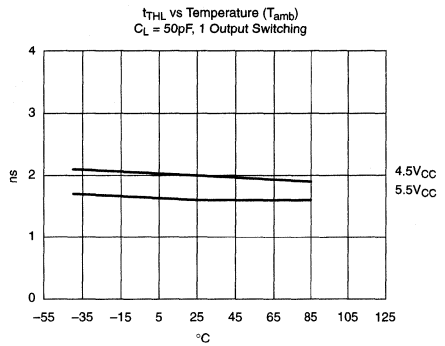
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching

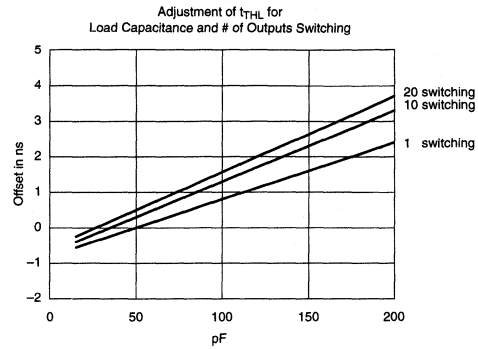


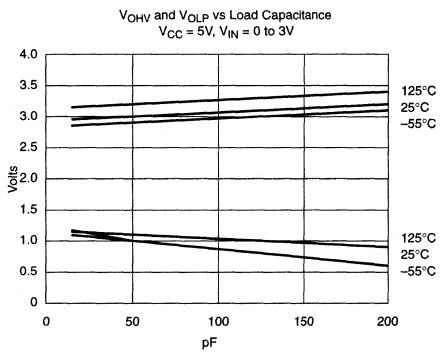
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching

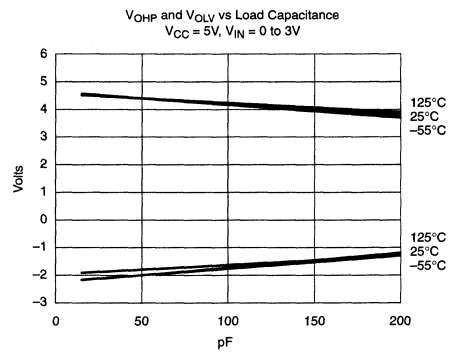


SB00127


t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}


Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
20 switching
10 switching
1 switching


V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C


V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
–55°C
125°C
25°C
–55°C

SB00128

16-bit transceiver/register, non-inverting (3-State) MB2652

FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiplexed real-time and stored data
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2652 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2652 transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (nOEAB, ($n\overline{OEBA}$) and Select ($n\overline{SAB}$, $n\overline{SBA}$) pins are provided for bus management.

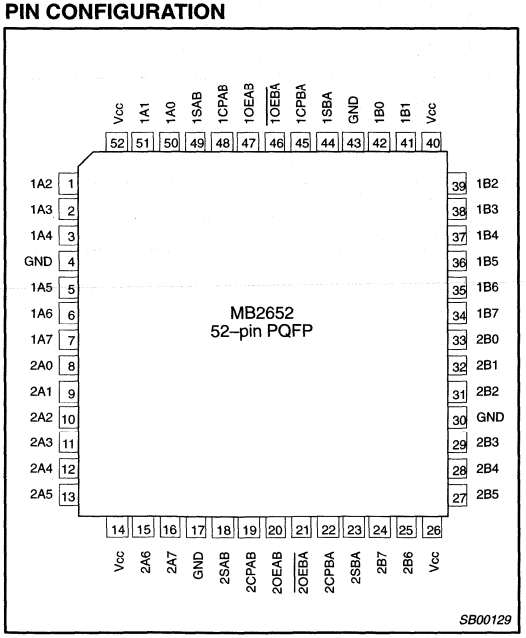
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	3.9 4.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

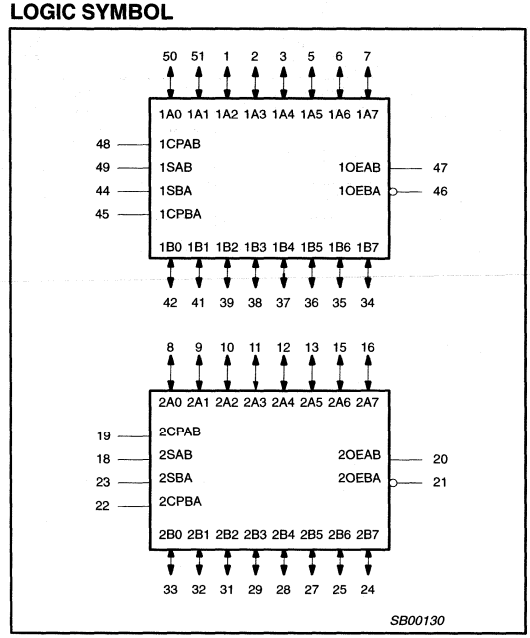
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2652 BB	MB2652 BB	SOT379-1

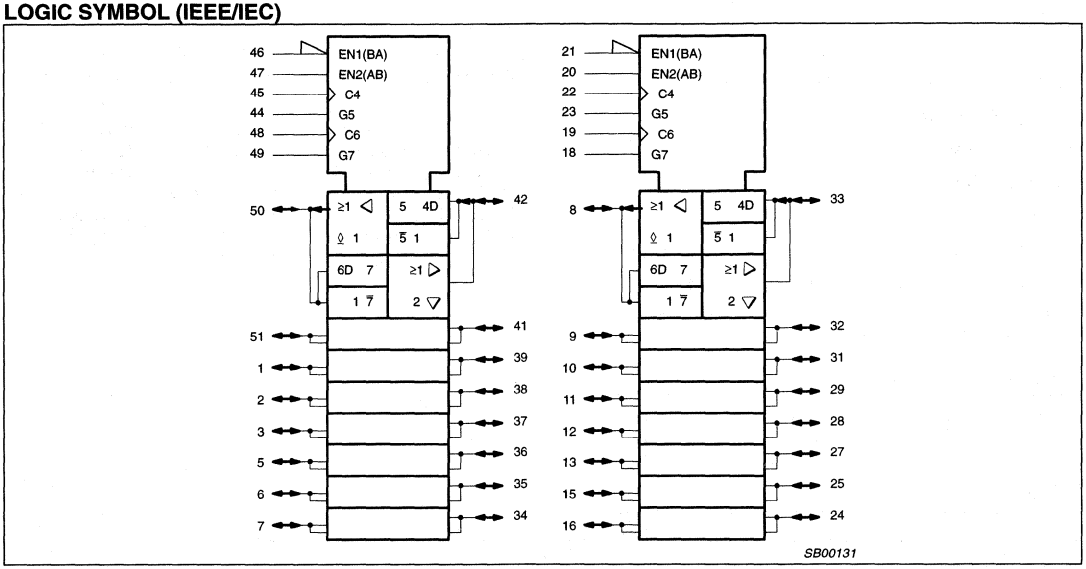
PIN CONFIGURATION



LOGIC SYMBOL



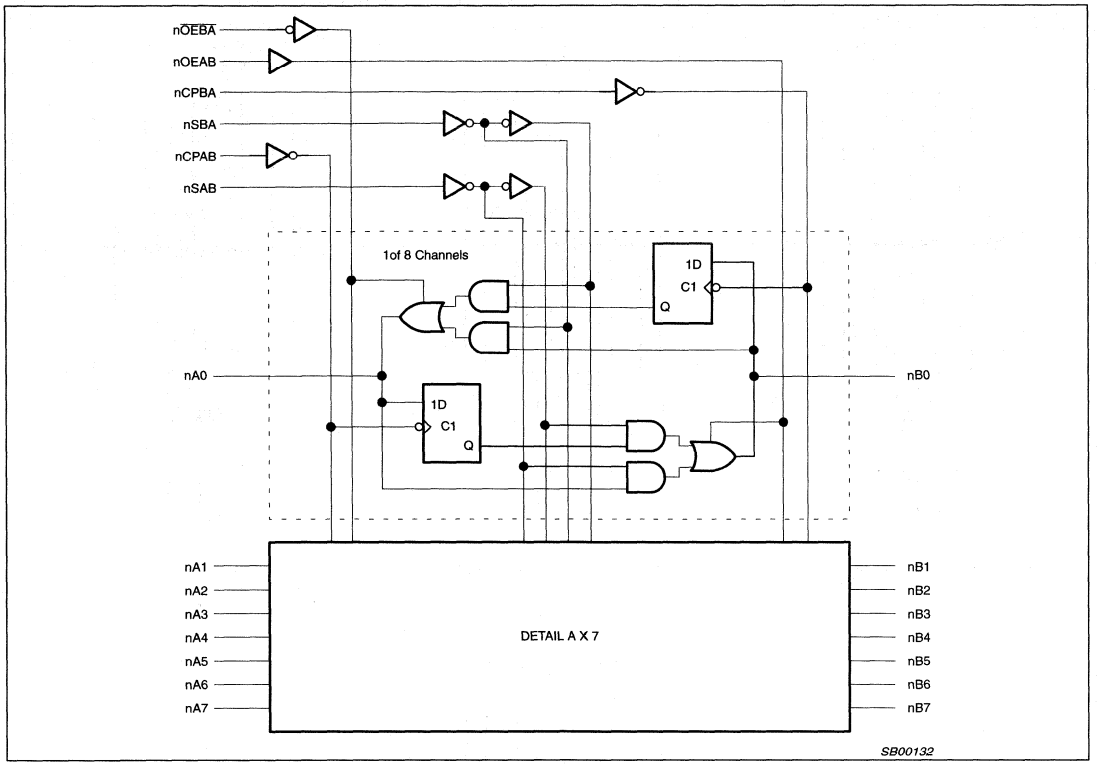
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
48, 45, 19, 22	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
49, 44, 18, 23	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
47, 46, 20, 21	1OEAB, $1\overline{OEBA}$, 2OEAB, $2\overline{OEBA}$	Output enable inputs
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



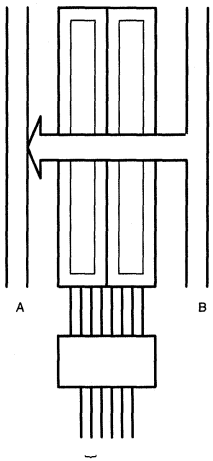
FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOEBA and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (nSAB and nSBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

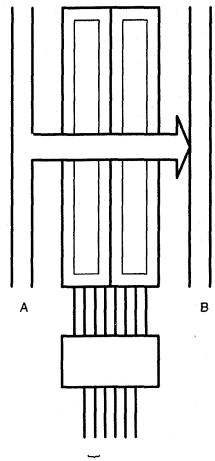
The following examples demonstrate the four fundamental bus-management functions that can be performed with the MB2652.The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

REAL TIME BUS TRANSFER
BUS B TO BUS A



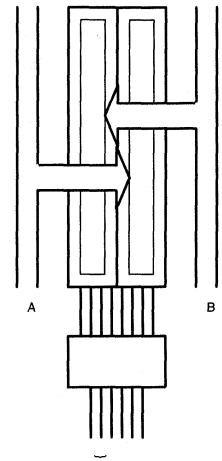
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER
BUS A TO BUS B



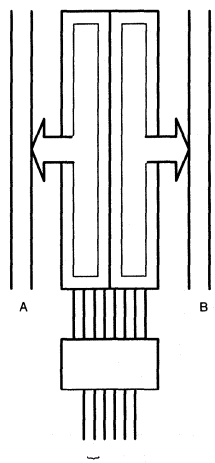
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
H	H	X	X	L	X

STORAGE FROM
A, B, OR A AND B



nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA
TO A OR B



nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
H	L	H|L	H|L	H	H

SB00133

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low–level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5V; I_{OL} = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]		V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = $V_{\overline{OE}}$ = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3–State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3–State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{cc}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		38	60		60	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	130	190		130		MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	2.1 2.7	3.9 4.4	5.3 5.7	2.1 2.7	5.8 6.3	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	4	1.4 1.4	3.2 3.3	4.3 4.7	1.4 1.4	4.8 5.3	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	2	1.3 2.1	3.6 3.8	5.0 5.3	1.3 2.1	5.6 5.8	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OEBA}$ to nAx	5 3	1.0 1.8	2.9 3.6	4.1 4.8	1.0 1.8	4.8 5.5	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OEBA}$ to nAx	5 3	1.0 1.6	3.8 3.2	5.0 4.5	1.0 1.6	5.5 5.1	ns
t_{PZH} t_{PZL}	Output enable time nOEAB to nBx	5 3	1.2 2.7	3.7 4.5	5.0 5.8	1.2 2.7	5.6 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time nOEAB to nBx	5 3	1.0 1.2	3.4 3.1	4.7 4.2	1.0 1.2	5.3 4.9	ns

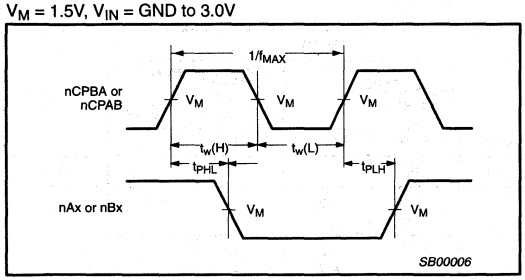
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

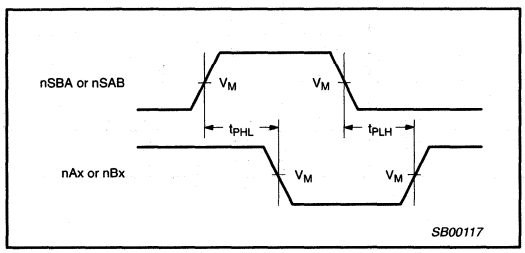
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time nAx to nCPBA, nBx to nCPAB	5	2.0 1.5	0.8 -0.1	2.0 1.5	ns
t_h(H) t_h(L)	Hold time nAx to nCPBA, nBx to nCPAB	5	1.5 1.0	0.1 -0.7	1.5 1.0	ns
t_w(H) t_w(L)	Pulse width, High or Low nCPAB or nCPBA	1	4.5 3.0	2.5 2.0	4.5 3.0	ns

AC WAVEFORMS

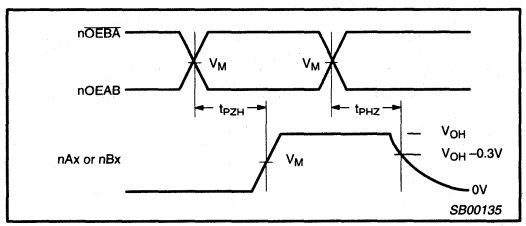
V_M = 1.5V, V_{IN} = GND to 3.0V



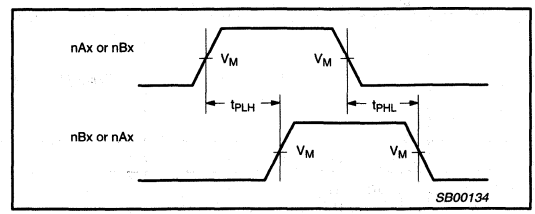
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



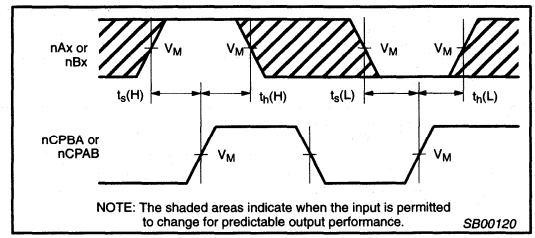
Waveform 2. Propagation Delay, SBA TO nAx or SAB nBx



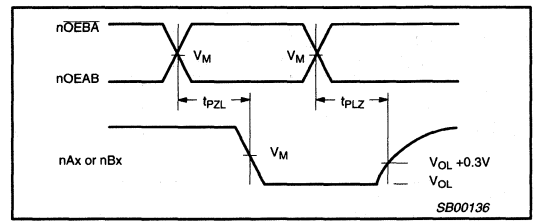
Waveform 3. 3-State Output Enable Time to High Level and Output Enable Time from High Level



Waveform 4. Propagation Delay, nAx to nBx or nBx to nAx

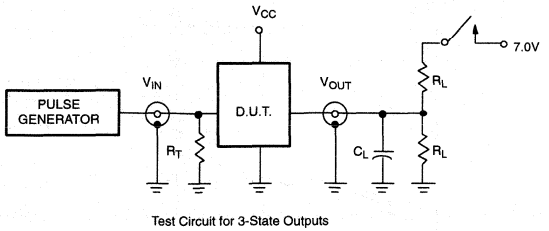


Waveform 5. Data Setup and Hold Times

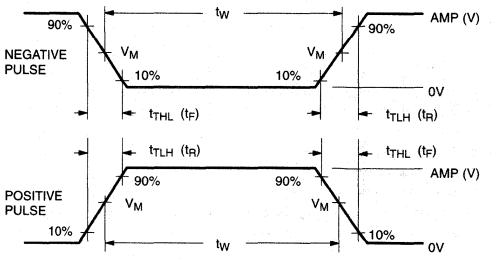


Waveform 6. 3-State Output Disable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

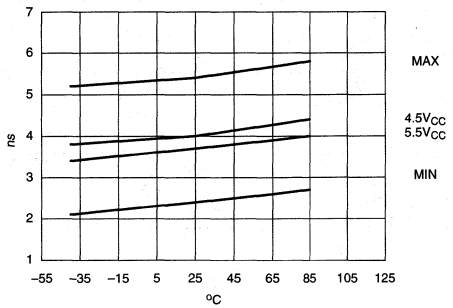
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

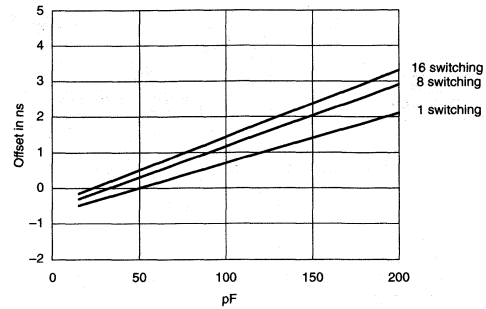
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

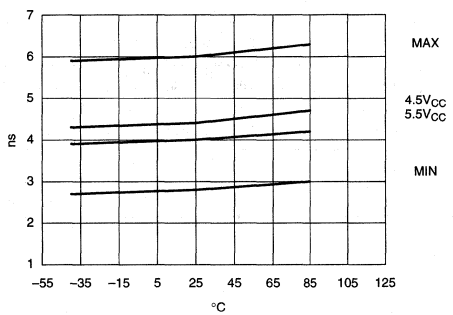
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCPAB to nBx or nCPBA to nAx



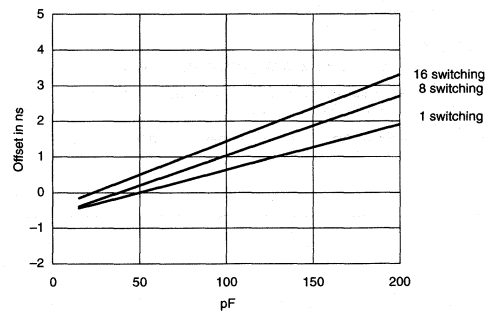
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nCPAB to nBx or nCPBA to nAx



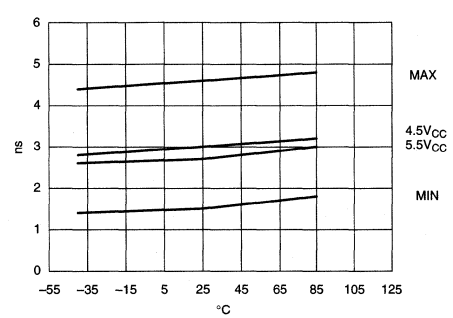
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCPAB to nBx or nCPBA to nAx



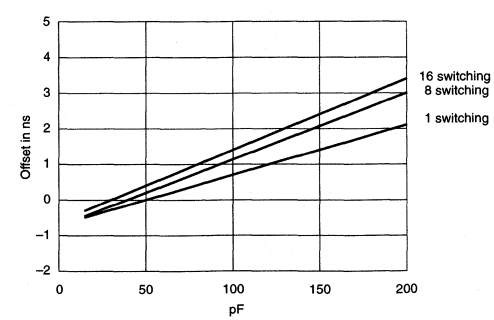
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nCPAB to nBx or nCPBA to nAx



t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx or nBx to nAx

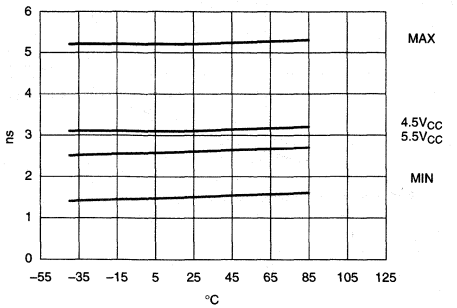


Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nAx to nBx or nBx to nAx

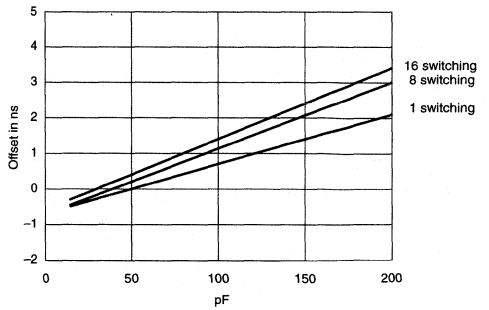


SB00137

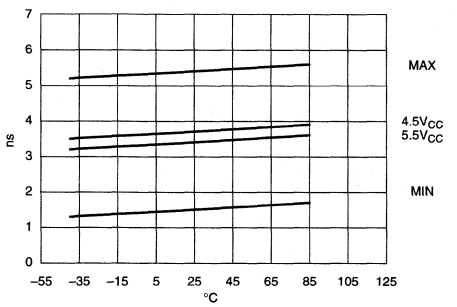
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nBx or nBx to nAx



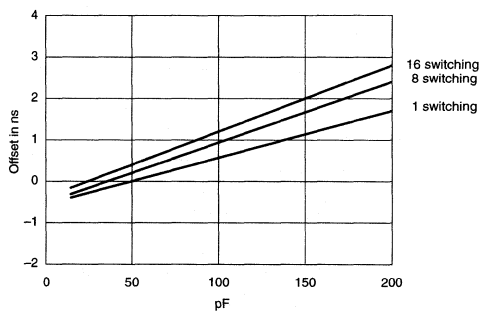
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nAx to nBx or nBx to nAx



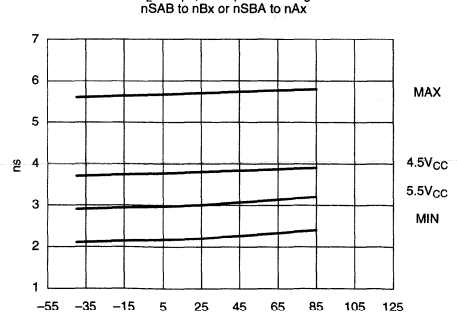
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nSAB to nBx or nSBA to nAx



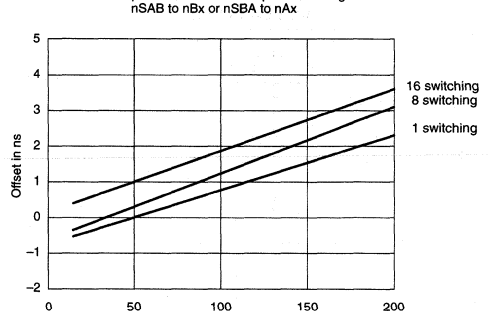
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nSAB to nBx or nSBA to nAx



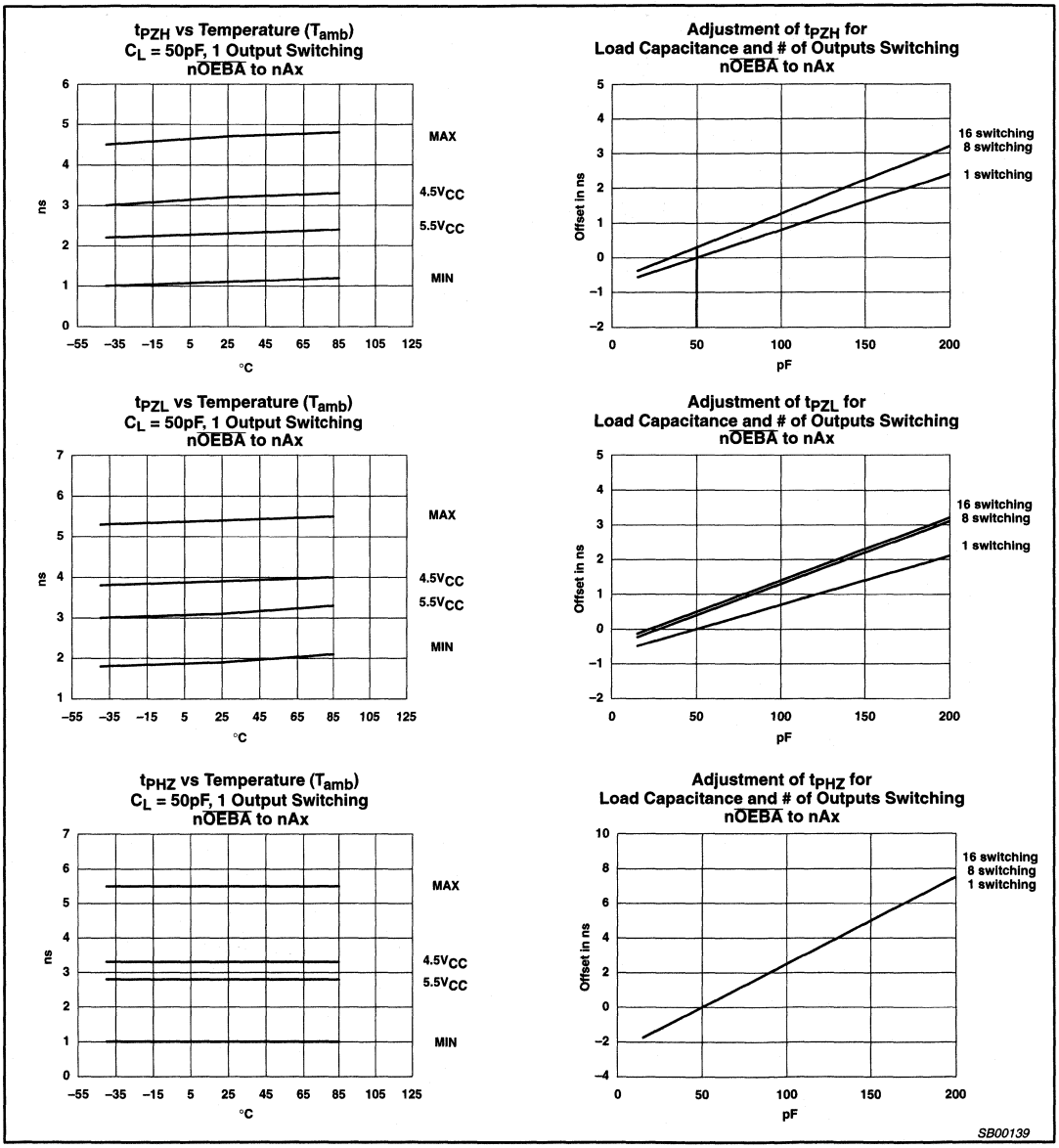
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nSAB to nBx or nSBA to nAx



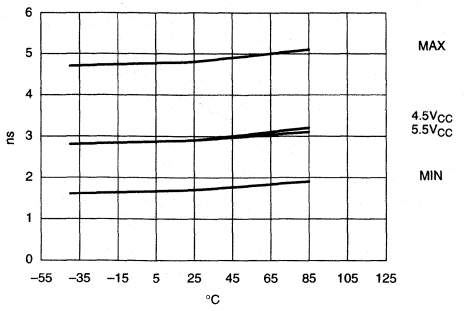
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nSAB to nBx or nSBA to nAx



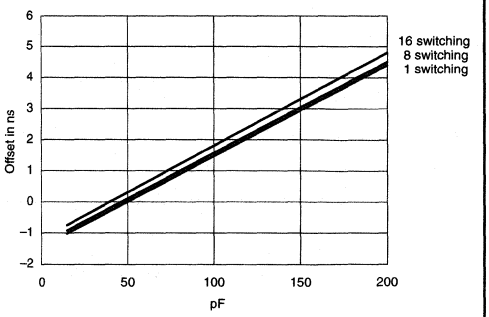
SB00138


tPZH vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOEBA to nAx
ns
°C
MAX
4.5VCC
5.5VCC
MIN
Adjustment of tPZH for
Load Capacitance and # of Outputs Switching
nOEBA to nAx
Offset in ns
pF
16 switching
8 switching
1 switching
tPZL vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOEBA to nAx
Adjustment of tPZL for
Load Capacitance and # of Outputs Switching
nOEBA to nAx
tPHZ vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOEBA to nAx
Adjustment of tPHZ for
Load Capacitance and # of Outputs Switching
nOEBA to nAx
SB00139

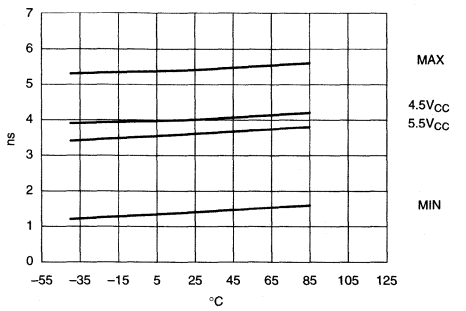
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OEBA}$ to nAx



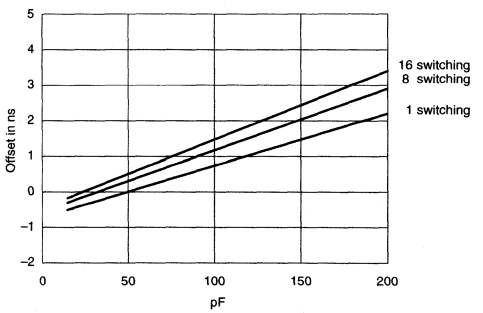
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OEBA}$ to nAx



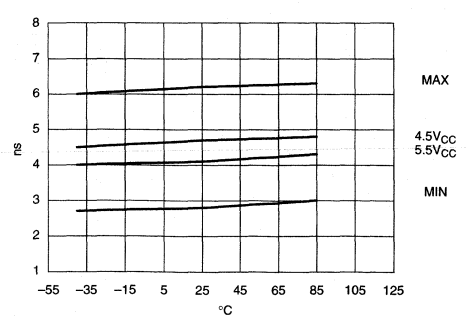
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nOEAB to nBx



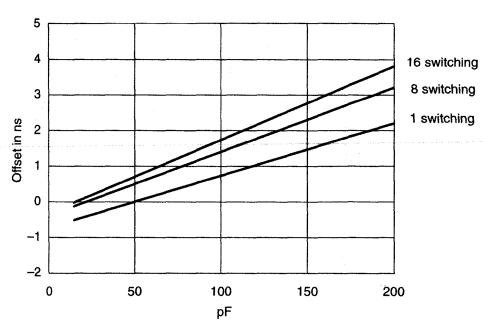
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
nOEAB to nBx



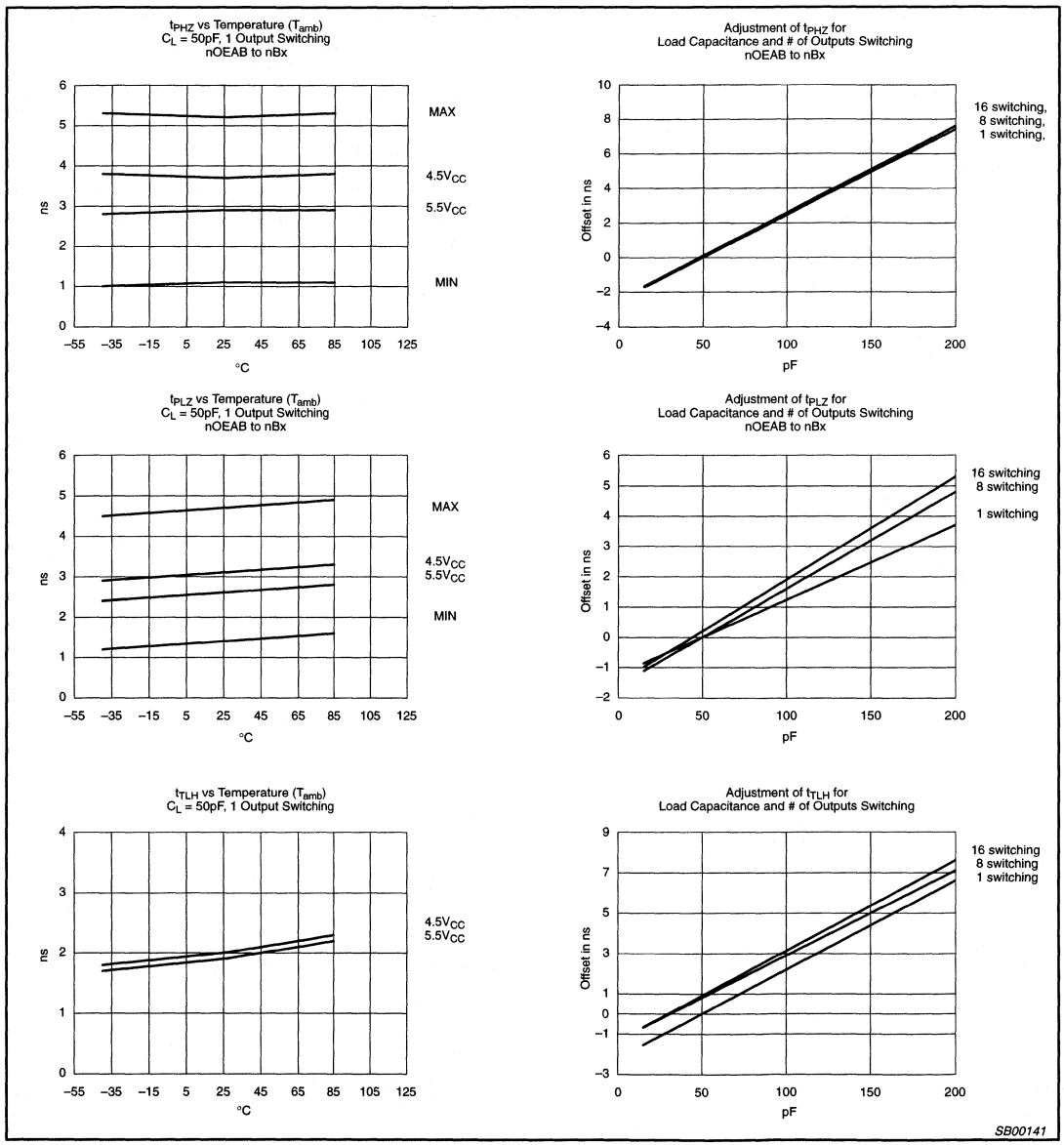
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nOEAB to nBx

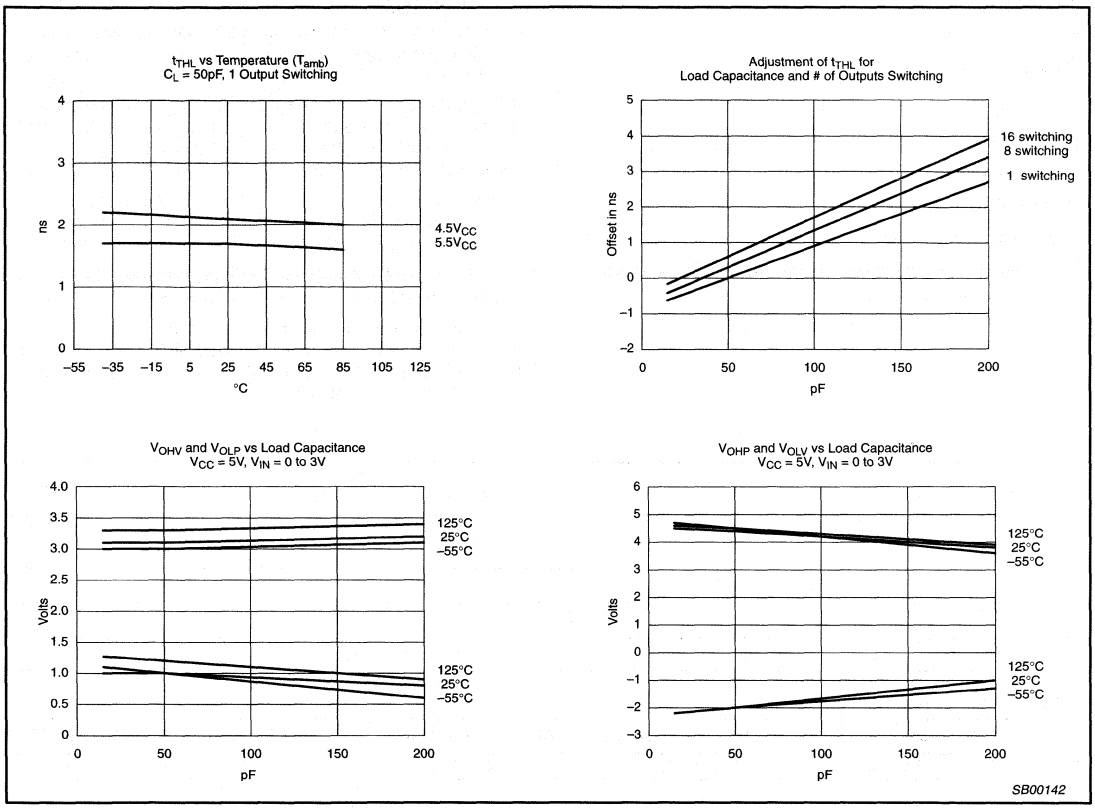


Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
nOEAB to nBx



SB00140


tPHZ vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOEAB to nBx
ns
°C
MAX
4.5VCC
5.5VCC
MIN
Adjustment of tPHZ for
Load Capacitance and # of Outputs Switching
nOEAB to nBx
Offset in ns
pF
16 switching,
8 switching,
1 switching,
tPLZ vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOEAB to nBx
Adjustment of tPLZ for
Load Capacitance and # of Outputs Switching
nOEAB to nBx
16 switching
8 switching
1 switching
tTLH vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
Adjustment of tTLH for
Load Capacitance and # of Outputs Switching
SB00141


t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
16 switching
8 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
–55°C
SB00142

20-bit D-type flip-flop; positive-edge trigger (3-State) MB2821

FEATURES

- 20-bit positive-edge triggered register
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2821 has two 10-bit, edge triggered registers, with each register coupled to ten 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($n\overline{OE}$) controls all ten 3-State buffers independent of the register operation. When $n\overline{OE}$ is Low, the data in the register appears at the outputs. When $n\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

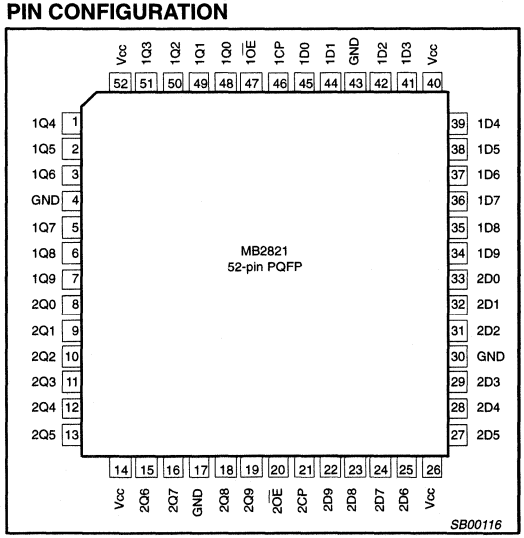
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	4.4 4.6	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2821 BB	MB2821 BB	SOT379-1

PIN CONFIGURATION

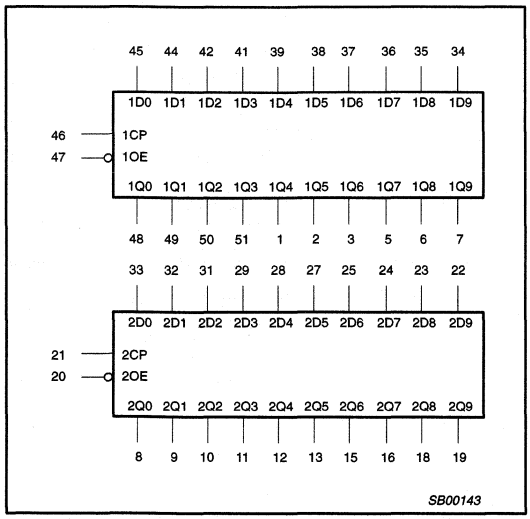


PIN DESCRIPTION

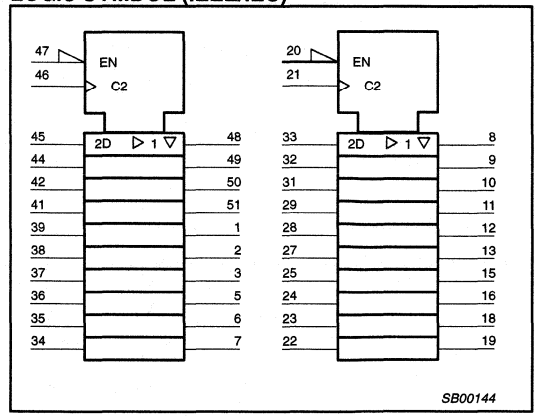
PIN NUMBER	SYMBOL	FUNCTION
45, 44, 42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24, 23, 22	1D0 – 1D9 2D0 – 2D9	Data inputs
48, 49, 50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 18, 19	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
47, 20	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
46, 21	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

20-bit D-type flip-flop; positive-edge trigger (3-State) MB2821

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

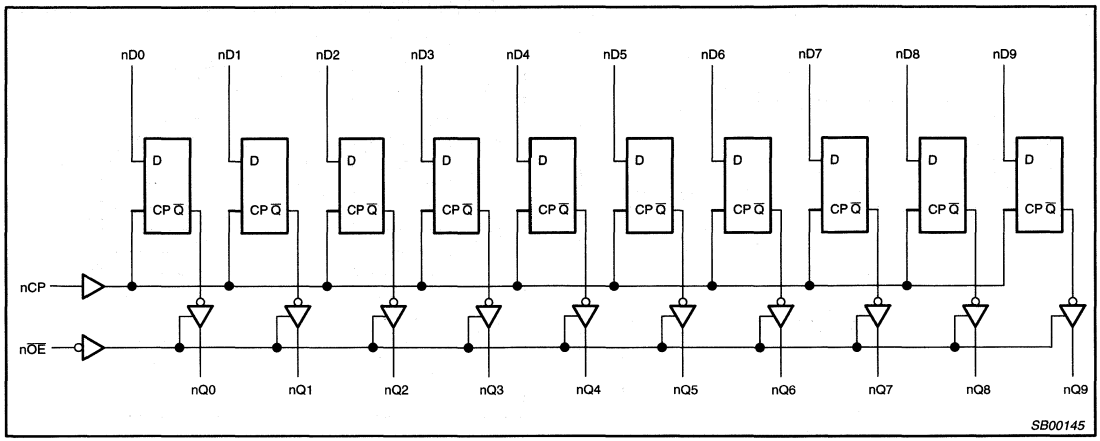


FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx	REGISTER	nQ0 – nQ9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $\overline{V_{OE}}$ = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−70	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		54	76		76	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

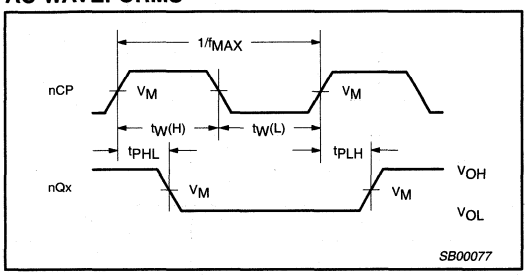
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	160	250		160		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	2.5 2.7	4.4 4.6	5.6 6.0	2.5 2.7	6.4 6.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2 4	1.2 2.2	3.3 3.8	4.2 5.1	1.2 2.2	5.0 5.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2 4	1.3 1.5	3.2 3.0	4.6 4.2	1.3 1.5	5.0 4.7	ns

AC SETUP REQUIREMENTS

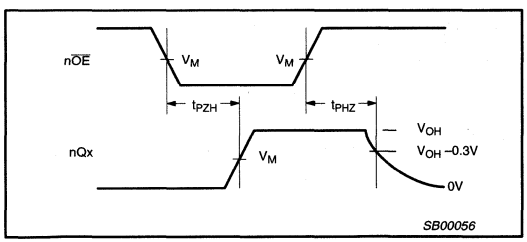
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nCP	3	1.5 1.0	0.6 –0.2		1.5 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	3	1.0 1.0	0.3 –0.4		1.0 1.0		ns
$t_w(H)$ $t_w(L)$	nCP pulse width High or Low	1	3.5 3.0	2.2 1.6		3.5 3.0		ns

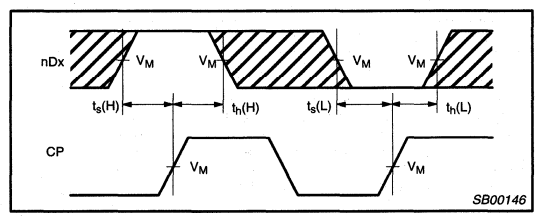
AC WAVEFORMS



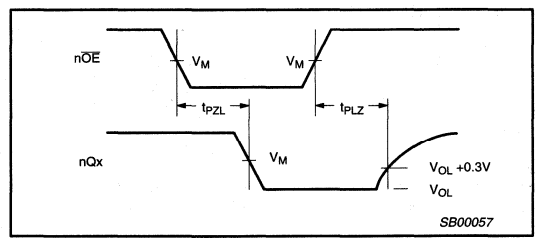
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

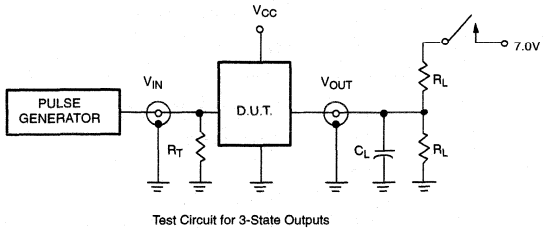


Waveform 3. Data Setup and Hold Times

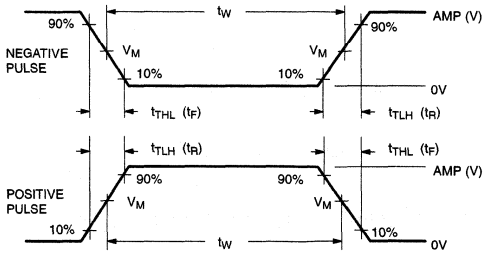


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

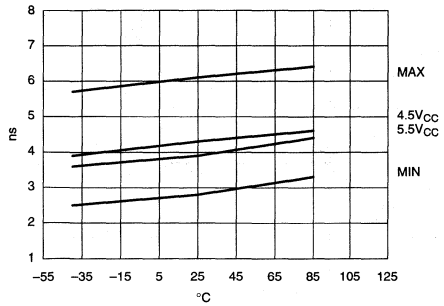
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

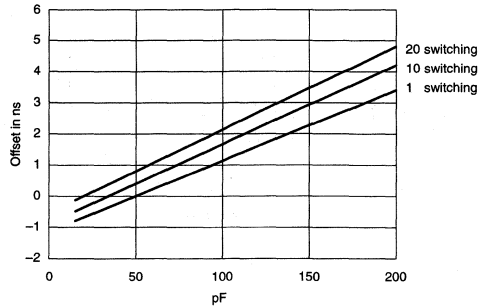
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

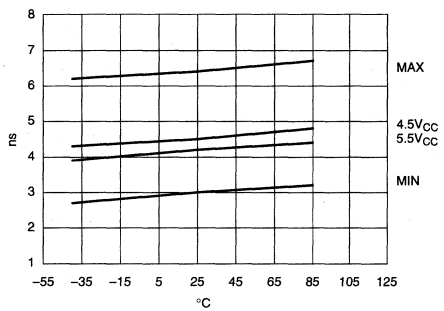
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCP to nQx



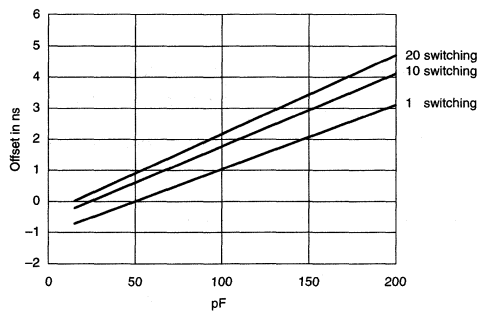
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nCP to nQx



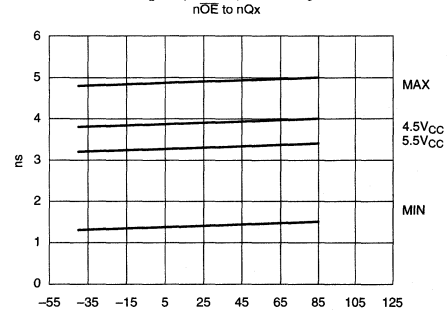
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCP to nQx



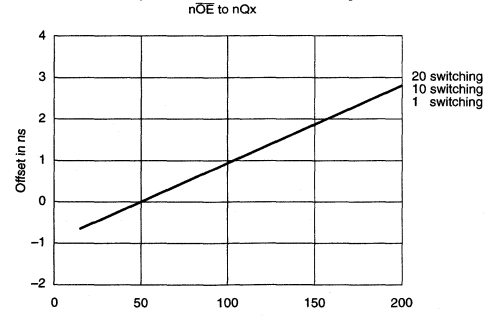
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nCP to nQx



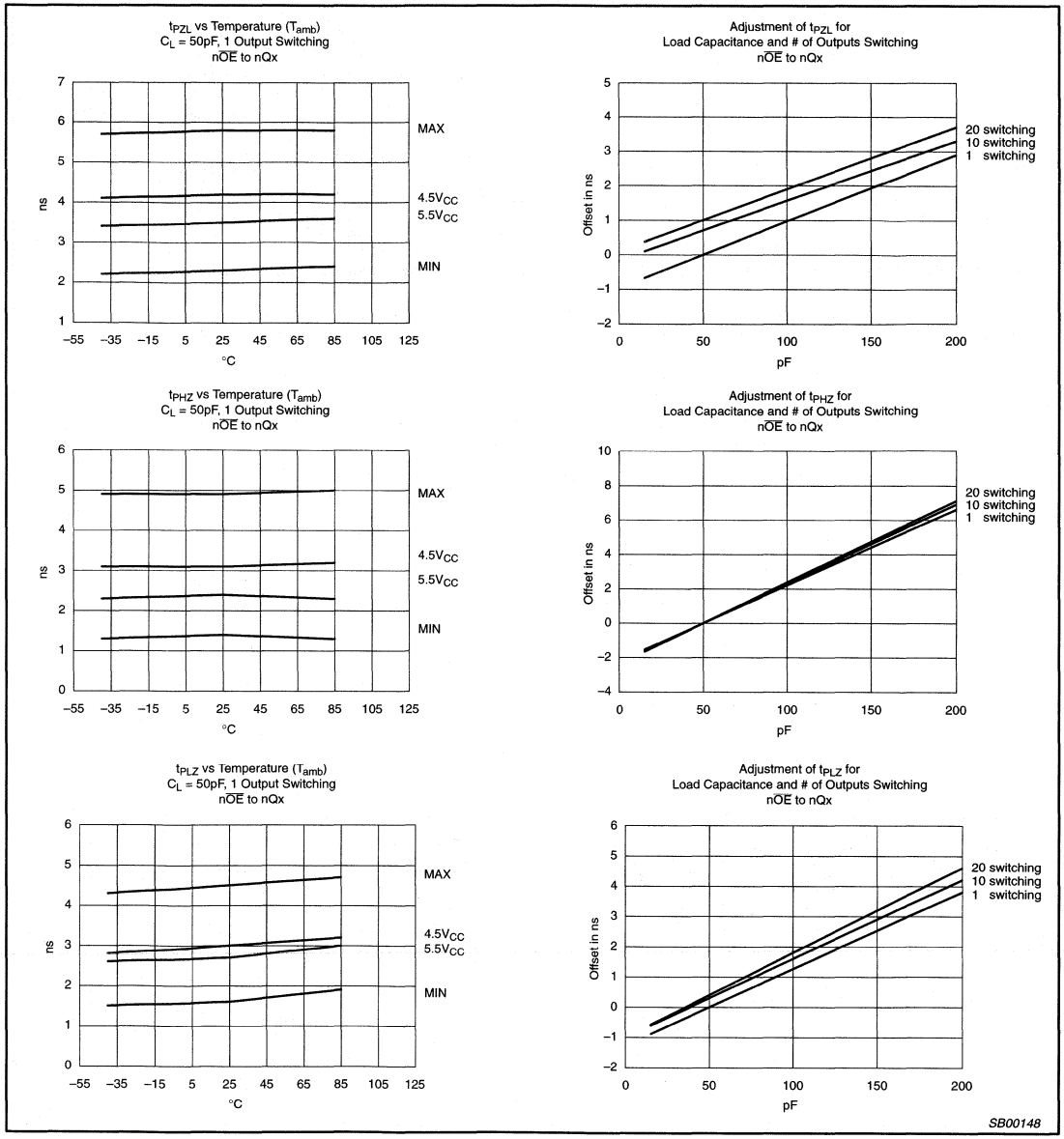
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$ to nQx

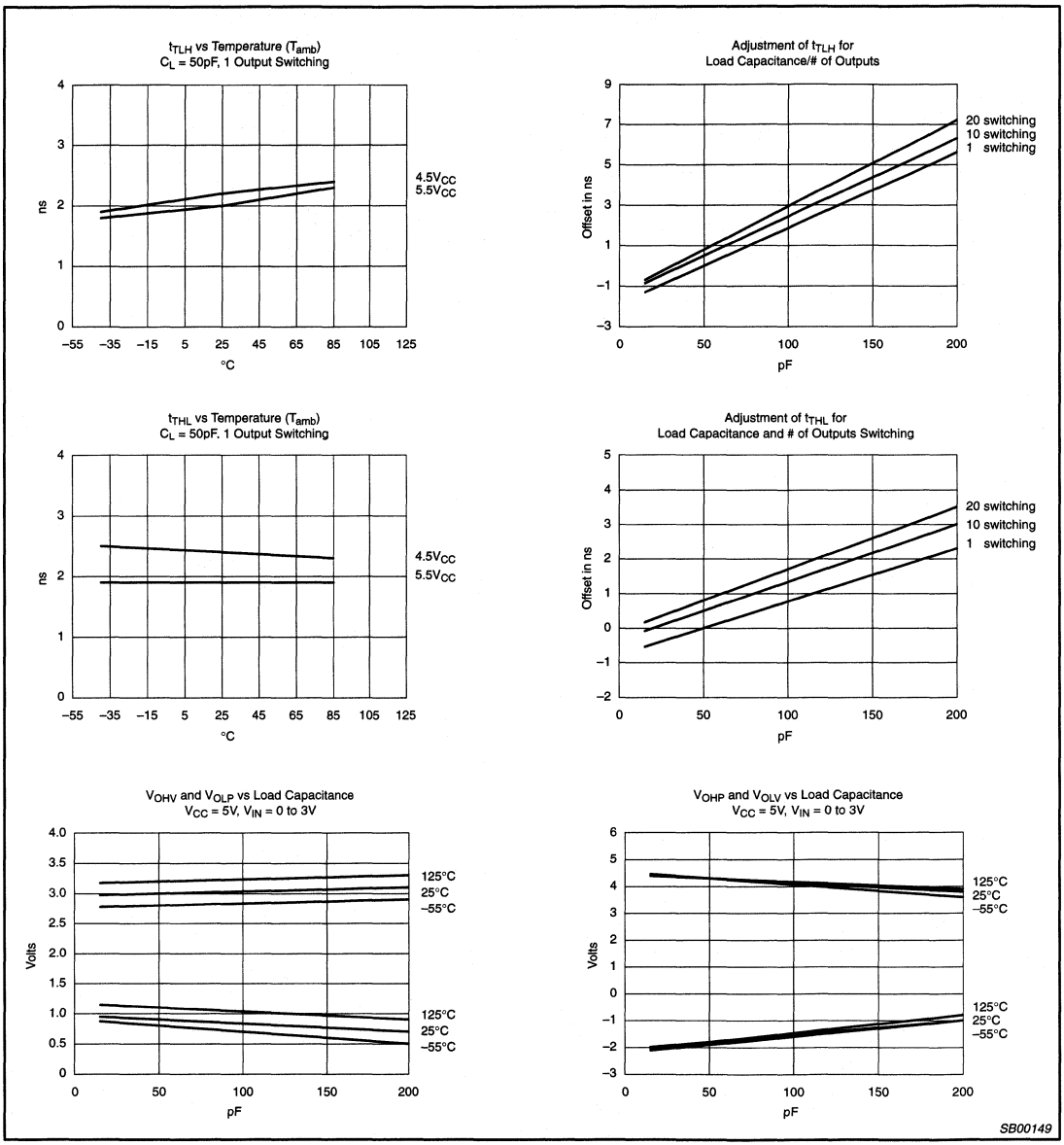


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$ to nQx



SB00147


tPZL vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOE to nQx
ns
°C
MAX
4.5VCC
5.5VCC
MIN
Adjustment of tPZL for
Load Capacitance and # of Outputs Switching
nOE to nQx
Offset in ns
pF
20 switching
10 switching
1 switching
tPHZ vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOE to nQx
Adjustment of tPHZ for
Load Capacitance and # of Outputs Switching
nOE to nQx
tPLZ vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOE to nQx
Adjustment of tPLZ for
Load Capacitance and # of Outputs Switching
nOE to nQx
SB00148


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{TLH} for
Load Capacitance/# of Outputs
Offset in ns
pF
20 switching
10 switching
1 switching
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
SB00149

18-bit D-type flip-flop with reset and enable (3-State) MB2823

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan–in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The MB2823 dual bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The MB2823 has two 9-bit wide buffered registers with Clock Enable ($n\overline{CE}$) and Master Reset ($n\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the Low-clock transition is transferred to the corresponding flip-flop's Q output.

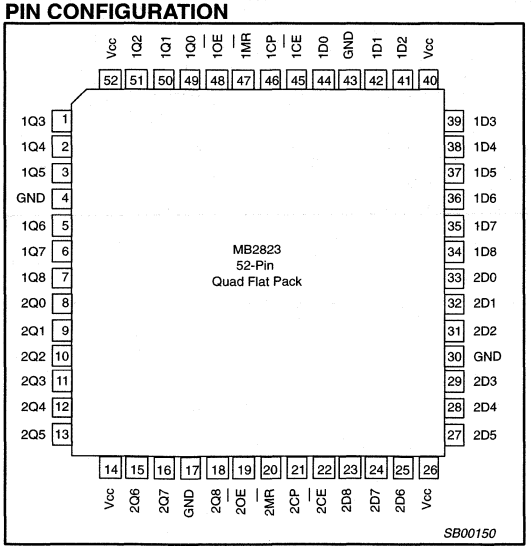
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 5V	3.8 4.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-state	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2823 BB	MB2823 BB	SOT379-1

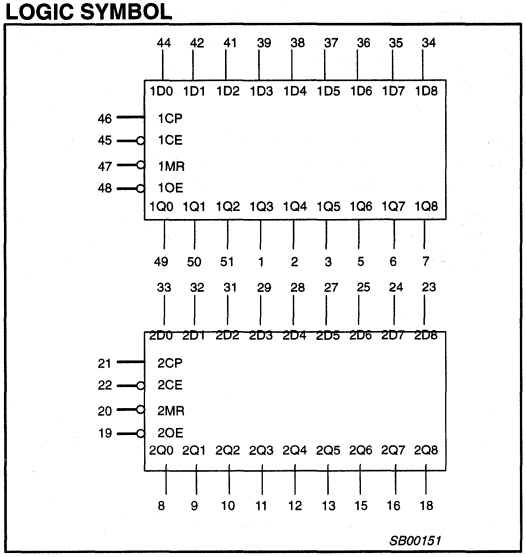
PIN CONFIGURATION



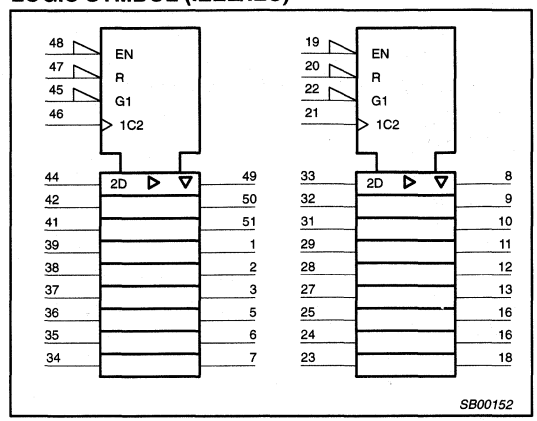
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
48, 19	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active–Low)
44, 42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24, 23	1D0-1D8 2D0-2D8	Data inputs
49, 50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 18	1Q0-1Q8 2Q0-2Q8	Data outputs
46, 21	1CP, 2CP	Clock pulse input (active rising edge)
45, 22	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active–Low)
47, 20	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active–Low)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

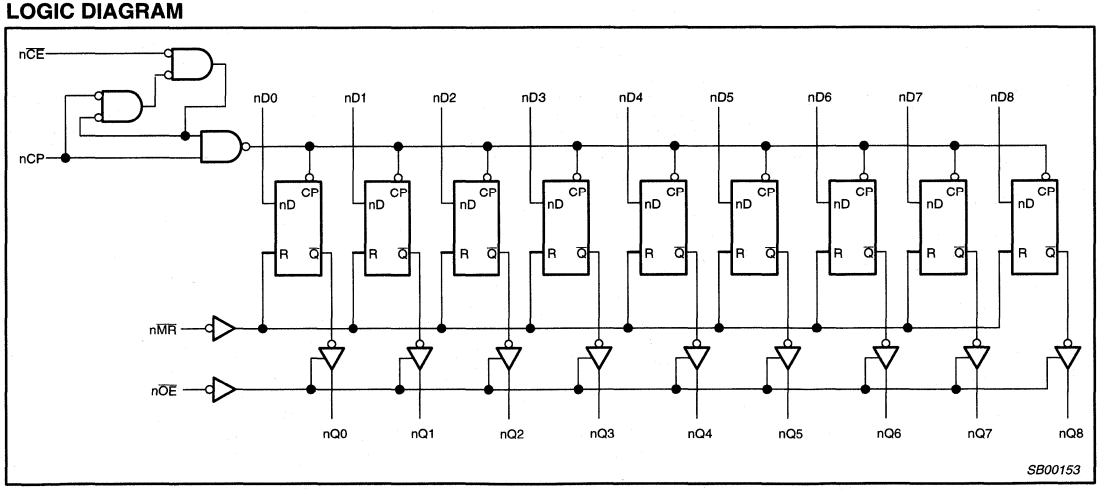
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$n\overline{OE}$	$n\overline{MR}$	$n\overline{CE}$	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_{OL} = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}, V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		45	68		68	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	140	190		140		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	2.0 2.5	3.8 4.2	5.1 5.6	2.0 2.5	5.7 6.1	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQx	2	3.2	5.3	6.6	3.2	7.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.3 2.2	3.2 4.0	4.4 5.3	1.3 2.2	5.1 5.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.3 1.5	3.3 3.1	4.6 4.4	1.3 1.5	5.1 5.9	ns

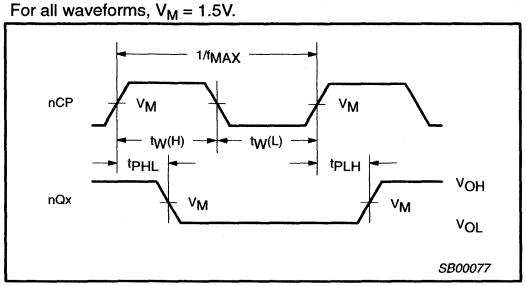
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

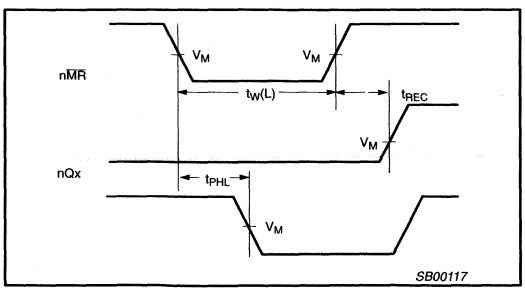
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nCP	3	2.0 1.5	0.6 0.2	2.0 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	3	1.5 1.5	–0.2 –0.5	1.5 1.5	
$t_w(H)$ $t_w(L)$	nCP pulse width High or Low	1	3.0 3.5	1.0 2.3	3.0 3.5	ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low n$\overline{CE}$ to nCP	3	1.5 2.0	–0.2 1.0	1.5 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low n$\overline{CE}$ to nCP	3	1.5 1.5	–1.2 0.3	1.5 1.5	ns
$t_w(L)$	n$\overline{MR}$ pulse width, Low	2	3.0	1.6	3.0	ns
t_{rec}	Recovery time n$\overline{MR}$ to nCP	2	2.5	0.6	2.5	ns

AC WAVEFORMS

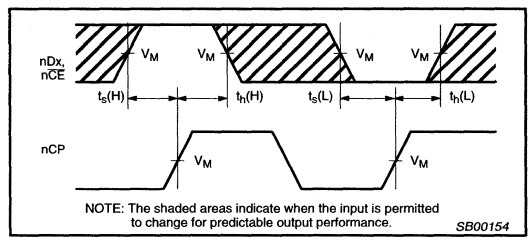
For all waveforms, V_M = 1.5V.



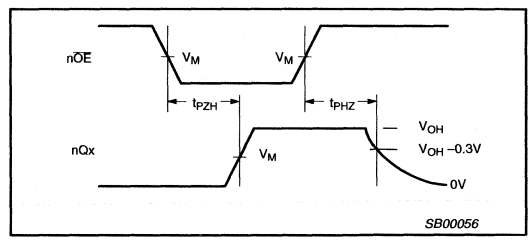
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



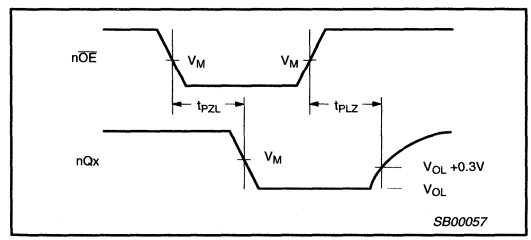
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. Data Setup and Hold Times

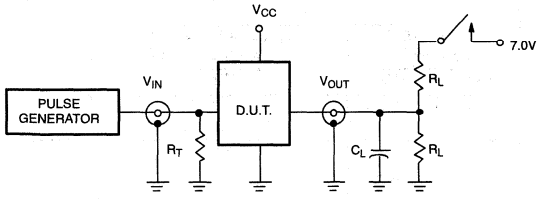


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

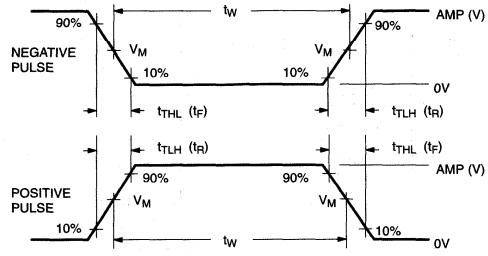


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

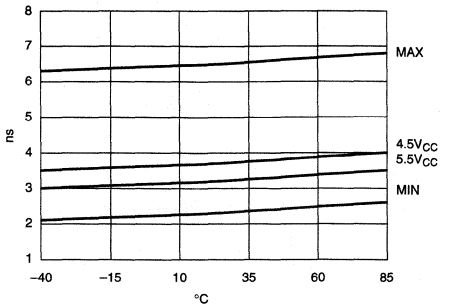
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

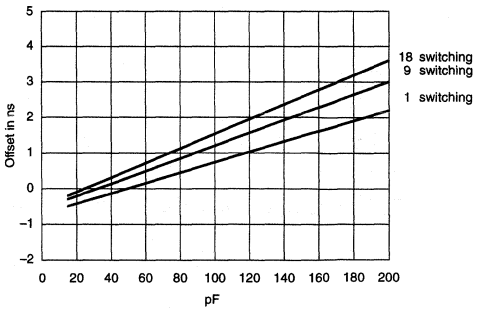
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

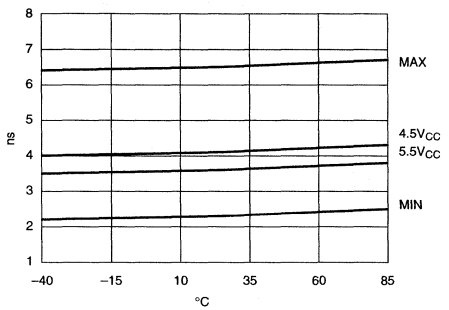
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCp to nQx



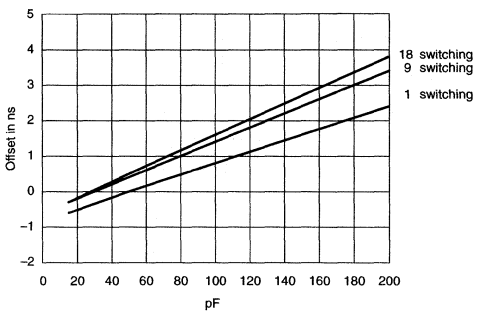
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nCp to nQx



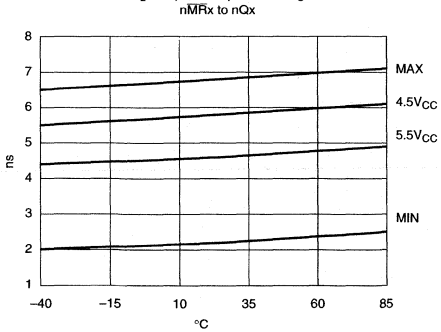
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nCp to nQx



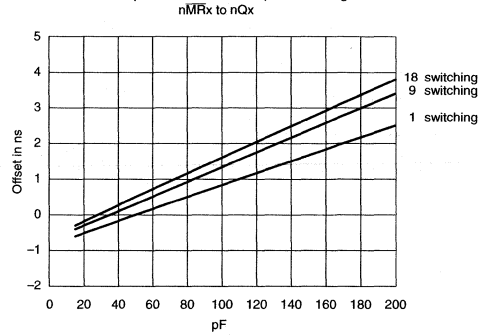
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nCp to nQx



t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{MR}$x to nQx

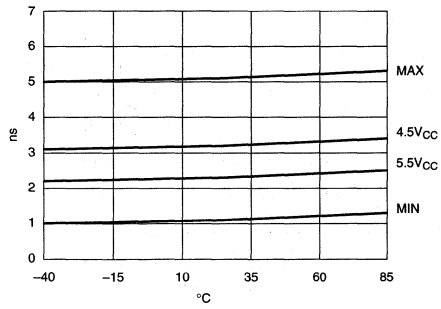


Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
n$\overline{MR}$x to nQx

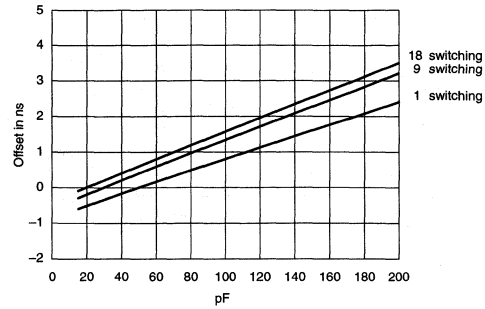


SB00155

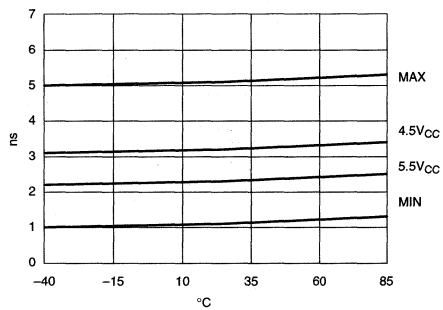
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



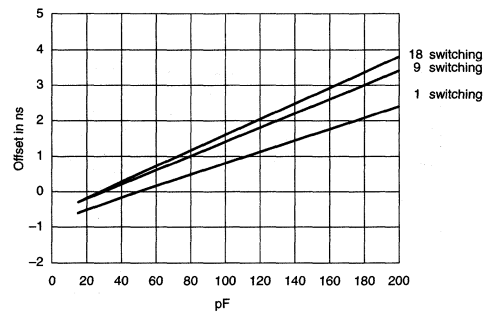
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



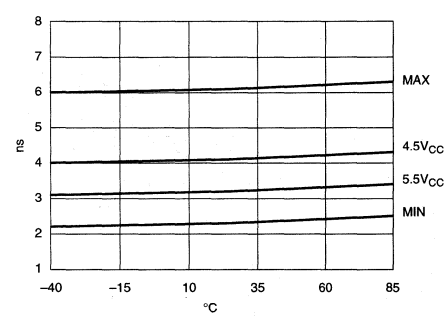
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



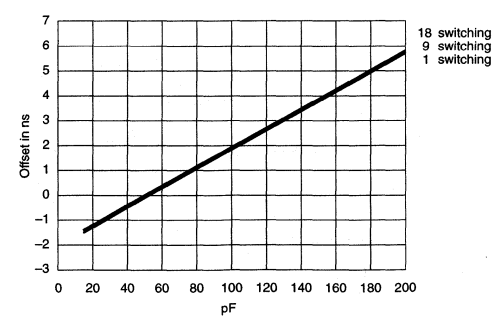
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$x to nQx

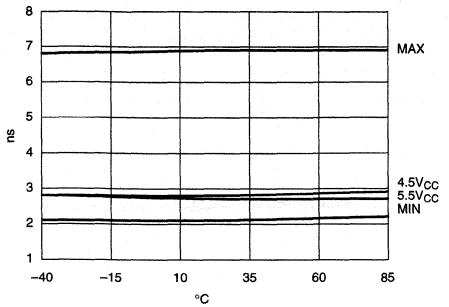


Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$x to nQx

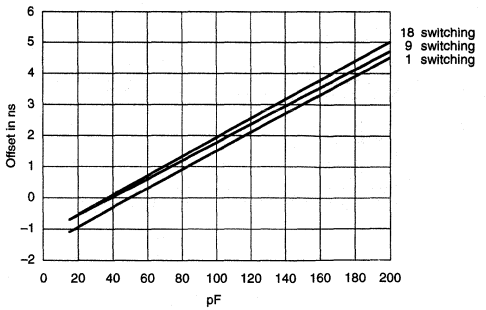


SB00156

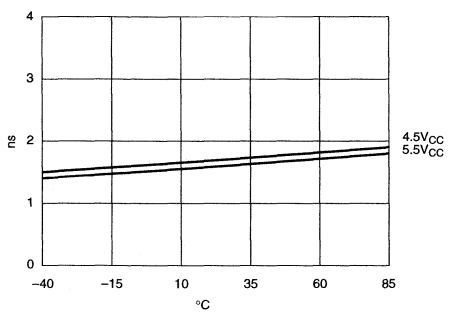
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



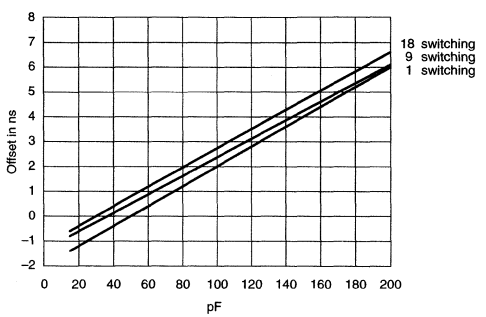
Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



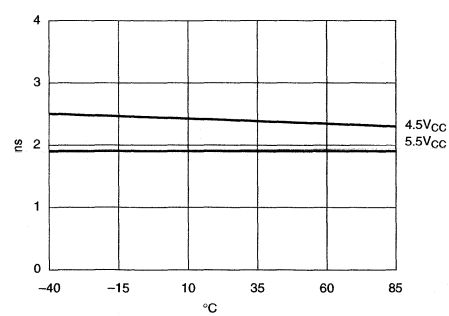
t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



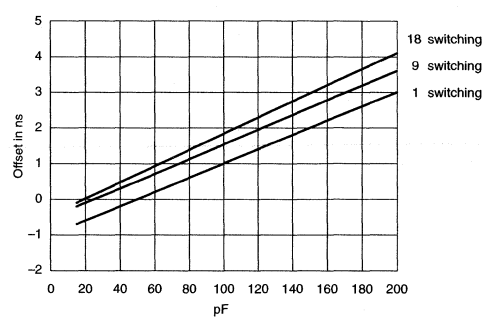
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



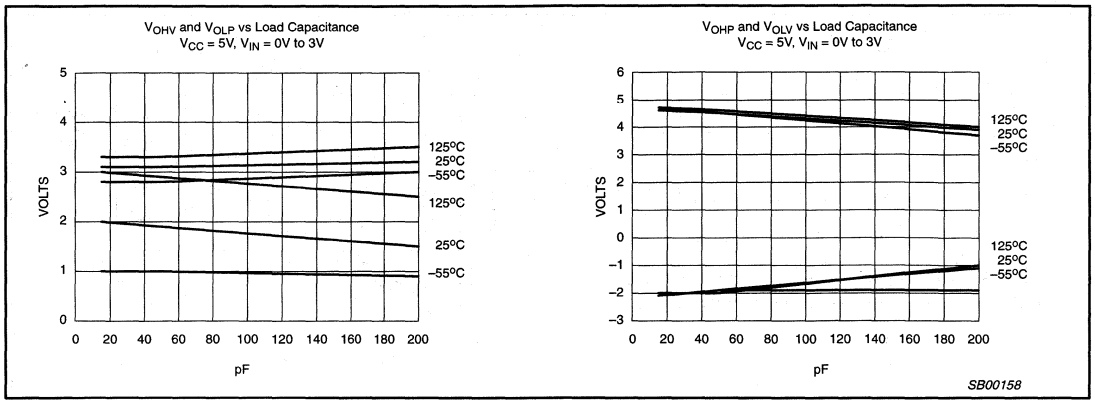
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching



Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching



SB00157


V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0V to 3V
VOLTS
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0V to 3V
VOLTS
pF
125°C
25°C
–55°C
125°C
25°C
–55°C
SB00158

20-bit buffer/line driver, non-inverting (3-State) MB2827

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The MB2827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

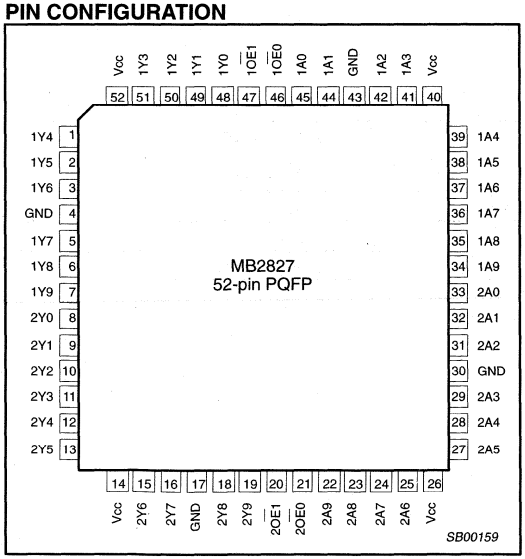
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	2.6 2.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	80	µA

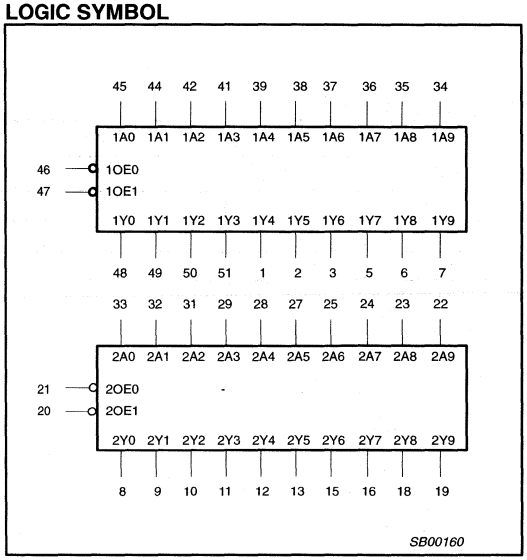
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2827 BB	MB2827 BB	SOT379-1

PIN CONFIGURATION



LOGIC SYMBOL

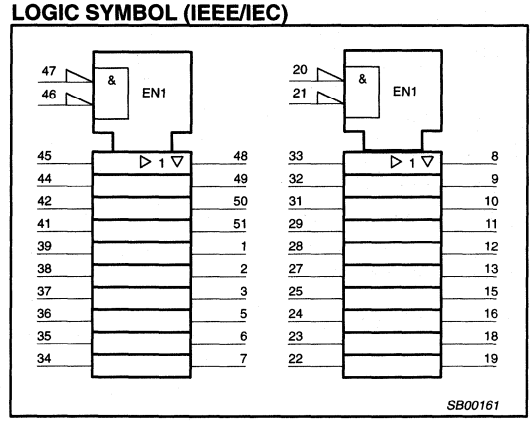


20-bit buffer/line driver, non-inverting (3-State) MB2827

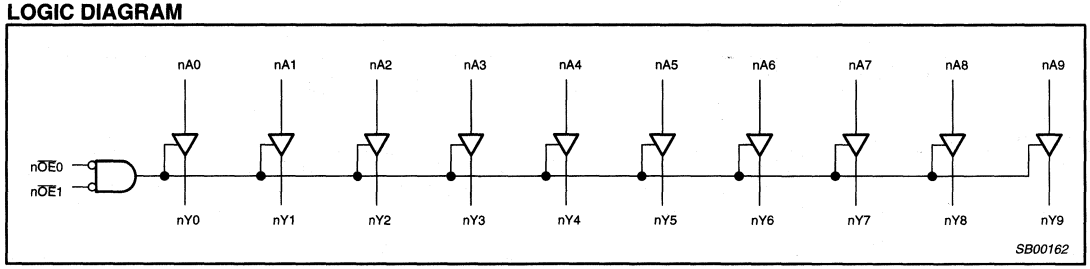
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
45, 44, 42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24, 23, 22	1A0 – 1A9 2A0 – 2A9	Data inputs
48, 49, 50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 18, 19	1Y0 – 1Y9 2Y0 – 2Y9	Data outputs
46, 47, 21, 20	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active–Low)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$n\overline{OE}x$	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O = 4.5V; V_I = 0V or 5.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		80	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		52	76		76	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		80	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

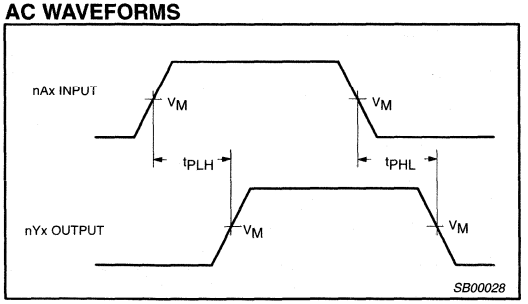
NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

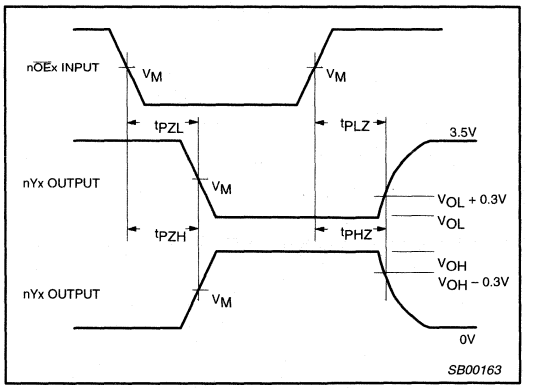
GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.1 1.4	2.6 2.8	3.9 4.1	1.1 1.4	4.1 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.7 2.4	3.5 4.4	4.8 5.6	1.7 2.4	5.6 6.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.9 1.6	3.5 3.2	4.8 4.5	1.9 1.6	5.0 4.9	ns

AC WAVEFORMS

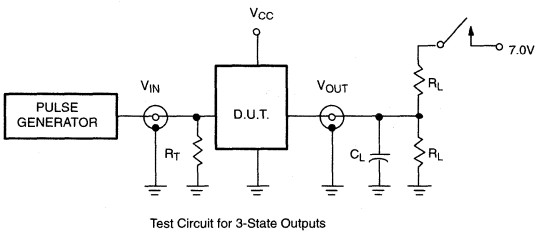


Waveform 1. Waveforms Showing the Input (nAx) to Output (nYx) Propagation Delays

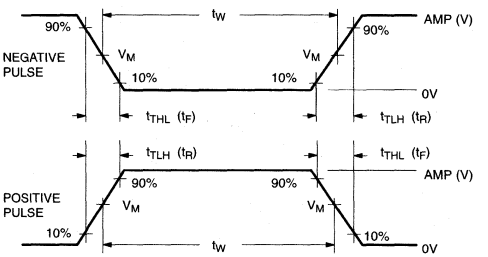


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



VM = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

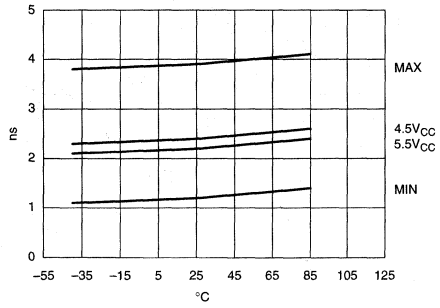
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

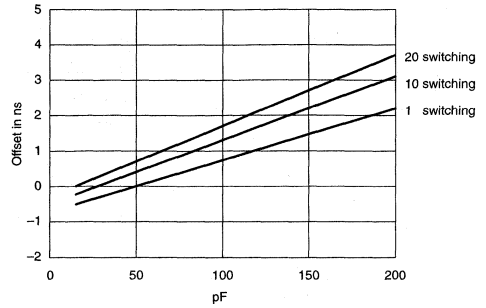
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

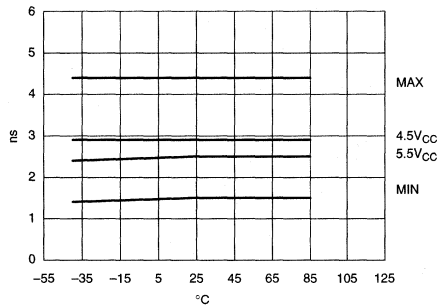
t_{PLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nYx



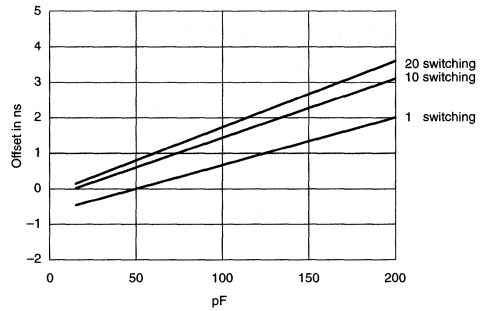
Adjustment of t_{PLH} for
Load Capacitance and # of Outputs Switching
nAx to nYx



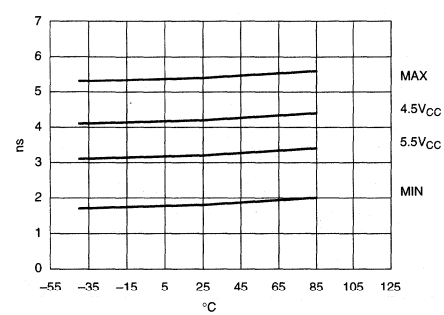
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nAx to nYx



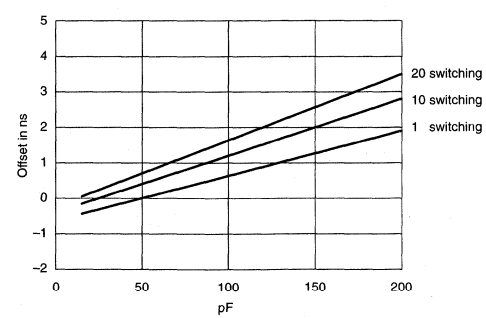
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nAx to nYx



t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$x to nYx

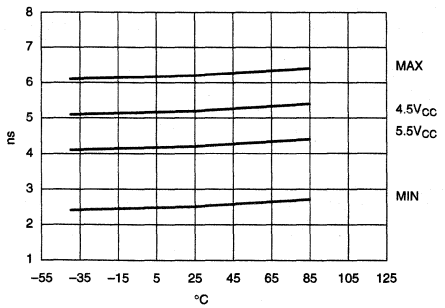


Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$x to nYx

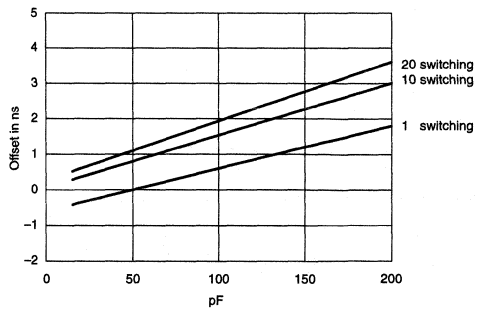


SB00164

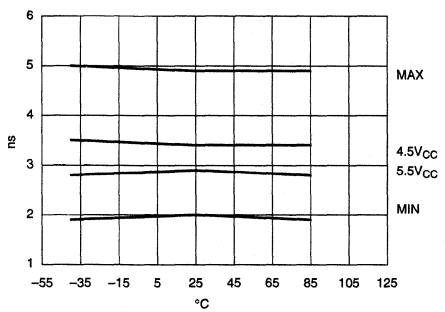
t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$x to nYx



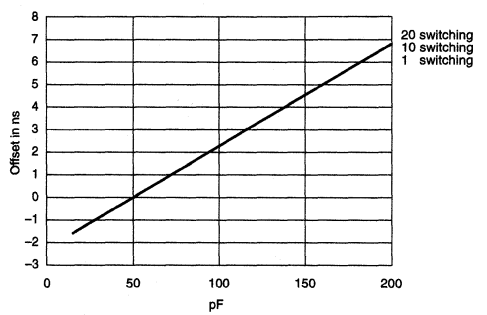
Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$x to nYx



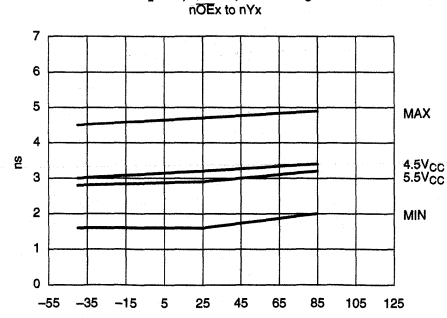
t_{PHZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$x to nYx



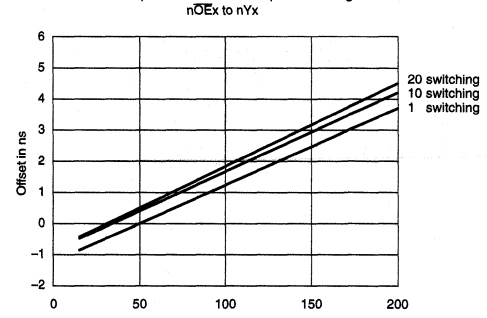
Adjustment of t_{PHZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$x to nYx



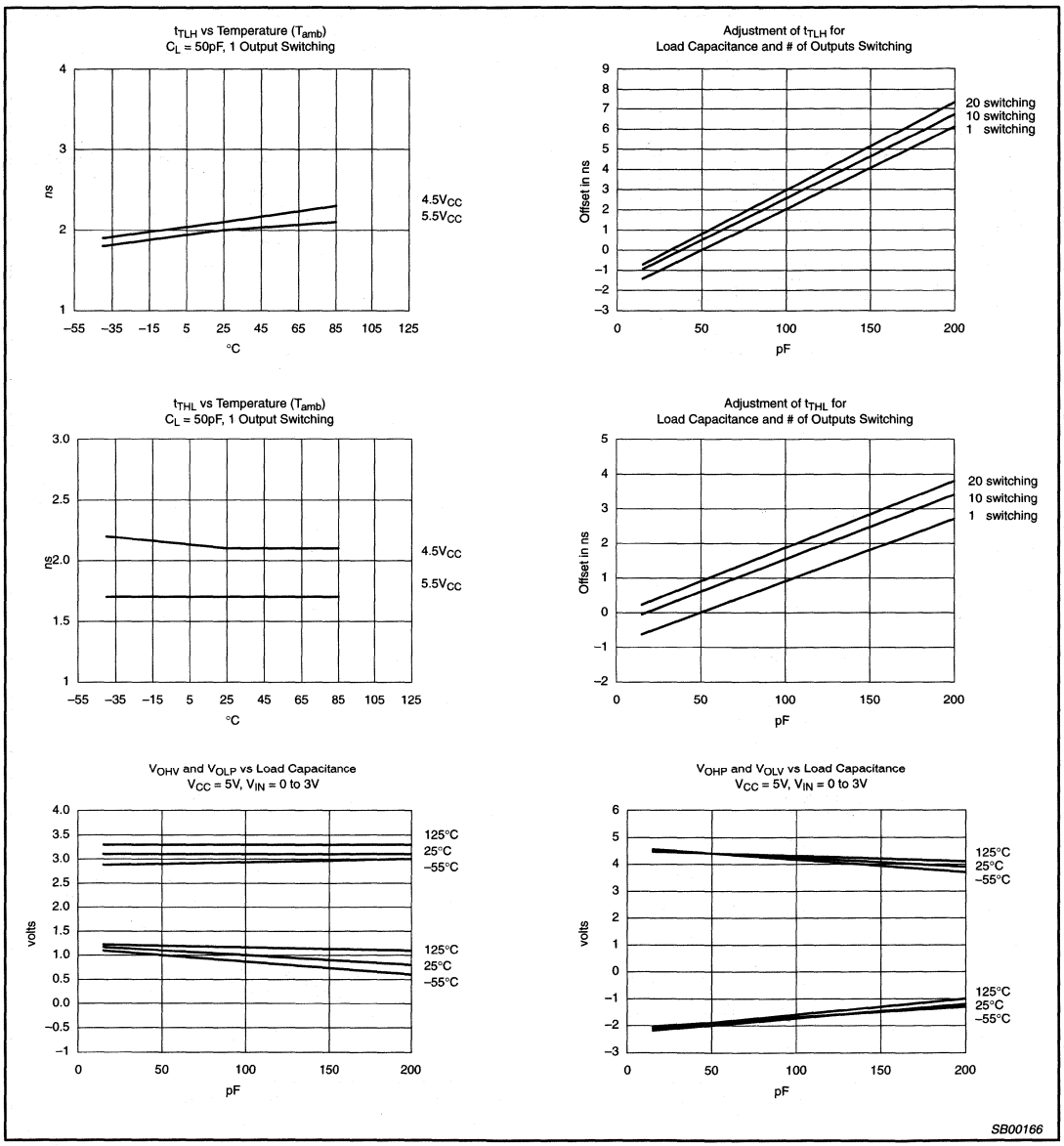
t_{PLZ} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
n$\overline{OE}$x to nYx



Adjustment of t_{PLZ} for
Load Capacitance and # of Outputs Switching
n$\overline{OE}$x to nYx



SB00165


t_{TLH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{TLH} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
20 switching
10 switching
1 switching
t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
volts
125°C
25°C
–55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
SB00166

20-bit bus interface latch (3-State) MB2841

FEATURES

- High speed parallel latches
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2841 Bus interface register is designed to provide extra data width for wider data/address paths of buses carrying parity.

The MB2841 consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($n\overline{OE}$) is Low. When $n\overline{OE}$ is High the output is in the High-impedance state.

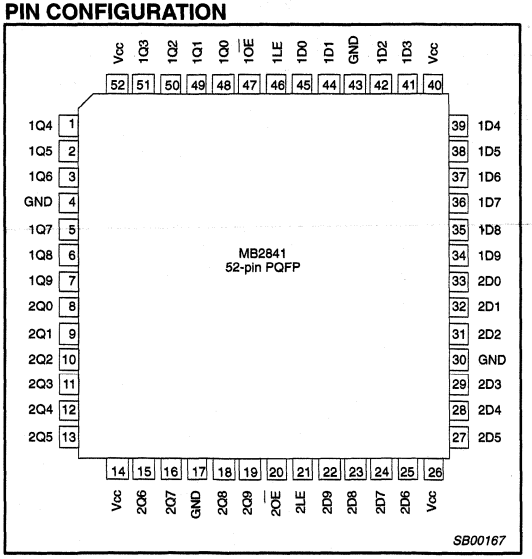
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF; V_{CC} = 5V	3.1 3.5	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5V	120	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2841 BB	MB2841 BB	SOT379-1

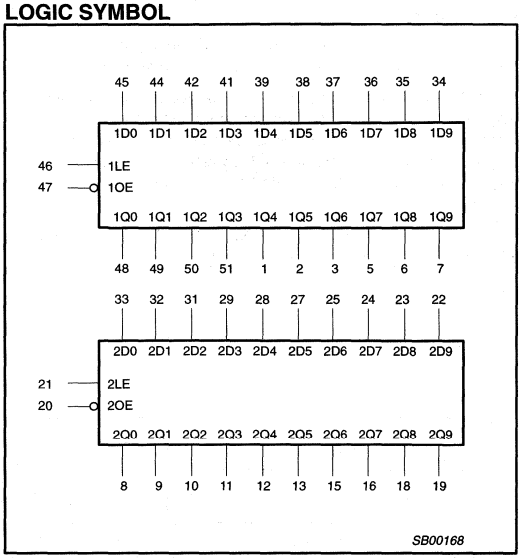
PIN CONFIGURATION



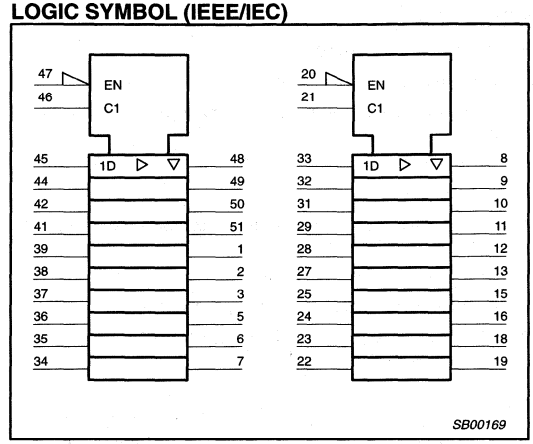
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
45, 44, 42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24, 23, 22	1D0 – 1D9 2D0 – 2D9	Data inputs
48, 49, 50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 18, 19	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
47, 20	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
46, 21	1LE, 2LE	Latch enable inputs (active rising edge)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

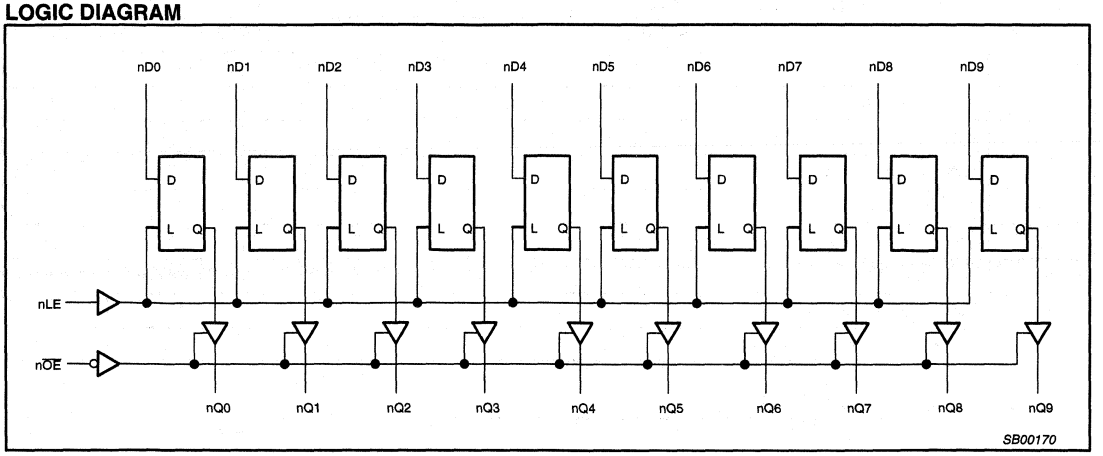


FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$n\overline{OE}$	nLE	nDx	nQ0 – nQ9	
L L	H H	L H	L H	Transparent
L L	↓ ↓	l h	L H	Latched
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
↓ = High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		120	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		56	76		76	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		120	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.5 1.7	3.1 3.5	4.4 4.7	1.5 1.7	5.0 5.3	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	2.4 2.9	4.2 4.6	5.7 6.0	2.4 2.9	6.5 6.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.3 2.3	3.1 4.0	4.2 5.2	1.3 2.3	4.9 5.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.0 1.5	3.3 3.2	4.6 4.5	1.0 1.5	5.1 5.0	ns

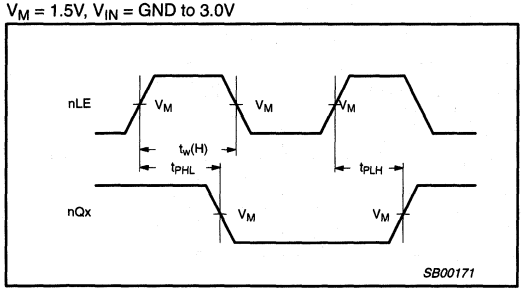
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

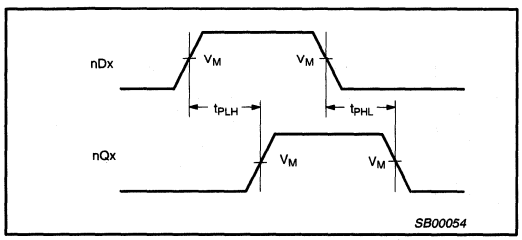
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low nDx to nLE	3	2.0 1.5	0.8 0.4		2.0 1.5		ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nLE	3	0.5 0.5	–0.3 –0.7		0.5 0.5		ns
t_w(H)	nLE pulse width High	1	2.9	1.9		2.9		ns

AC WAVEFORMS

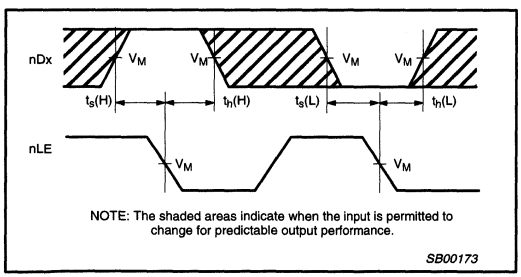
V_M = 1.5V, V_{IN} = GND to 3.0V



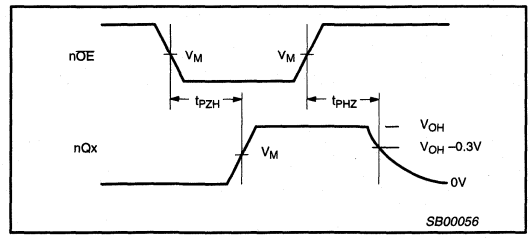
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



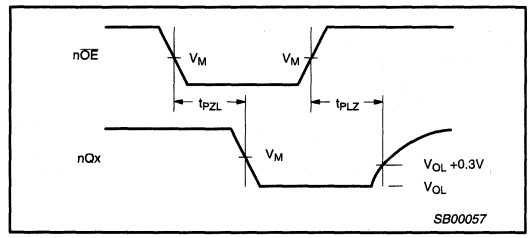
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

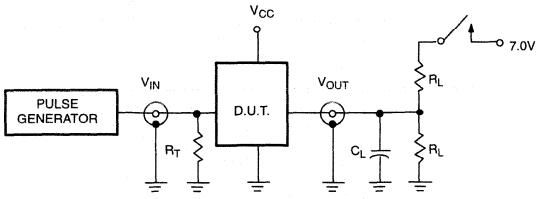


Waveform 4. 3–State Output Enable Time to High Level and Output Disable Time from High Level

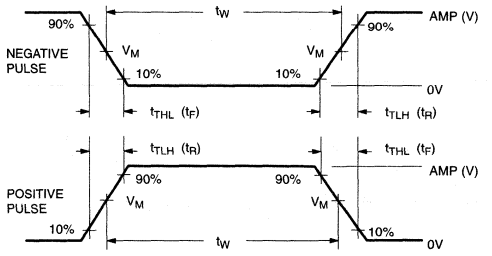


Waveform 5. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

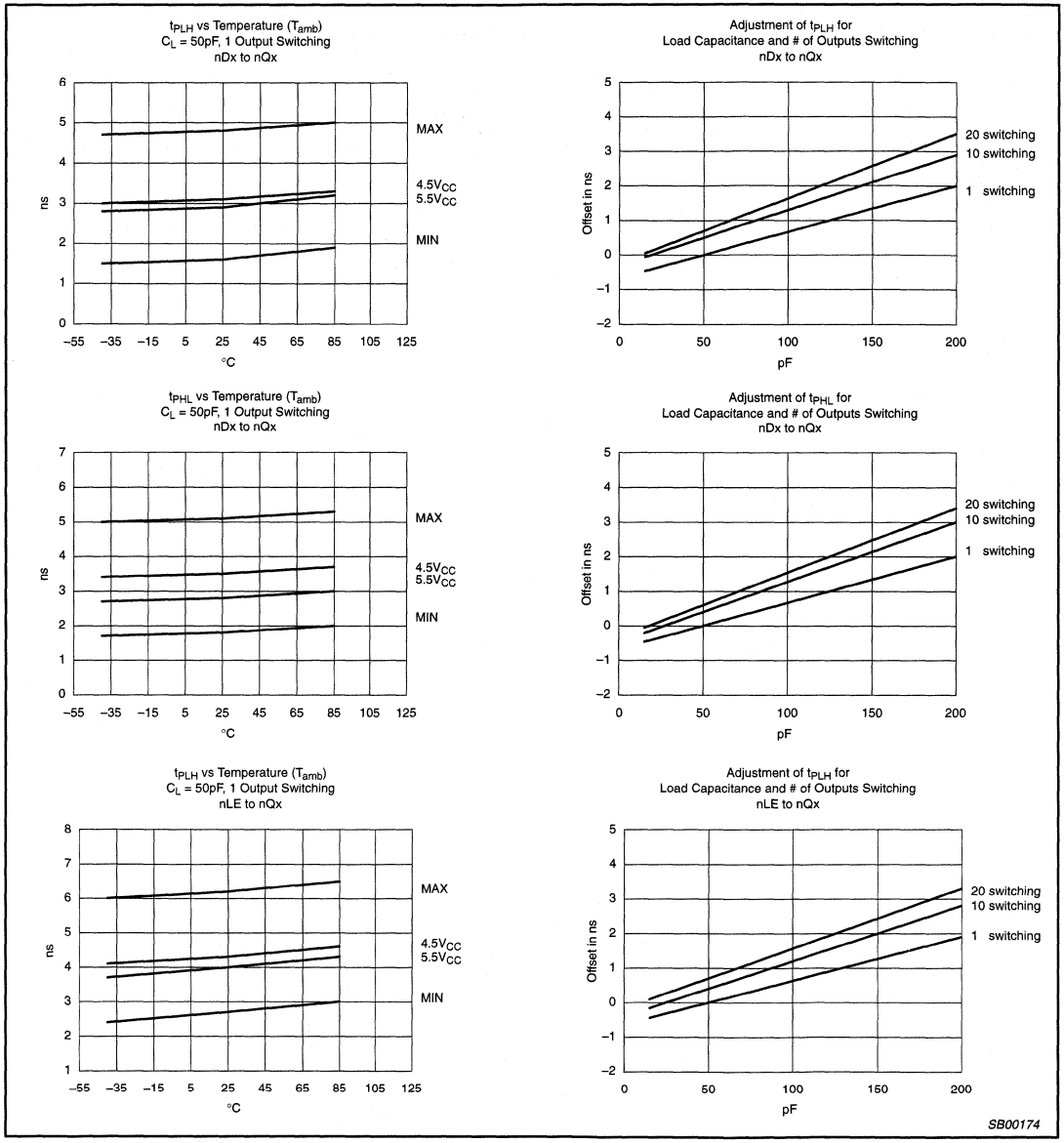
R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

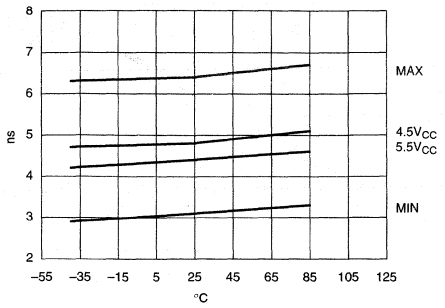
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

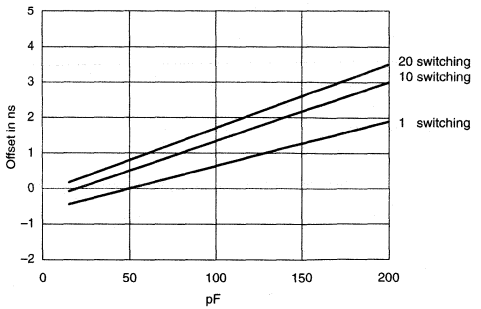
SB00010


tPLH vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nDx to nQx
ns
°C
MAX
4.5VCC
5.5VCC
MIN
Adjustment of tPLH for
Load Capacitance and # of Outputs Switching
nDx to nQx
Offset in ns
pF
20 switching
10 switching
1 switching
tPHL vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nDx to nQx
Adjustment of tPHL for
Load Capacitance and # of Outputs Switching
nDx to nQx
tPLH vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nLE to nQx
Adjustment of tPLH for
Load Capacitance and # of Outputs Switching
nLE to nQx
SB00174

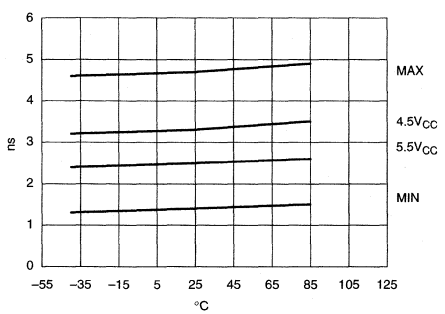
t_{PHL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
nLE to nQx



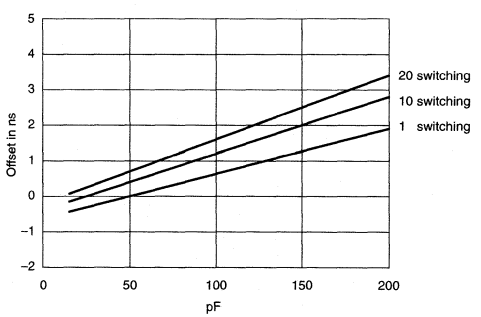
Adjustment of t_{PHL} for
Load Capacitance and # of Outputs Switching
nLE to nQx



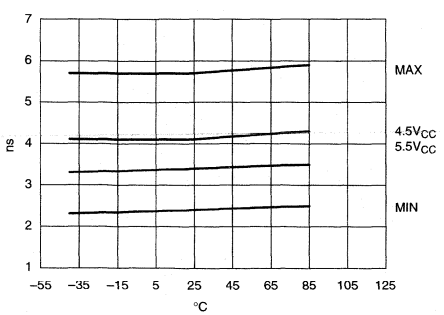
t_{PZH} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



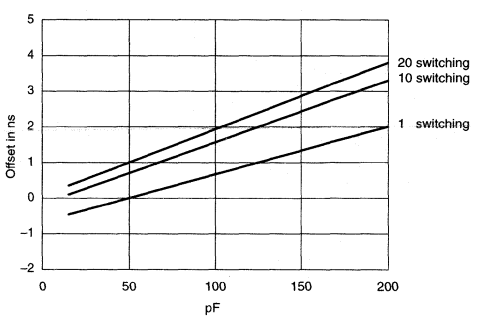
Adjustment of t_{PZH} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



t_{PZL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
$n\overline{OE}$ to nQx



Adjustment of t_{PZL} for
Load Capacitance and # of Outputs Switching
$n\overline{OE}$ to nQx



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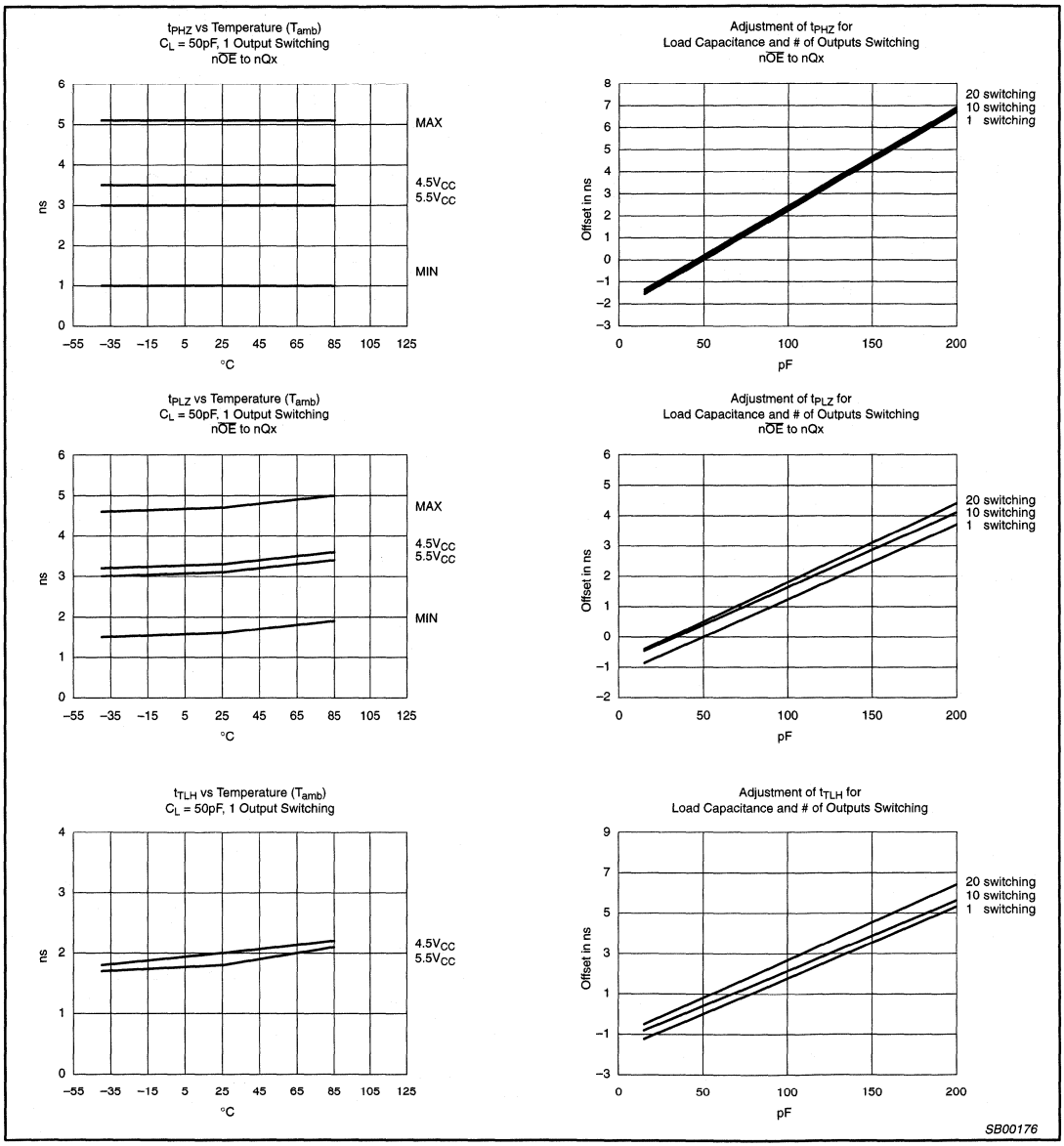
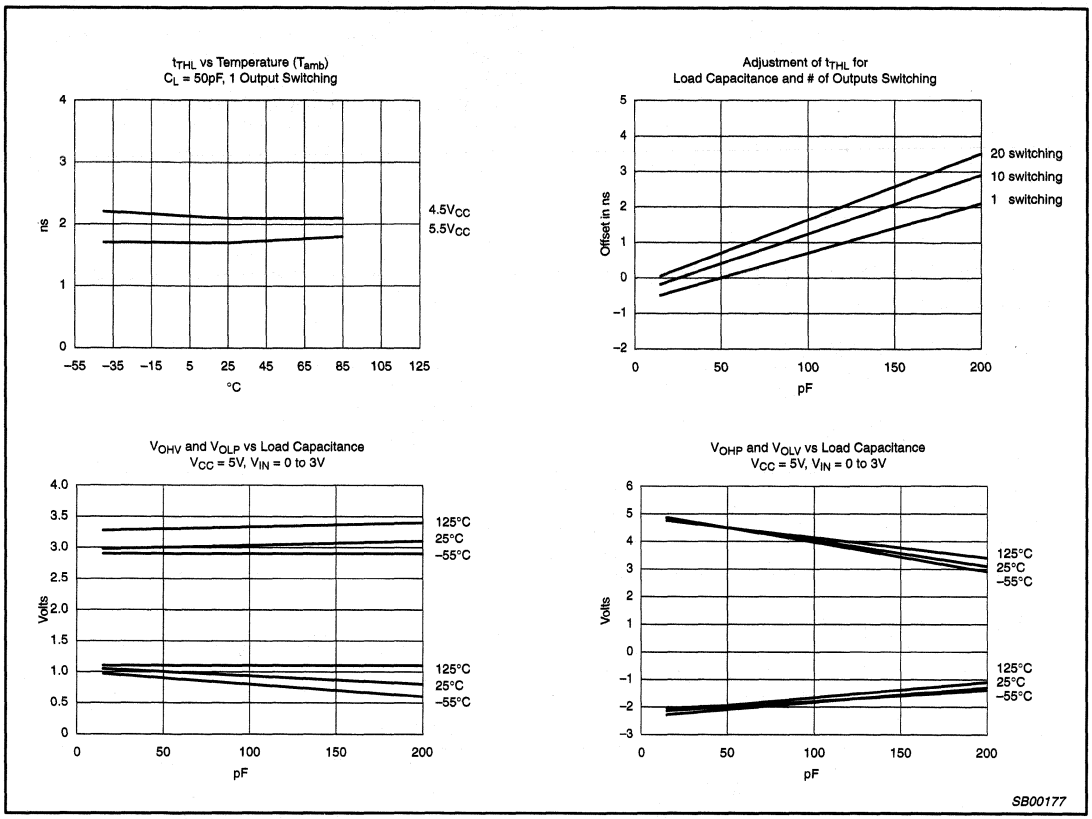

tPHZ vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOE to nQx
ns
°C
MAX
4.5VCC
5.5VCC
MIN
Adjustment of tPHZ for
Load Capacitance and # of Outputs Switching
nOE to nQx
Offset in ns
pF
20 switching
10 switching
1 switching
tPLZ vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
nOE to nQx
Adjustment of tPLZ for
Load Capacitance and # of Outputs Switching
nOE to nQx
tTLH vs Temperature (Tamb)
CL = 50pF, 1 Output Switching
Adjustment of tTLH for
Load Capacitance and # of Outputs Switching
SB00176


t_{THL} vs Temperature (T_{amb})
C_L = 50pF, 1 Output Switching
ns
°C
4.5V_{CC}
5.5V_{CC}
Adjustment of t_{THL} for
Load Capacitance and # of Outputs Switching
Offset in ns
pF
20 switching
10 switching
1 switching
V_{OHV} and V_{OLP} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
−55°C
V_{OHP} and V_{OLV} vs Load Capacitance
V_{CC} = 5V, V_{IN} = 0 to 3V
Volts
pF
125°C
25°C
−55°C
SB00177

20-bit bus transceiver (3-State) MB2861

FEATURES

- Provides high performance bus interface buffering for wide data/address paths or buses carrying parity
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Output capability: +64mA/-32mA
- Power-up 3-State
- Live insertion/extraction permitted
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The MB2861 bus transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity.

The MB2861 20-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

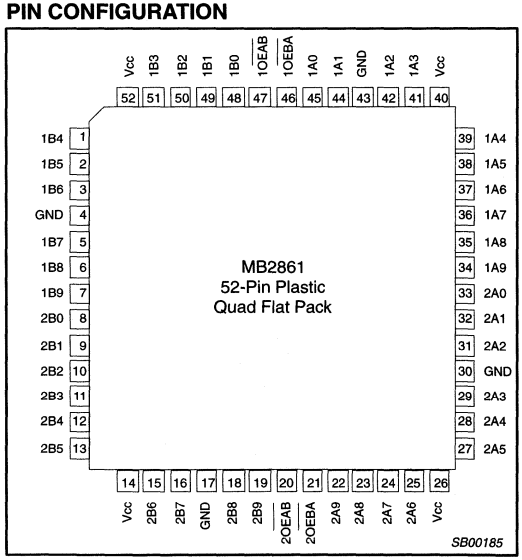
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 5V	2.9 2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	65	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52–pin plastic Quad Flat Pack	–40°C to +85°C	MB2861 BB	MB2861 BB	SOT379-1

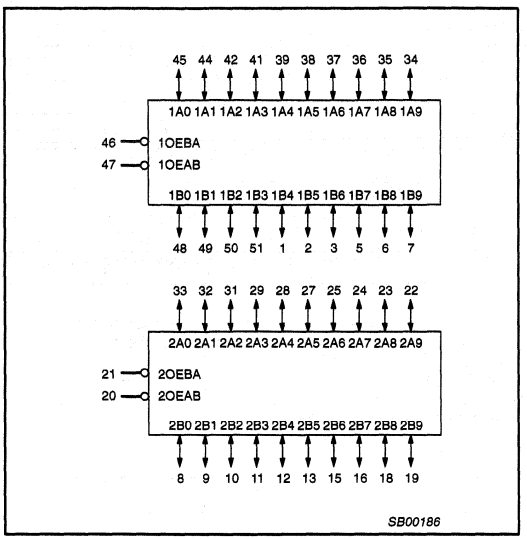
PIN CONFIGURATION



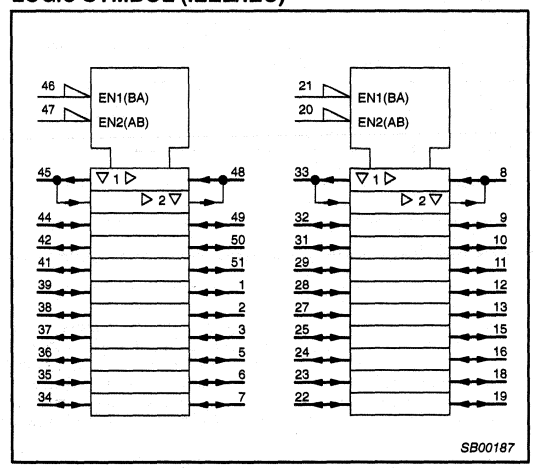
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 20	$1\overline{OEAB}$, $2\overline{OEAB}$	A side to B side output enable inputs (active-Low)
45, 44, 42, 41, 39, 38, 37, 36, 35, 34 33, 32, 31, 29, 28, 27, 25, 24, 23, 22	1A0-1A9, 2A02nA9	Data inputs/outputs (A side)
48, 49, 50, 51, 1, 2, 3, 5, 6, 7 8, 9, 10, 11, 12, 13, 15, 16, 18, 19	1B0-1B9, 2B02nB9	Data outputs/outputs (B side)
46, 21	$1\overline{OEBA}$, $2\overline{OEBA}$	B side to A side output enable inputs (active-Low)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V_{CC}	Positive supply voltage

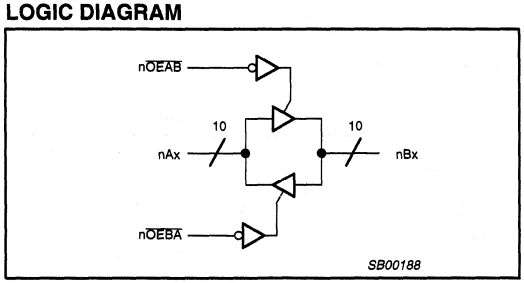
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODE
$\overline{nOEAB}$	$\overline{nOEBA}$	
L	H	A data to B bus
H	L	B data to A bus
H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0V; I_{OH} = −3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5V; I_{OH} = −32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
$I_{PD/PD}$	Power-up/down 3-State output current[3]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		−5.0	−50		−50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	−50	−80	−180	−50	−180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		65	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		45	72		72	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		65	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1 to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

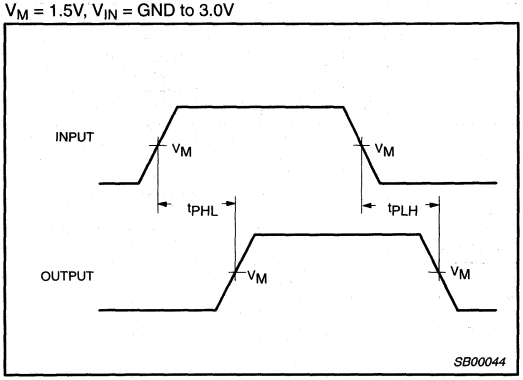
AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

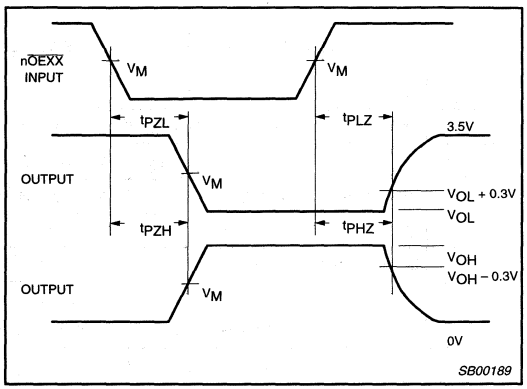
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.4 1.5	2.9 2.9	4.1 4.1	1.4 1.5	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 2.0	3.0 3.6	3.9 4.8	1.5 2.0	4.6 5.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.2 1.7	3.6 3.1	4.8 4.3	1.2 1.7	5.3 4.8	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

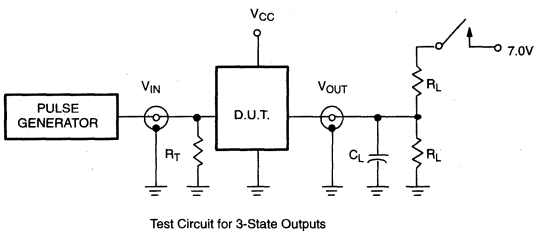


Waveform 1. Input to Output Propagation Delays

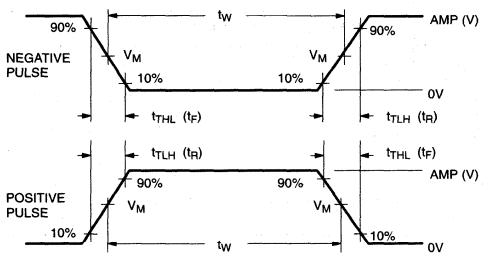


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

Section 3
3.3V Devices
LVT, LVT16

BiCMOS Bus Interface Logic

CONTENTS

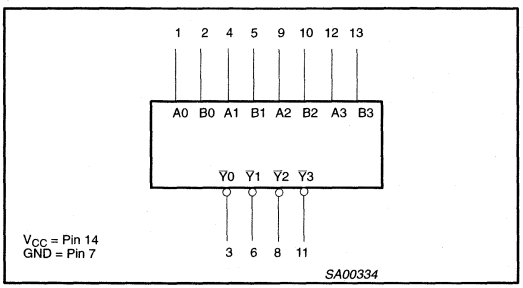
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 3.3V	2.7 2.7	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CCL}	Total supply current	Outputs Low; V_{CC} = 3.6V	1	mA

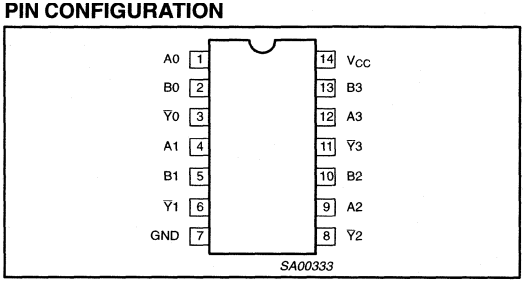
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT00 D	74LVT00 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT00 DB	74LVT00 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT00 PW	74LVT00PW DH	SOT402-1

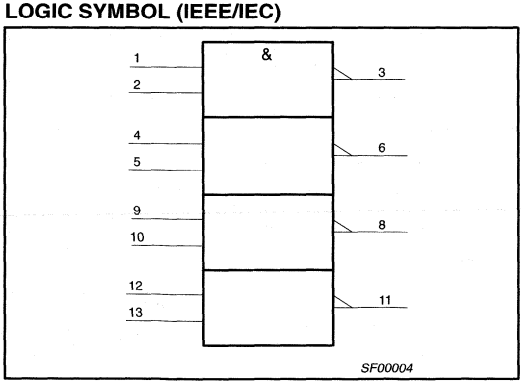
LOGIC SYMBOL



PIN CONFIGURATION



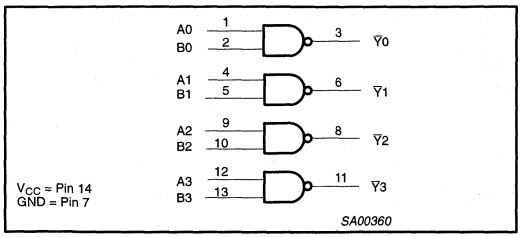
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An-Bn	Data inputs
3, 6, 8, 11	$\overline{Y}n$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}$n
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		1	2	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		3		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

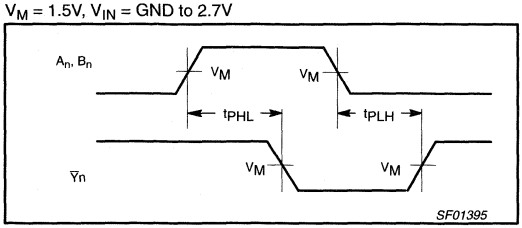
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}$n	1	1.0 1.0	2.7 2.7	4.1 3.9	5.0 3.8	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

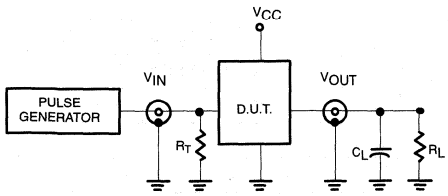
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

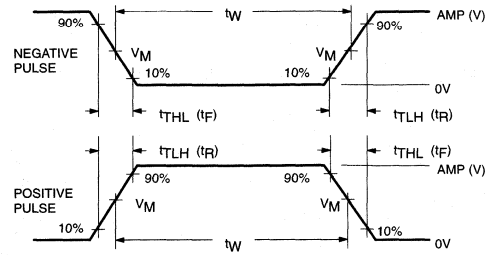


Waveform 1. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00022

3.3V Quad 2-input NOR gate | 74LVT02

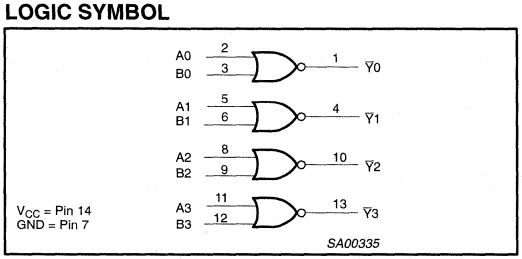
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 3.3V	2.8 2.6	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CCL}	Total supply current	Outputs Low; V_{CC} = 3.6V	1	mA

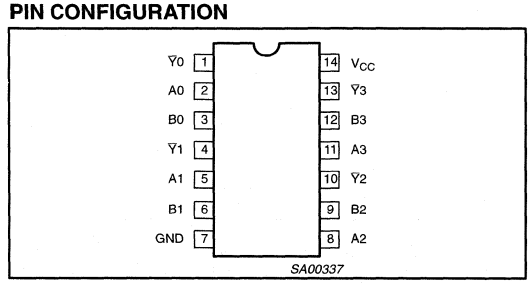
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT02 D	74LVT02 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT02 DB	74LVT02 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT02 PW	74LVT02PW DH	SOT402-1

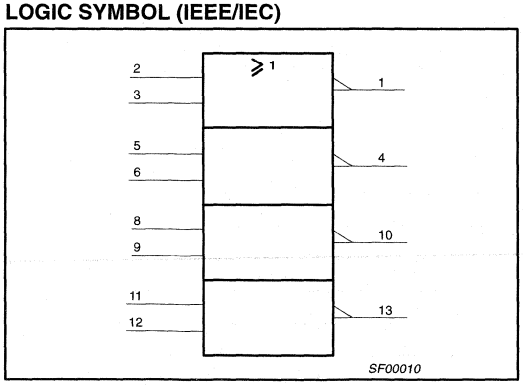
LOGIC SYMBOL



PIN CONFIGURATION



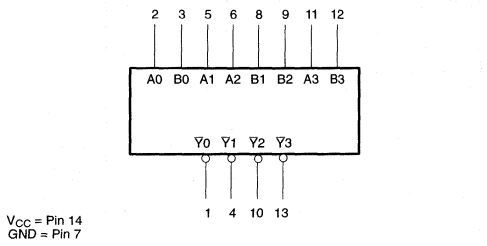
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 5, 6, 8, 9, 11, 12	An-Bn	Data inputs
1, 4, 10, 13	$\overline{Y}$n	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
Dna	**Dnb**	**$\overline{Qn}$**
L	L	H
L	H	L
H	L	L
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		1	2	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		3		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

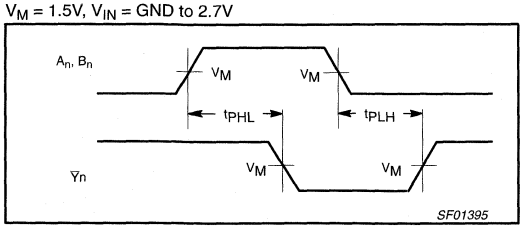
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}$n	1	1.0 1.0	2.8 2.6	4.4 3.6	5.2 3.4	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

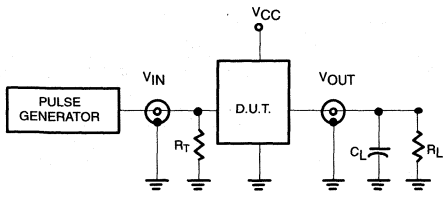
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

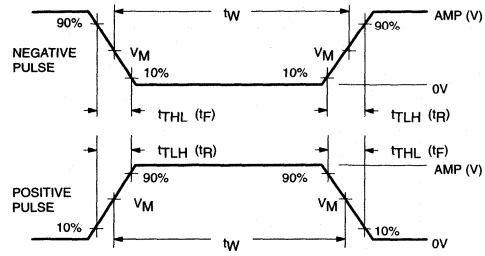


Waveform 1. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

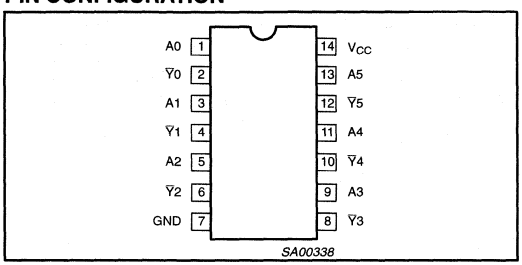
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00022

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}n$	C_L = 50pF; V_{CC} = 3.3V	2.6 2.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CCL}	Total supply current	Outputs Low; V_{CC} = 3.6V	1.5	mA

PIN CONFIGURATION



SA00338

PIN DESCRIPTION

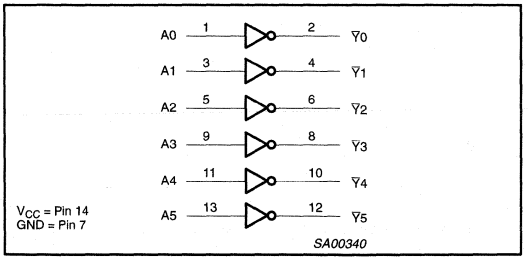
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	An	Data inputs
2, 4, 6, 8, 10, 12	$\overline{Y}n$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS	OUTPUT
An	**$\overline{Y}n$**
L	H
H	L

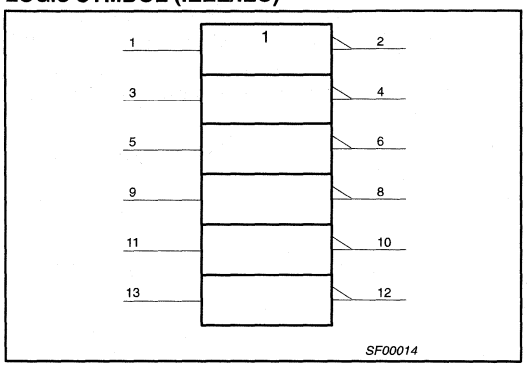
NOTES:
H = High voltage level
L = Low voltage level

LOGIC DIAGRAM



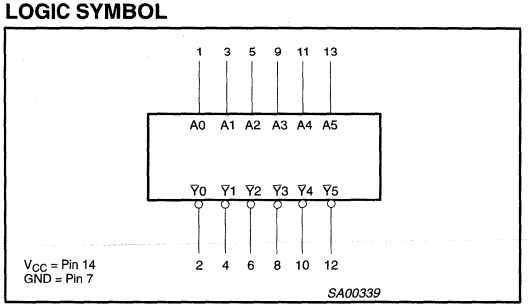
SA00340

LOGIC SYMBOL (IEEE/IEC)



SF00014

LOGIC SYMBOL



SA00339

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT04 D	74LVT04 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT04 DB	74LVT04 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT04 PW	74LVT04PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low–level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		1.5	3	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		3		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

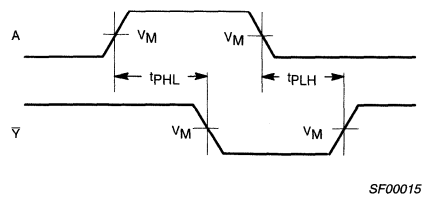
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	1	1.0 1.0	2.6 2.5	3.9 3.5	4.7 3.2	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

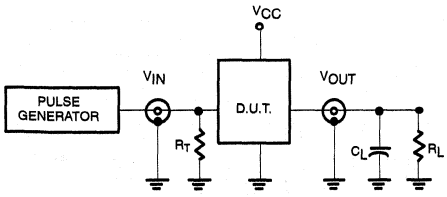
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

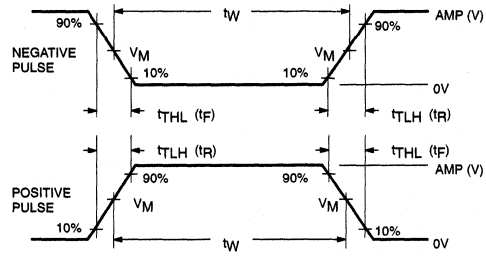


Waveform 1. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00022

3.3V Quad 2-input AND gate 74LVT08

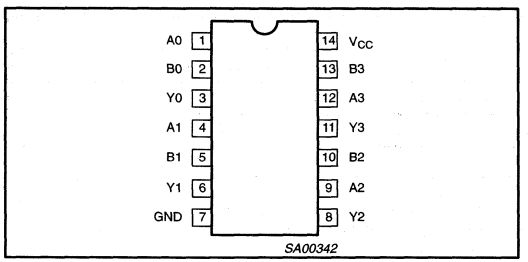
QUICK REFERENCE DATA

SYMBOL	PARAMETER	TEST CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An or Bn to Yn	C_L = 50pF; V_{CC} = 3.3V	3.0 3.4	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
I_{CCL}	Total supply current	Outputs Low; V_{CC} = 3.6V	1	mA

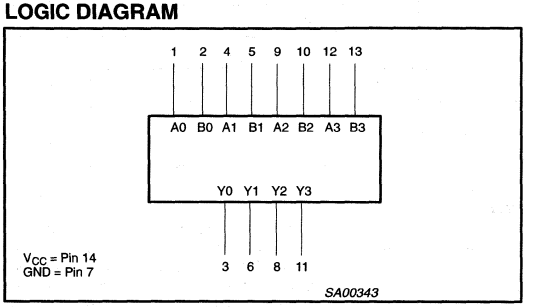
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic SO	–40°C to +85°C	74LVT08 D	74LVT08 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT08 DB	74LVT08 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT08 PW	74LVT08PW DH	SOT402-1

PIN CONFIGURATION



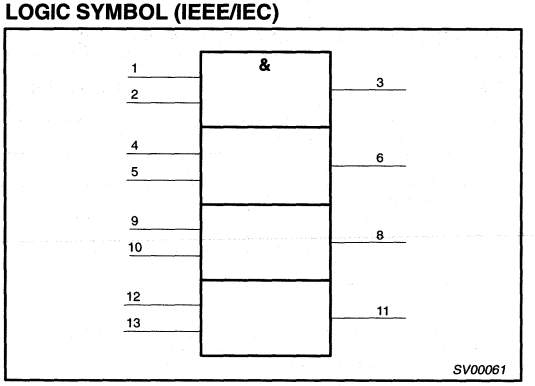
LOGIC DIAGRAM



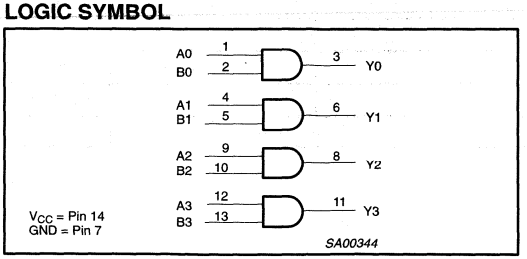
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An-Bn	Data inputs
3, 6, 8, 11	Yn	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:
H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		1	2	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		4		pF
C_O	Output capacitance	V_O = 3V or 0		10		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

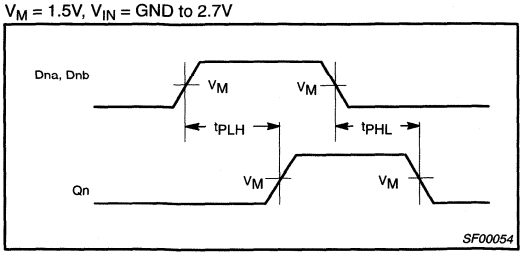
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An or Bn to Yn	1	1.0 1.0	3.0 3.4	3.9 4.6	4.7 4.8	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

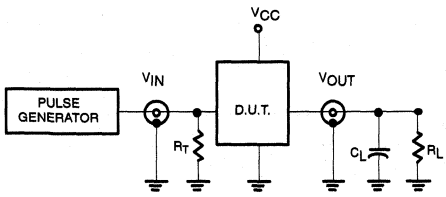
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

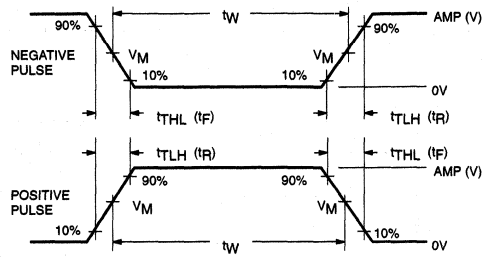


Waveform 1. Propagation Delay for Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

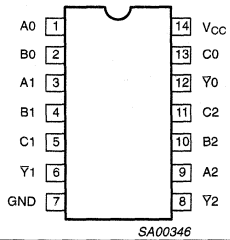
SV00022

3.3V Triple 3-input NAND gate | 74LVT10

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 3.3V	3.8 3.3	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	2	pF
I_{CCL}	Total supply current	Outputs Low; V_{CC} = 3.6V	1	mA

PIN CONFIGURATION

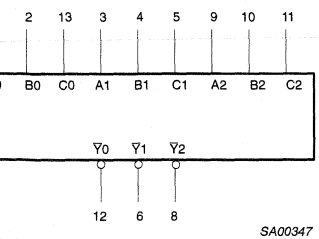


SA00346

PIN DESCRIPTION

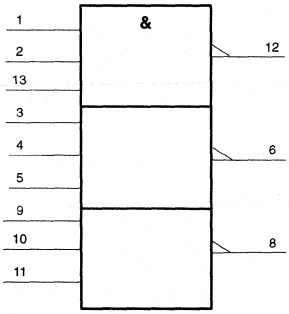
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 9, 10, 11, 13	An, Bn, Cn	Data inputs
6, 8, 12	$\overline{Y}n$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



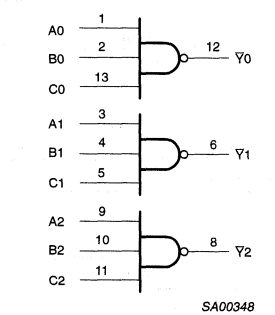
SA00347

LOGIC SYMBOL (IEEE/IEC)



SV00059

LOGIC DIAGRAM



SA00348

FUNCTION TABLE

INPUTS			OUTPUTS
Dna	Dnb	Dnc	$\overline{Q}n$
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT10 D	74LVT10 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT10 DB	74LVT10 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT10 PW	74LVT10PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA		0.05	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA		0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA		0.35	0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V		0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND		0.01	±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V		1	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0		0.001	0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		1	2	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND		0.1	0.2	mA
C_I	Input capacitance	V_I = 3V or 0		2		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

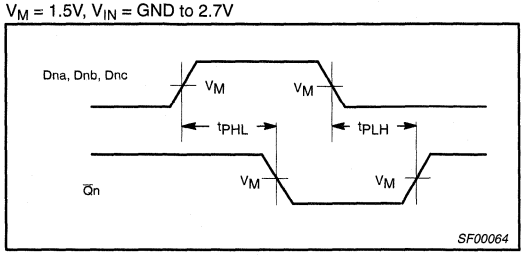
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn to $\overline{Y}$n	1	1.0 1.0	3.8 3.3	5.2 4.4	6.2 4.4	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

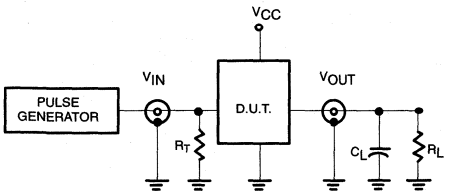
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

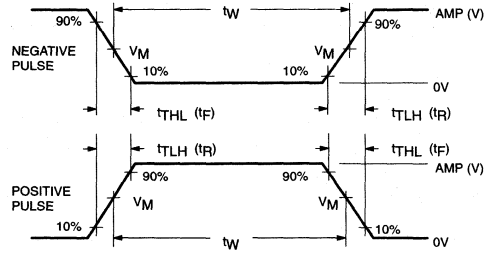


Waveform 1. Propagation Delay for Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00022

3.3V Hex inverter Schmitt trigger | 74LVT14

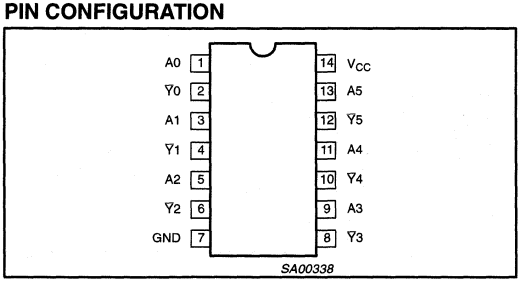
DESCRIPTION

The 74LVT14 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. They are capable of transforming slowly changing input signals into sharply defined, jitter free output signals. In addition, they have greater noise margin than conventional inverters. Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive-going and negative-going input threshold (typically 600mV) is determined internally by resistor ratios and is insensitive to temperature and supply voltage variations.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}n$	C_L = 50pF; V_{CC} = 3.3V	3.2 3.0	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CCL}	Total supply current	Outputs low; V_{CC} = 3.6V	1.5	mA

PIN CONFIGURATION



SA00338

PIN DESCRIPTION

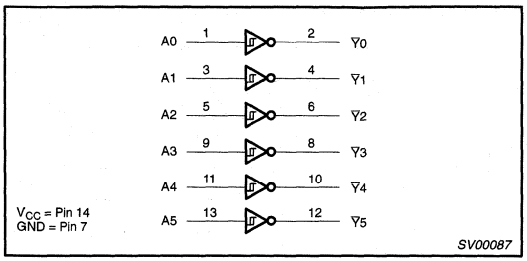
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	An	Data inputs
2, 4, 6, 8, 10, 12	$\overline{Y}$n	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS	OUTPUT
Dn	$\overline{Q}$n
L	H
H	L

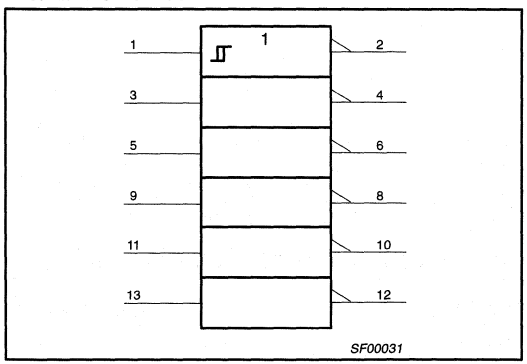
NOTES:
H = High voltage level
L = Low voltage level

LOGIC DIAGRAM



SV00087

IEC/IEEE SYMBOL

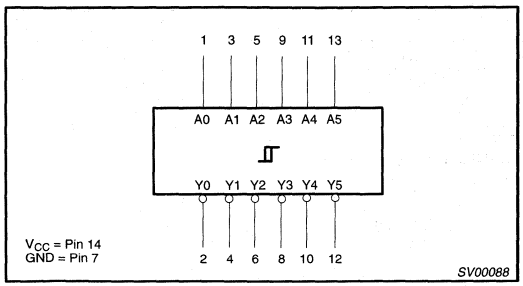


SF00031

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT14 D	74LVT14 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT14 DB	74LVT14 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT14 PW	74LVT14 PWDH	SOT402-1

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{T+}	Positive-going threshold	V_{CC} = 3.3V	1.5	1.7	2.0	V
V_{T-}	Negative-going threshold	V_{CC} = 3.3V	0.9	1.1	1.3	V
ΔV_T	Hysteresis	V_{CC} = 3.3V	0.4	0.6		V
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low–level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		1.5	3	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		3		pF

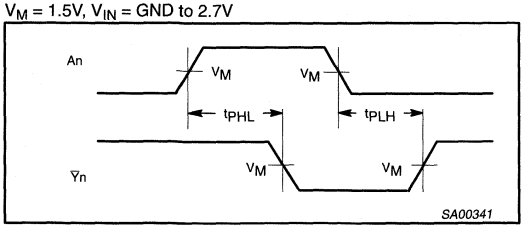
NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	Waveform 1	1.0 1.0	3.8 3.2	5.7 4.5	6.9 4.1	ns

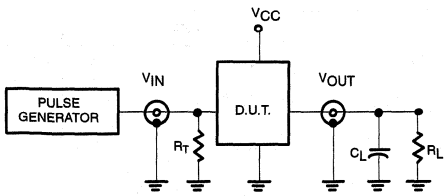
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

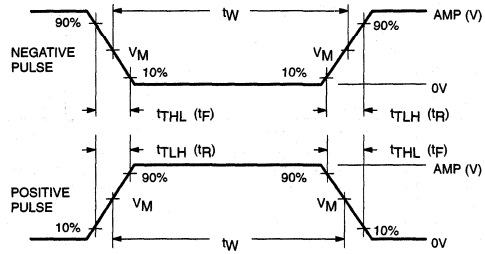


Waveform 1. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

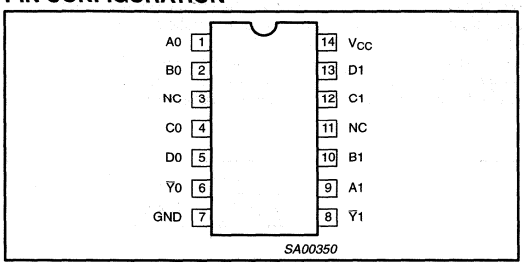
SV00022

3.3V Dual 4-input NAND gate 74LVT20

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn, Dn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 3.3V	3.4 3.2	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CCL}	Total supply current	Outputs Low; V_{CC} = 3.6V	0.5	mA

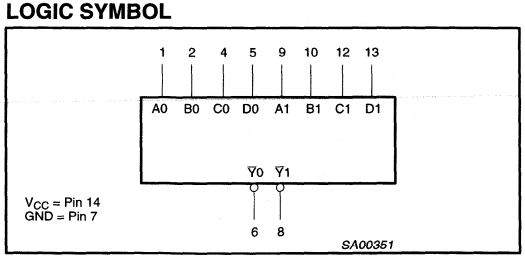
PIN CONFIGURATION



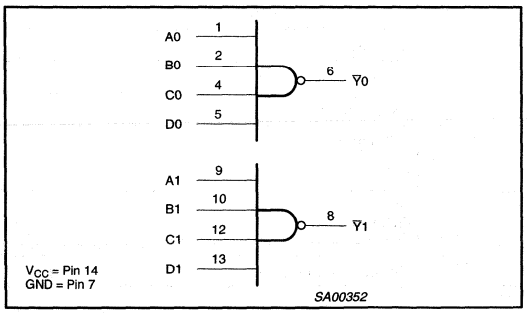
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An, Bn, Cn, Dn	Data inputs
6, 8	$\overline{Y}n$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

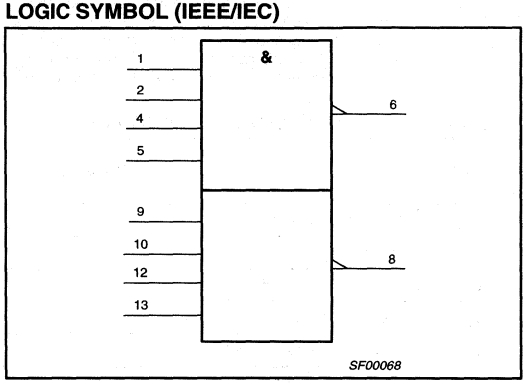
LOGIC SYMBOL



LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUT
Dna	Dnb	Dnc	Dnd	$\overline{Q}n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT20 D	74LVT20 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT20 DB	74LVT20 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT20 PW	74LVT20PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		48	
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		0.5	1.2	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		3		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

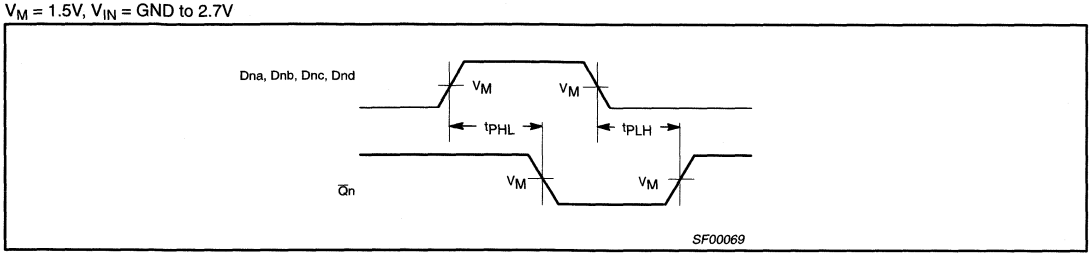
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An, Bn, Cn, Dn to $\overline{Y}$n	1	1.0 1.0	3.4 3.2	5.4 4.4	6.4 4.3	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

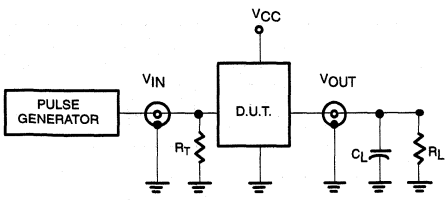
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

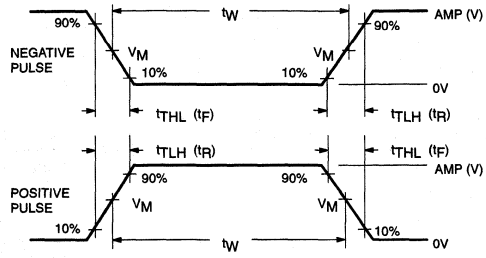


Waveform 1. Propagation Delay for Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

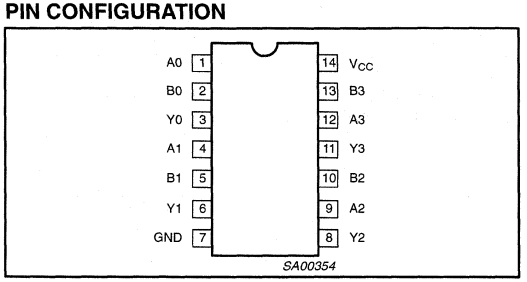
SV00022

3.3V Quad 2-input OR gate | 74LVT32

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An, Bn to Yn	C_L = 50pF; V_{CC} = 3.3V	2.6 3.2	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CCL}	Total supply current	Outputs Low; V_{CC} = 3.6V	1	mA

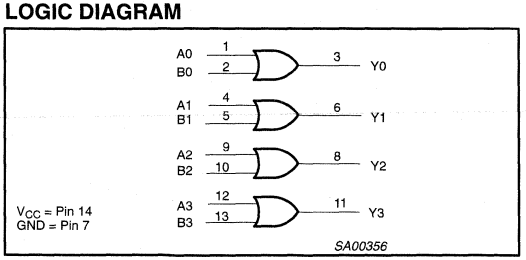
PIN CONFIGURATION



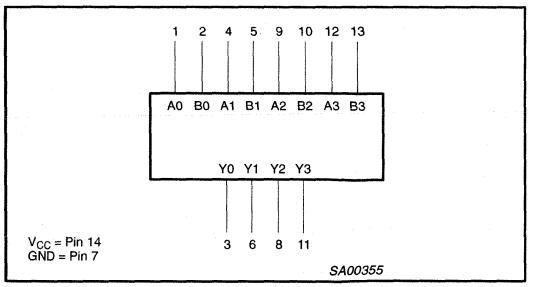
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An, Bn	Data inputs
3, 6, 8, 11	Yn	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

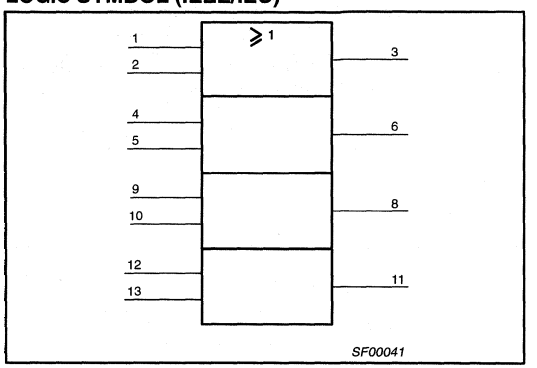
LOGIC DIAGRAM



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	L
L	H	H
H	L	H
H	H	H

NOTES:
H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT32 D	74LVT32 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT32 DB	74LVT32 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT32 PW	74LVT32PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		1	2	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		3		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

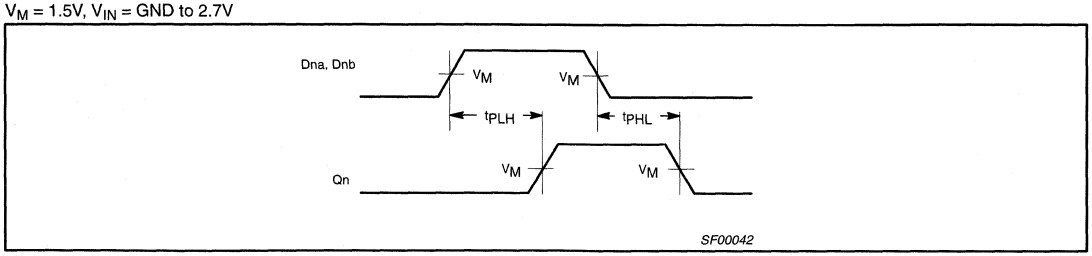
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An, Bn to Yn	1	1.0 1.0	2.6 3.2	3.8 4.6	4.5 4.9	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

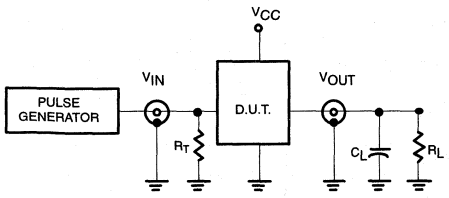
AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

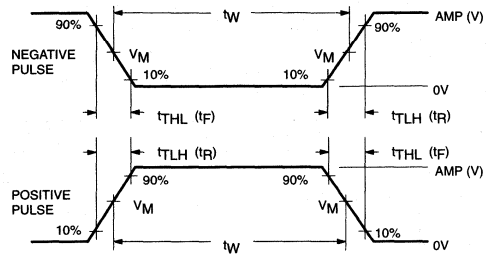


Waveform 1. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

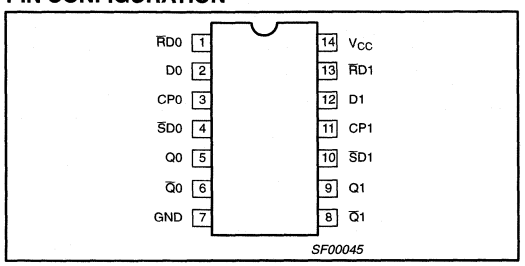
SV00022

3.3V Dual D-type flip-flop | 74LVT74

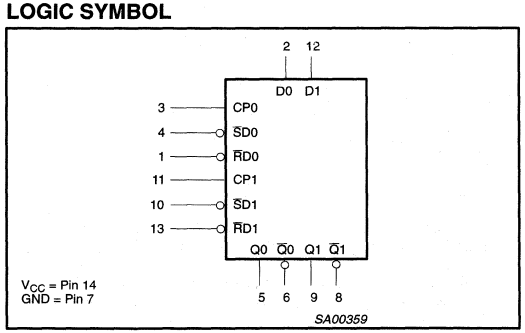
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPn to Qn	C_L = 50pF; V_{CC} = 3.3V	3.1 3.6	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CC}	Total supply current	V_{CC} = 3.6V	0.5	mA

PIN CONFIGURATION



LOGIC SYMBOL



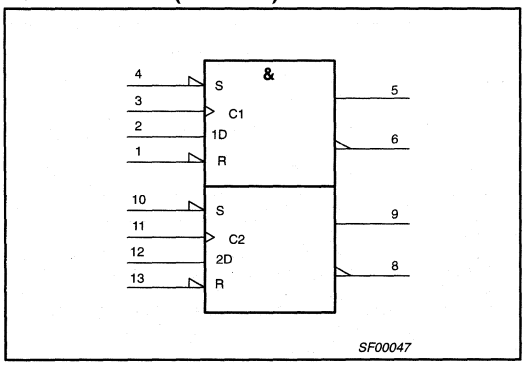
DESCRIPTION

The 74LVT74 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock input. When set and reset are inactive (high), data at the D input is transferred to the Q and $\overline{Q}$ outputs on the low-to-high transition of the clock. Data must be stable just one setup time prior to the low-to-high transition of the clock for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 12	D0, D1	Data inputs
3, 11	CP0, CP1	Clock inputs (active rising edge)
4, 10	$\overline{SD}$0, $\overline{SD}$1	Set inputs (active LOW)
1, 13	$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active LOW)
5, 6, 8, 9	Qn, $\overline{Q}$n	Data outputs

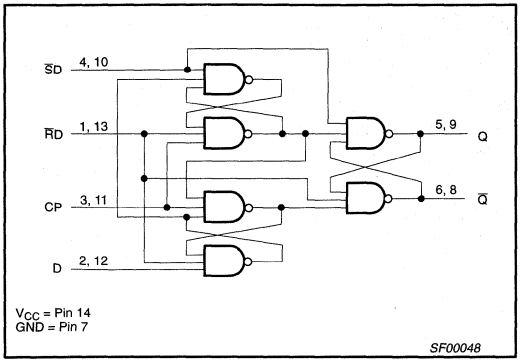
LOGIC SYMBOL (IEEE/IEC)



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT74 D	74LVT74 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT74 DB	74LVT74 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT74 PW	74LVT74PW DH	SOT402-1

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↕	X	NC	NC	Hold

NOTES:
H = High voltage level
h = High voltage level one setup time prior to low-to-high clock transition
L = Low voltage level
l = Low voltage level one setup time prior to low-to-high clock transition
NC = No change from the previous setup
X = Don't care
↑ = Low-to-high clock transition
↕ = Not low-to-high clock transition
* = This setup is unstable and will change when either set or reset return to the high level.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0		0.5	1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		3		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	345			MHz
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	1	1.0 1.0	3.1 3.6	4.8 5.0	5.8 5.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$Dn to Qn or $\overline{Q}$n	2	1.0 1.0	3.1 3.0	5.0 4.4	6.2 4.8	ns

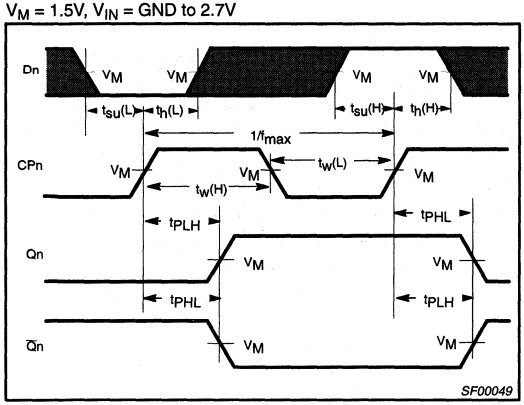
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS

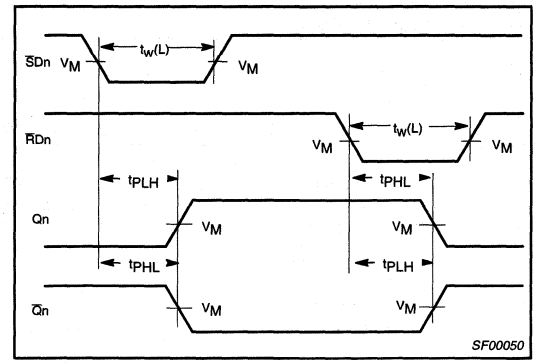
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
t_S (H) t_S (L)	Setup time Dn to CPn	1	1.7 1.4	0.6 0.4	1.8 1.6	ns
t_h (H) t_h (L)	Holdtime Dn to CPn	1	0.3 0	–0.3 –0.6	0.3 0	ns
t_W (H) t_W (L)	CPn Pulse Width	1	2.0 2.0	1.0 1.2	3.0 3.0	
t_W (L)	$\overline{S}$Dn, $\overline{R}$Dn Pulse Width	2	2.0	1.0	3.0	ns
t_{rec}	Recovery time $\overline{S}$Dn, $\overline{R}$Dn tp CPn	3	0.5	–0.3	0.5	

AC WAVEFORMS

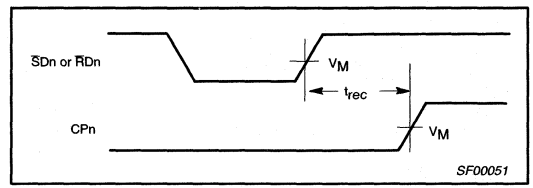
V_M = 1.5V, V_{IN} = GND to 2.7V



Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency

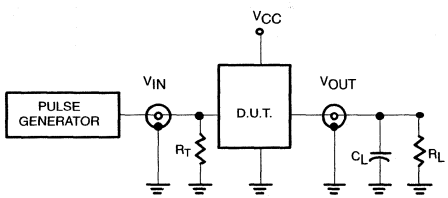


Waveform 2. Propagation delay for set and reset to output, set and reset pulse width

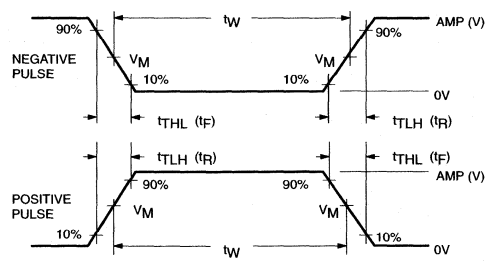


Waveform 3. Recovery time for set or reset to clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

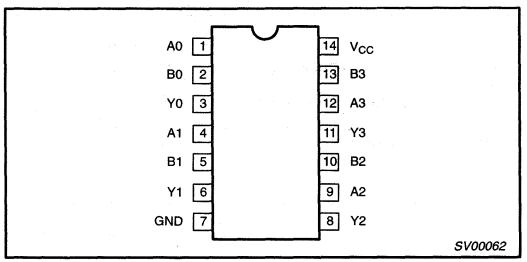
SV00022

3.3V Quad 2-input exclusive-OR gate 74LVT86

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An or Bn to Yn	C_L = 50pF; V_{CC} = 3.3V	3.4 3.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CCL}	Total supply current	Outputs Low; V_{CC} = 3.6V	1	mA

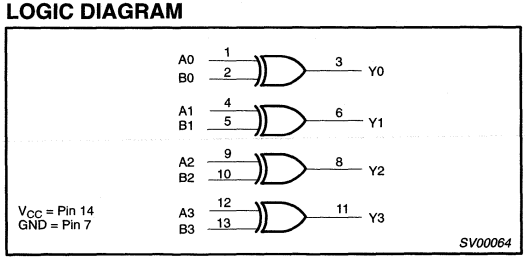
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	A_n, B_n	Data inputs
3, 6, 8, 11	Y_n	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC DIAGRAM

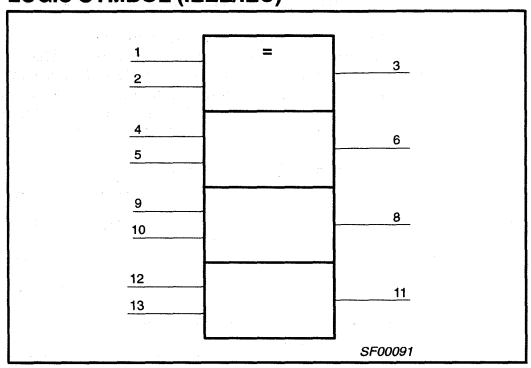


FUNCTION TABLE

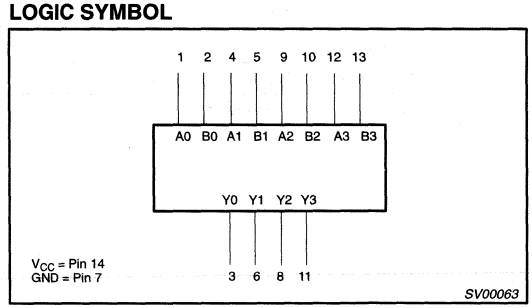
INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	L
L	H	H
H	L	H
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT86 D	74LVT86 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT86 DB	74LVT86 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT86 PW	74LVT86PW DH	SOT402-1

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–32	mA
		Output in Low state	64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA	V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –6mA	2.4			
		V_{CC} = 3.0V; I_{OH} = –20mA	2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.5	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.5	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±1	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.02	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0		1	2	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	µA
C_I	Input capacitance	V_I = 3V or 0		3		pF

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

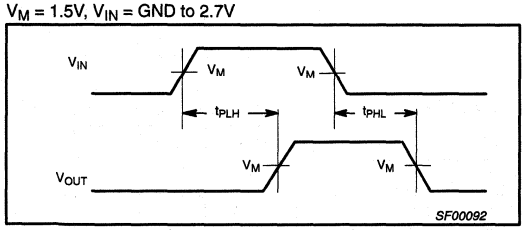
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An or Bn to Yn (other input Low)	1	1.0 1.0	3.0 3.5	4.2 5.1	5.3 5.6	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Yn (other input High)	2	1.0 1.0	3.4 3.1	5.2 4.2	6.3 4.4	ns

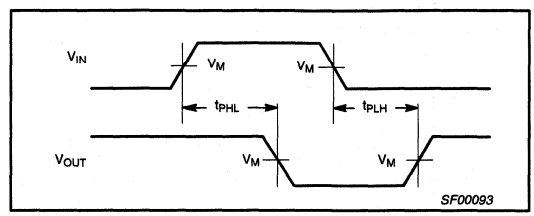
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

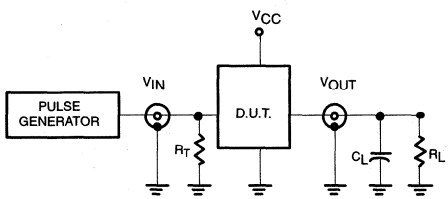


Waveform 1. Propagation Delay for Non-Inverting Outputs

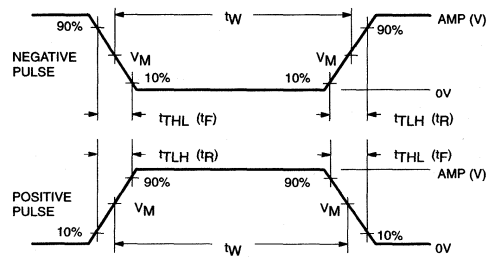


Waveform 2. Propagation Delay for Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00022

3.3V Quad buffer (3-State) 74LVT125

FEATURES

- Quad bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT125 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT125 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$, $\overline{OE}3$), each controlling one of the 3-State outputs.

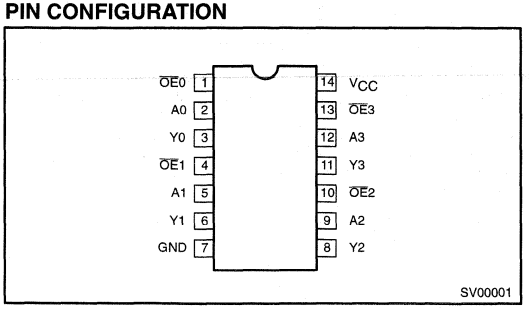
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 3.3V	2.7 2.9	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

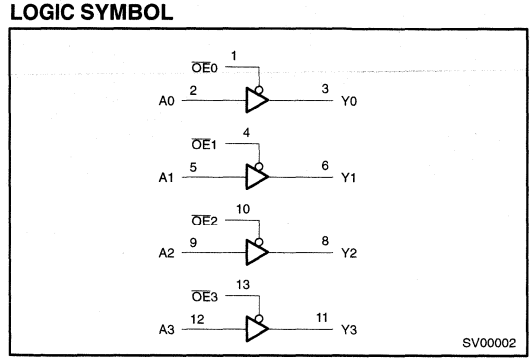
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT125 D	74LVT125 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT125 DB	74LVT125 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT125 PW	74LVT125PW DH	SOT402-1

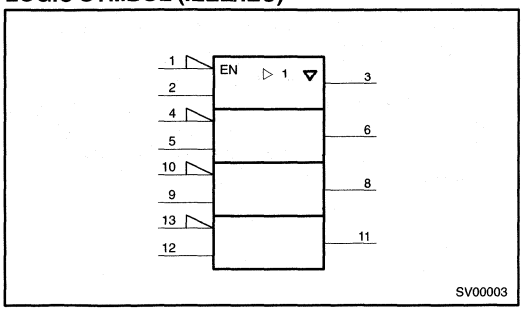
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE (EACH BUFFER)

INPUTS		OUTPUTS
$\overline{OE}n$	An	Yn
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 9, 12	A0 – A3	Data inputs
3, 6, 8, 11	Y0 – Y3	Data outputs
1, 4, 10, 13	$\overline{OE}0 – \overline{OE}3$	Output enables
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Out in High State	–64	mA
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V	All inputs		1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{OZH}	3-State output high current	V_{CC} = 3.6V; V_O = 3.0V			1	5	µA
I_{OZL}	3-State output low current	V_{CC} = 3.6V; V_O = 0.5V			–1	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

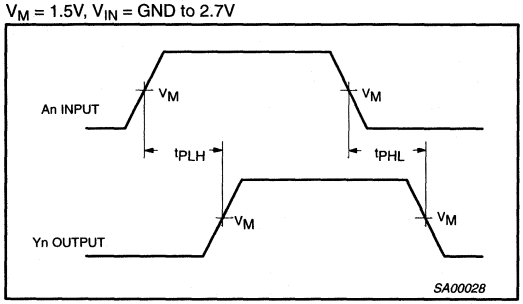
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω, T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Yn	6	1.0 1.0	2.7 2.9	4.0 3.9	4.5 4.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$n to Yn	7	1.0 1.1	3.4 3.4	4.7 4.7	6.0 6.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$n to Yn	7	1.8 1.3	3.7 2.6	5.1 4.5	5.7 4.0	ns

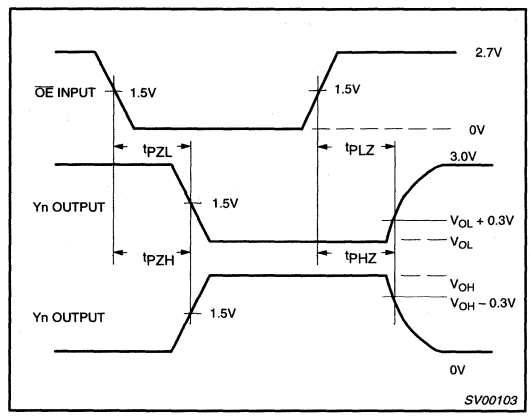
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

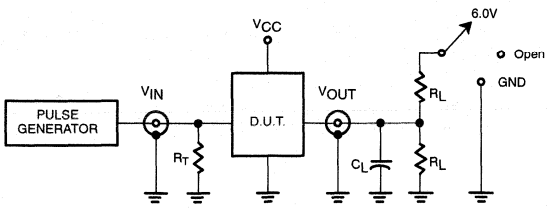


Waveform 6. Input (An) to Output (Yn) Propagation Delays

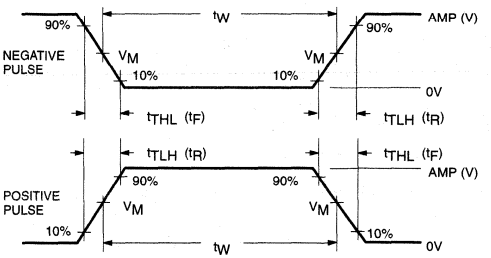


Waveform 7. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV00092

3.3V Quad buffer (3-State) 74LVT126

FEATURES

- Quad bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT126 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT126 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables (OE0, OE1, OE2, OE3), each controlling one of the 3-State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 3.3V	2.3 2.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

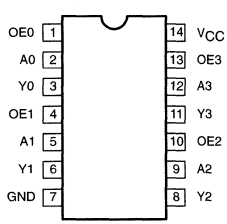
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVT126 D	74LVT126 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT126 DB	74LVT126 DB	SOT337-1
14-Pin Plastic TSSOP	–40°C to +85°C	74LVT126 PW	74LVT126PW DH	SOT402-1

PIN DESCRIPTION

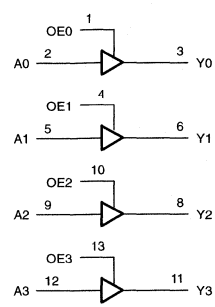
PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 9, 12	A0 – A3	Data inputs
3, 6, 8, 11	Y0 – Y3	Data outputs
1, 4, 10, 13	OE0 – OE3	Output enable inputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

PIN CONFIGURATION



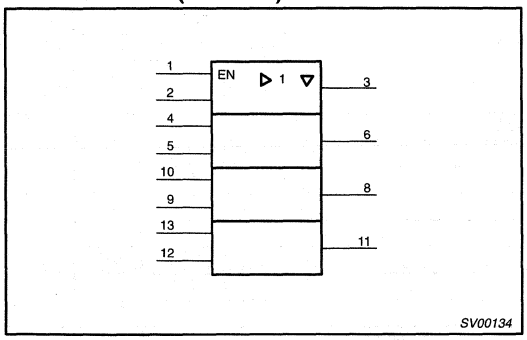
SA00031

LOGIC SYMBOL



SV00093

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS
OEn	An	Yn
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Out in High State	–64	mA
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V	All inputs		1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{OZH}	3-State output high current	V_{CC} = 3.6V; V_O = 3.0V			1	5	µA
I_{OZL}	3-State output low current	V_{CC} = 3.6V; V_O = 0.5V			–1	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or down to GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

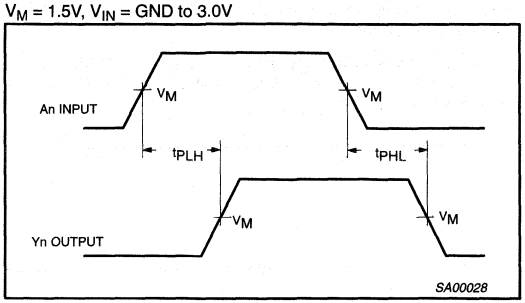
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω, T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.3 2.4	3.8 3.9	4.5 4.4	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$n to Yn	2	1.0 1.1	3.6 3.6	5.4 5.2	6.1 5.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$n to Yn	2	1.0 1.3	2.2 3.6	3.8 5.5	4.3 6.1	ns

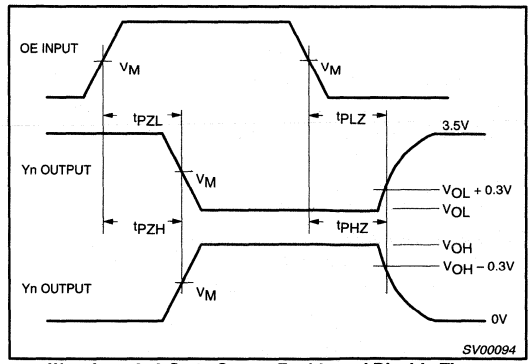
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

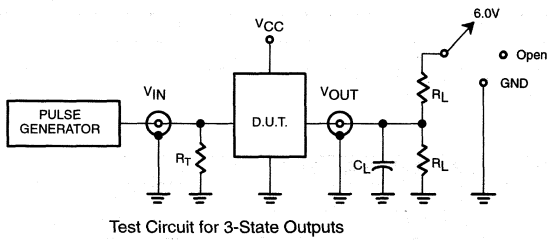


Waveform 1. Input (An) to Output (Yn) Propagation Delays

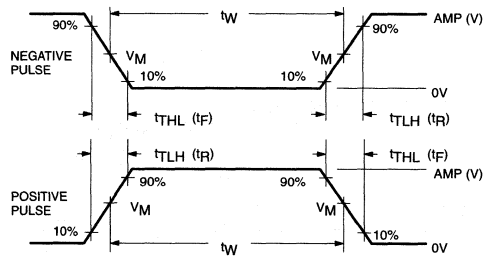


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal inverting buffer (3-State) 74LVT240

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model.

DESCRIPTION

The LVT240 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

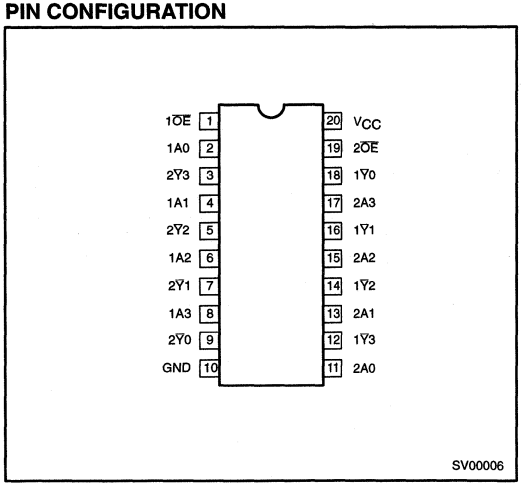
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 3.3V	2.5 2.6	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.12	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT240 D	74LVT240 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT240 DB	74LVT240 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT240 PW	74LVT240PW DH	SOT360-1

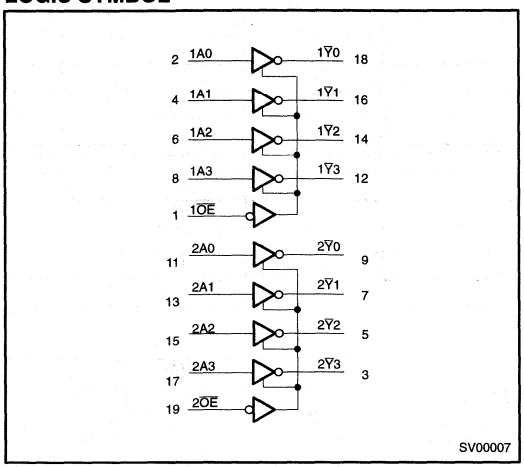
PIN CONFIGURATION



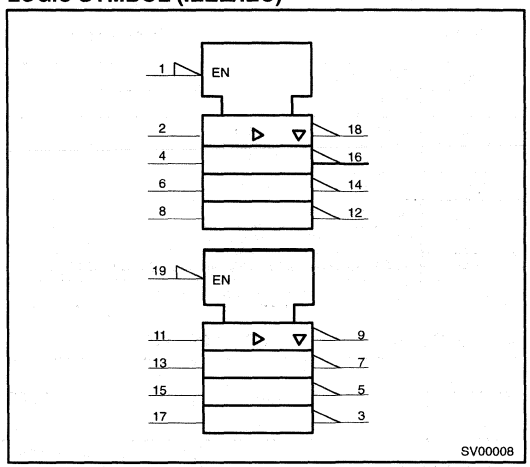
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1$\overline{Y}$0 – 1$\overline{Y}$3	Data outputs
9, 7, 5, 3	2$\overline{Y}$0 – 2$\overline{Y}$3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	$n\overline{Y}x$
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_I = –18mA			0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		V
		V_{CC} = 3V; I_{OH} = –32mA		2	2.2		V
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} = ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V			1	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V			–1	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.12	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.12	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3.0 to 3.6V; One input at V_{CC} -0.6V; Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. This is the increase in supply current for each input at V_{CC} –0.6V.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 10% a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C, only.
4. Unused pins at V_{CC} or GND
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

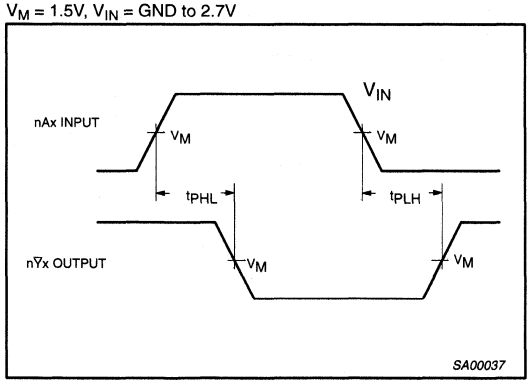
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T_{amb} = –40°C to +85°C, V_{CC} = +3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	3	1 1	2.5 2.5	4.3 4.3	5.2 5.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4	1 1	3.7 3.1	5.2 5.2	6.3 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4	2 1.6	3.4 3.2	5.6 5.1	6.3 5.6	ns

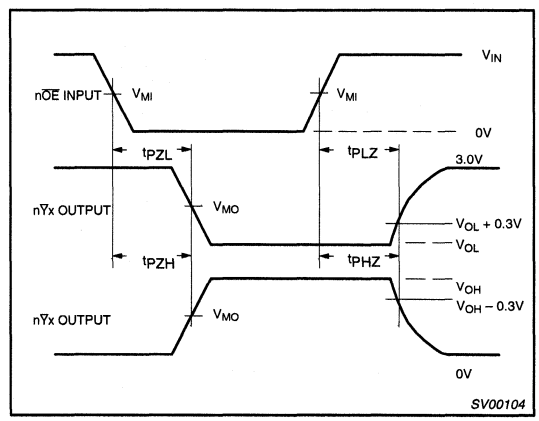
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

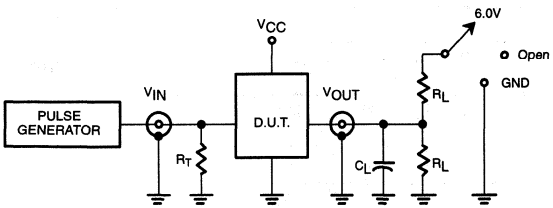


Waveform 3. Input (nAx) to Output (n$\overline{Y}$x) Propagation Delays

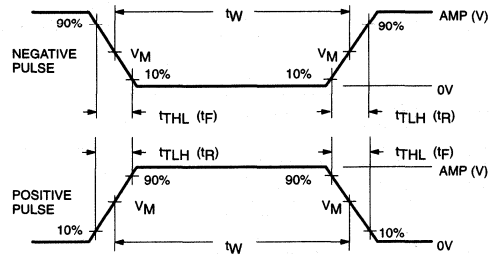


Waveform 4. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV00092

3.3V Octal buffer/line driver (3-State) 74LVT241

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model.

DESCRIPTION

The 74LVT241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT241 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, 2OE), each controlling four of the 3-State outputs.

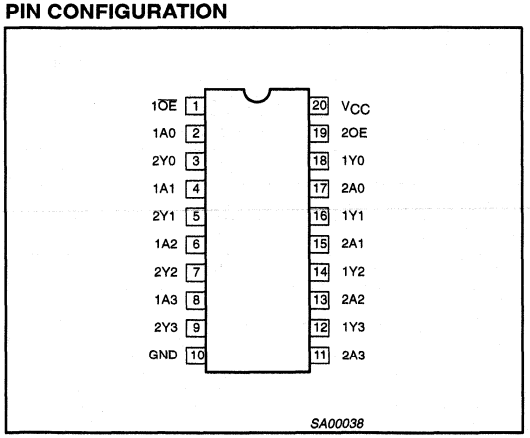
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	2.8 2.8	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.12	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT241 D	74LVT241 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT241 DB	74LVT241 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT241 PW	74LVT241PW DH	SOT360-1

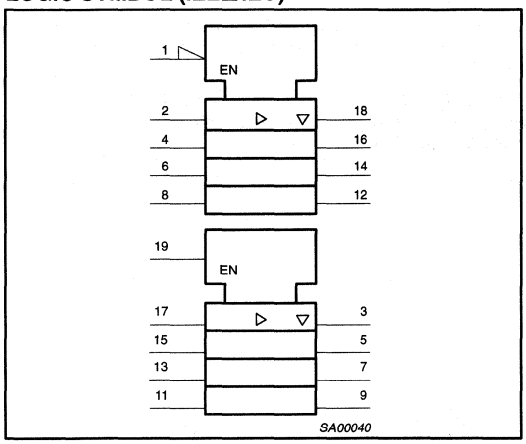
PIN CONFIGURATION



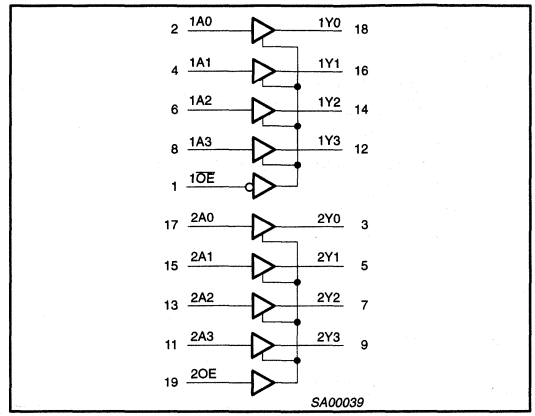
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
17, 15, 13, 11	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
3, 5, 7, 9	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, 2OE	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	2OE	2An	1Yn	2Yn
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_I = –18mA			0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		V
		V_{CC} = 3V; I_{OH} = –32mA		2	2.2		V
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} = ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V			1	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V			–1	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.12	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.12	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3.0 to 3.6V; One input at V_{CC} -0.6V; Other inputs at V_{CC} or GND			0.1	0.25	mA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. This is the increase in supply current for each input at V_{CC} –0.6V.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 10% a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

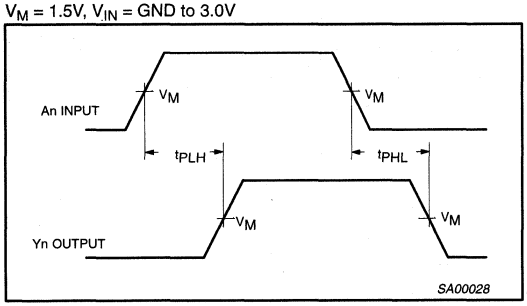
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T_{amb} = –40°C to +85°C V_{CC} = +3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1 1	2.8 2.8	3.8 3.8	4.0 4.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level 1$\overline{OE}$ to 1Y_n	2	1 1	3.2 3.1	4.4 4.3	5.0 4.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level 1$\overline{OE}$ to 1Y_n	2	2 1.6	3.6 2.9	5.2 4.2	5.4 4.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level 2OE to 2Y_n	2	1 1	3.8 3.8	5.1 5.0	5.6 5.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level 2OE to 2Y_n	2	1 1	3.1 2.8	4.5 4.0	5.0 4.3	ns

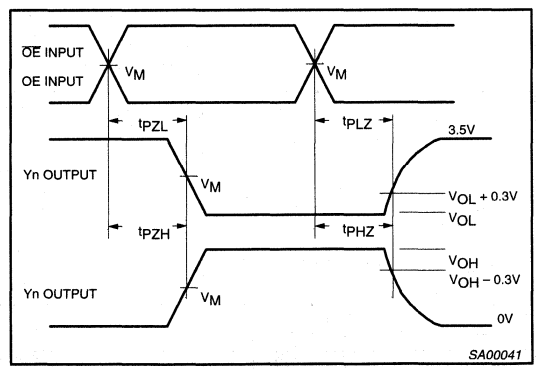
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

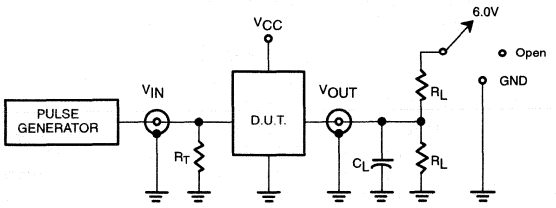


Waveform 1. Input (An) to Output (Yn) Propagation Delays

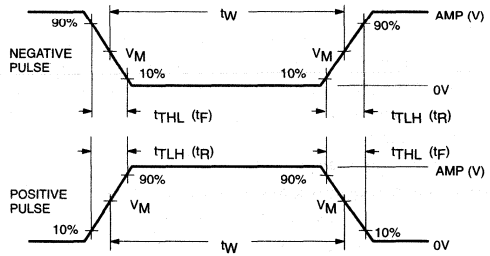


Waveform 2. 3–State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal buffer/line driver with 30Ω series termination resistors (3-State)

74LVT2241

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model.
- Outputs include series resistance of 30Ω, making external termination resistors unnecessary.

DESCRIPTION

The 74LVT2241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT2241 device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, 2OE), each controlling four of the 3-State outputs.

The 74LVT2241 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces the line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

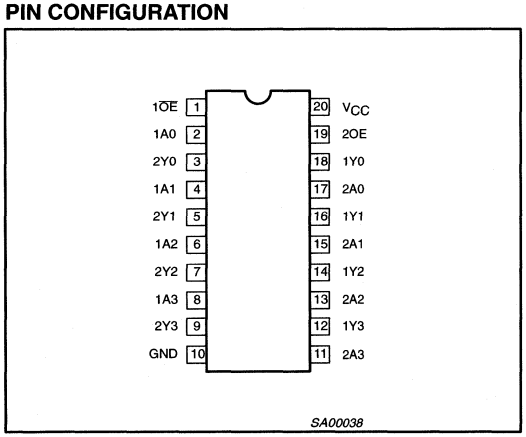
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	3.0 3.3	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.12	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT2241 D	74LVT2241 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT2241 DB	74LVT2241 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT2241 PW	7LVT2241PW DH	SOT360-1

PIN CONFIGURATION



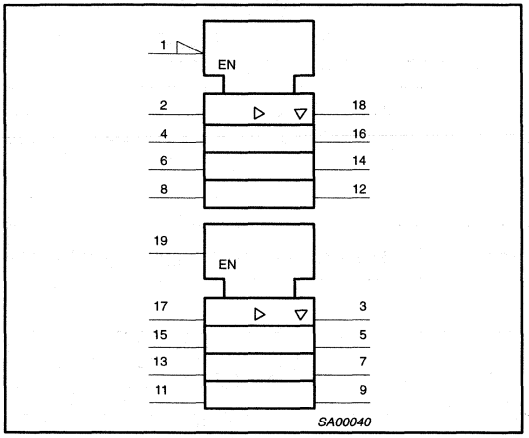
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
17, 15, 13, 11	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
3, 5, 7, 9	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, 2OE	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

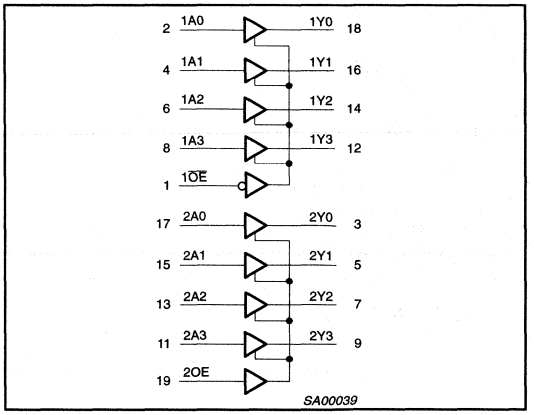
3.3V Octal buffer/line driver with 30Ω series termination resistors (3-State)

74LVT2241

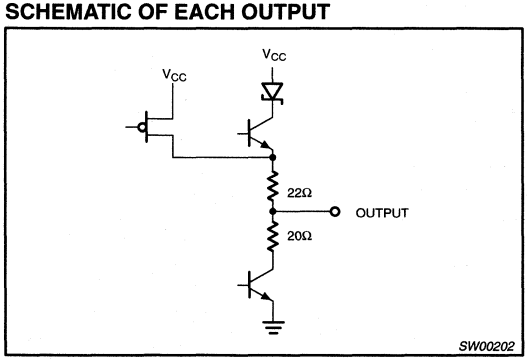
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



SCHEMATIC OF EACH OUTPUT



FUNCTION TABLE

INPUTS				OUTPUTS	
$1\overline{OE}$	1An	2OE	2An	1Yn	2Yn
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_I = –18mA			0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3V; I_{OH} = –12mA		2	2.2		V
V_{OL}	Low-level output voltage	V_{CC} = 3V; I_{OL} = 12mA				0.8	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus hold current A inputs	V_{CC} = 3.0V; V_I = 0.8V	A inputs	75	150		µA
		V_{CC} = 3.0V; V_I = 2.0V		-75	–150		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} = ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V			1	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V			–1	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.12	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.12	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3.0 to 3.6V; One input at V_{CC} -0.6V; Other inputs at V_{CC} or GND			0.1	0.25	mA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. This is the increase in supply current for each input at V_{CC} –0.6V.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 10% a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.

AC CHARACTERISTICS

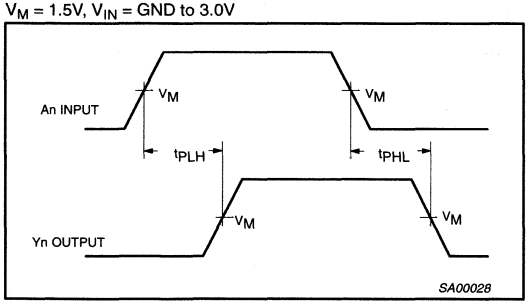
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T_{amb} = –40°C to +85°C, V_{CC} = +3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1 1	3.0 3.3	4.2 4.3	5.0 4.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level, 1$\overline{OE}$ to $1Y_n$	2	1 1	4.4 4.3	6.2 5.9	8.5 6.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level, 1$\overline{OE}$ to $1Y_n$	2	1 1.6	3.4 3.2	5.0 4.5	5.2 4.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level, 2OE to $2Y_n$	2	1 1	4.4 4.1	6.2 5.5	7.9 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level, 2OE to $2Y_n$	2	1 1	3.9 3.8	5.7 5.1	6.4 5.8	ns

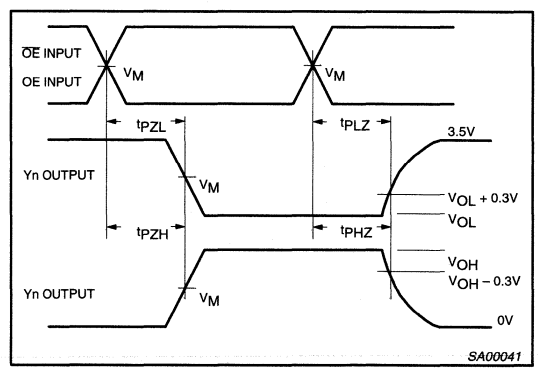
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

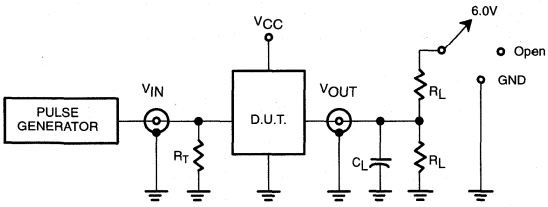


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

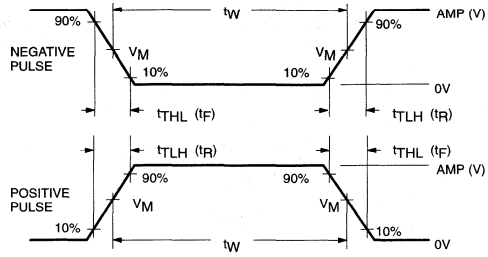


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal buffer/line driver (3-State) 74LVT244A

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT244A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($\overline{OE}1$, $\overline{OE}2$), each controlling four of the 3-State outputs.

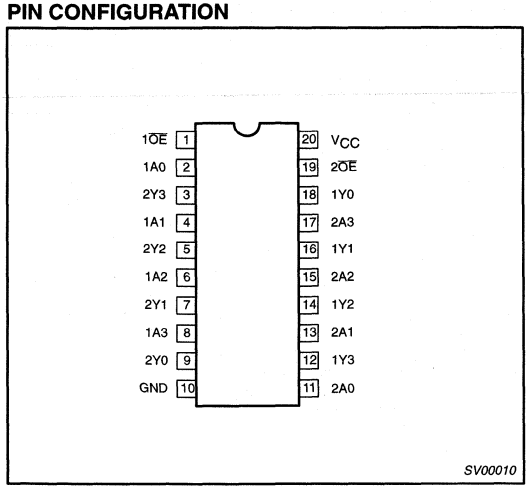
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	2.5 2.6	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT244A D	74LVT244A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT244A DB	74LVT244A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT244A PW	7LVT244APW DH	SOT360-1

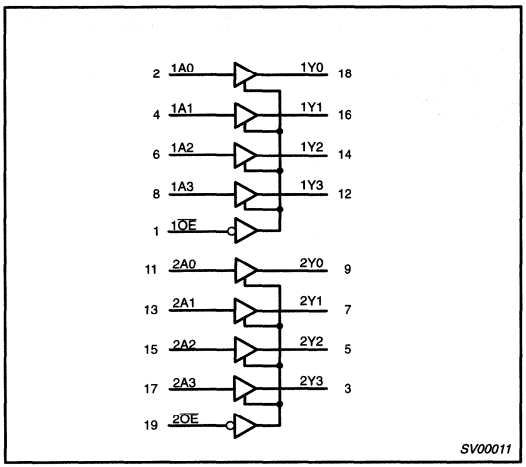
PIN CONFIGURATION



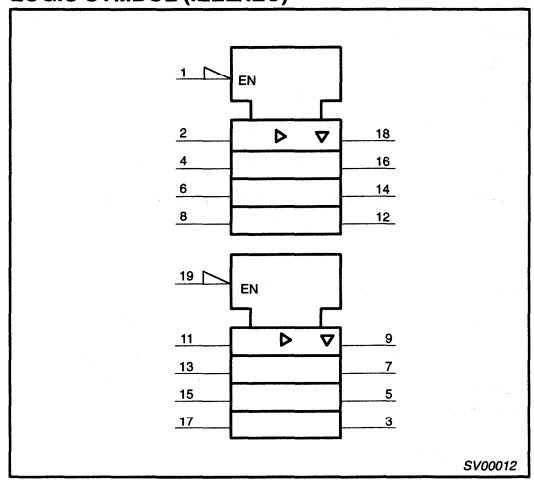
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11. 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{nOE}1$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data Pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{OZH}	3-State output high current	V_{CC} = 3.6V; V_O = 3V; V_I = V_{IL} or V_{IH}			1	5	µA
I_{OZL}	3-State output low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

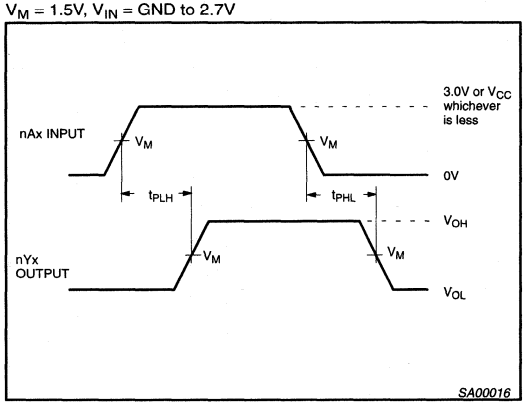
GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1 1	2.5 2.6	4.1 4.1	5.0 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1 1.1	3.2 3.1	5.2 5.2	6.3 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.9 1.8	3.3 3.3	5.6 5.1	6.3 5.6	ns

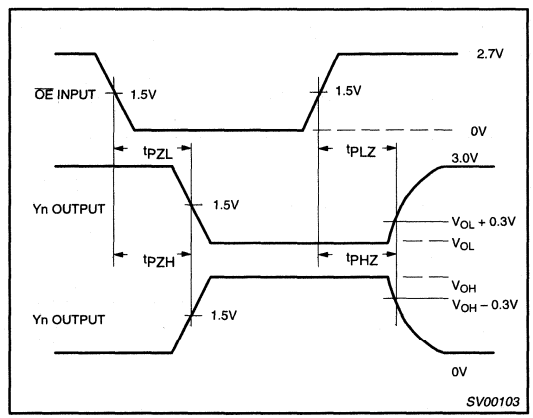
NOTE:
1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25°C$.

AC WAVEFORMS

$V_M = 1.5V$, V_{IN} = GND to 2.7V

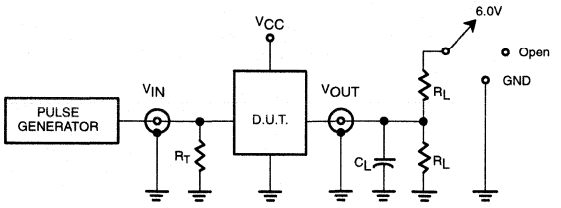


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

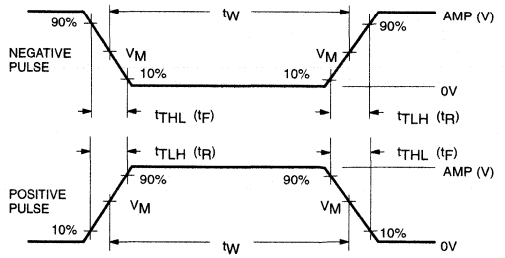


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal buffer/line driver with 30Ω series termination resistors (3-State)

74LVT2244

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Outputs include series resistance of 30Ω, making external termination resistors unnecessary.

DESCRIPTION

The LVT2244 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($\overline{OE}1$, $\overline{OE}2$), each controlling four of the 3-State outputs.

The 74LVT2244 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces the line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

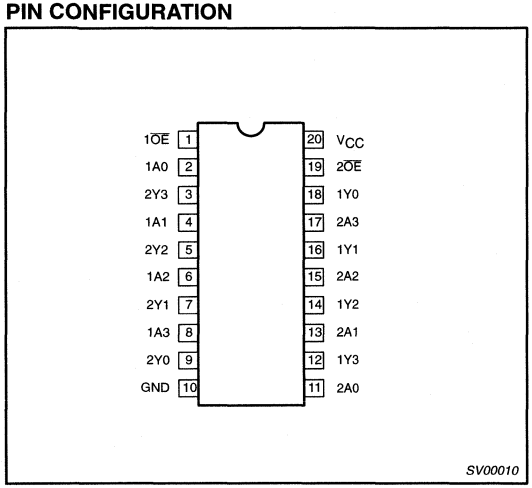
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	2.9 2.9	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT2244 D	74LVT2244 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT2244 DB	74LVT2244 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT2244 PW	7LVT2244PW DH	SOT360-1

PIN CONFIGURATION



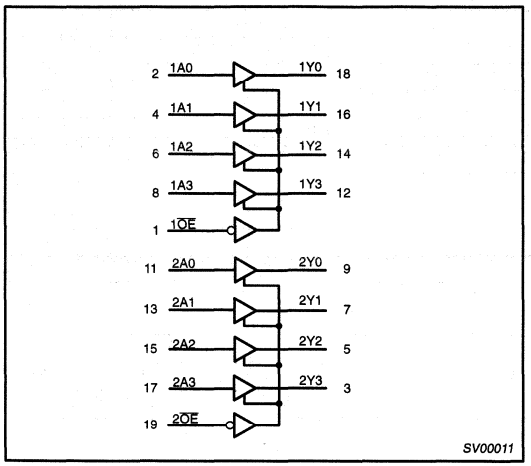
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11. 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	1$\overline{OE}$, 2$\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

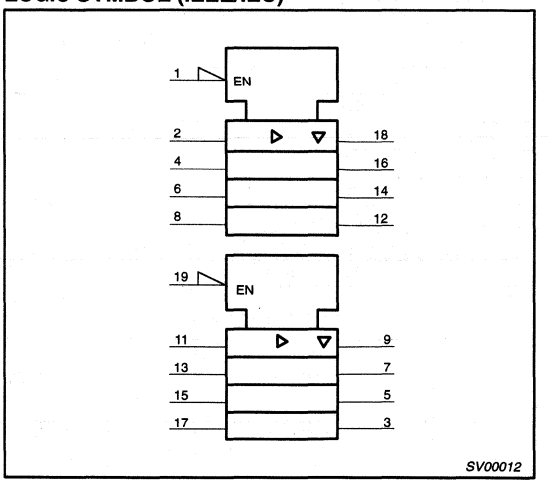
3.3V Octal buffer/line driver with 30Ω series termination resistors (3-State)

74LVT2244

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

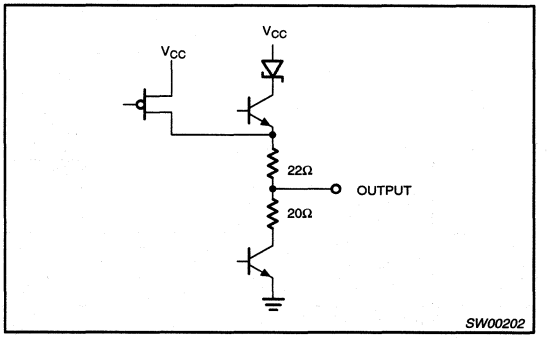


FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{nOE1}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

SCHEMATIC OF EACH OUTPUT



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_I = –18mA			0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3V; I_{OH} = –12mA		2	2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 3V; I_{OL} = 12mA				0.8	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} = ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V			1	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V			–1	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.12	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.12	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3.0 to 3.6V; One input at V_{CC} -0.6V; Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. This is the increase in supply current for each input at V_{CC} –0.6V.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 10% a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

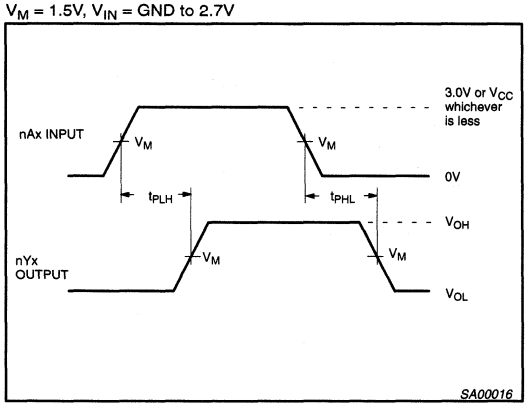
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1 1	2.9 2.9	4.4 4.1	5.3 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1 1.1	3.7 3.7	5.9 5.5	7.7 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.9 1.8	4.3 3.3	6.1 4.5	6.8 4.5	ns

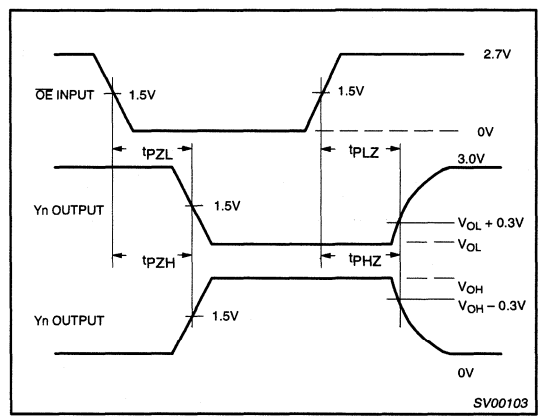
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

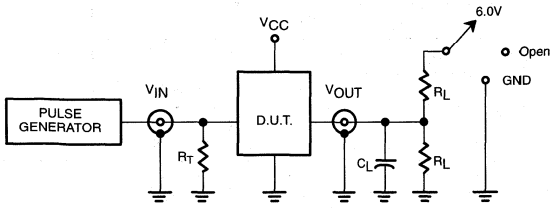


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

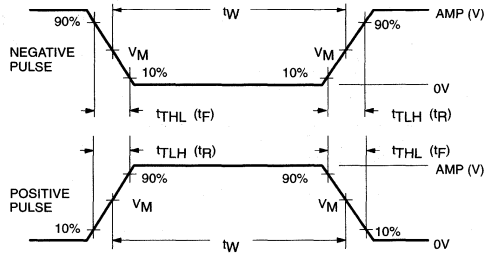


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal transceiver with direction pin (3-State) 74LVT245

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT245 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

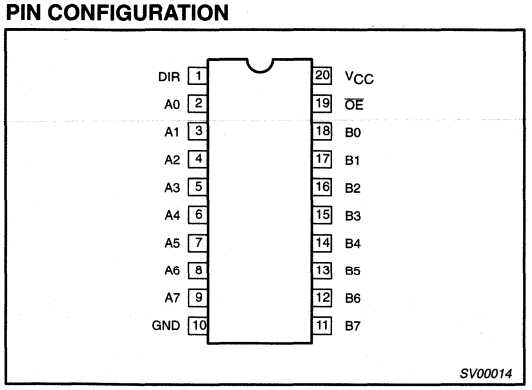
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.4	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SO	–40°C to +85°C	74LVT245 D	74LVT245 D	SOT163-1
20-Pin Plastic SSOP	–40°C to +85°C	74LVT245 DB	74LVT245 DB	SOT339-1
20-Pin Plastic TSSOP	–40°C to +85°C	74LVT245 PW	74LVT245PW DH	SOT360-1

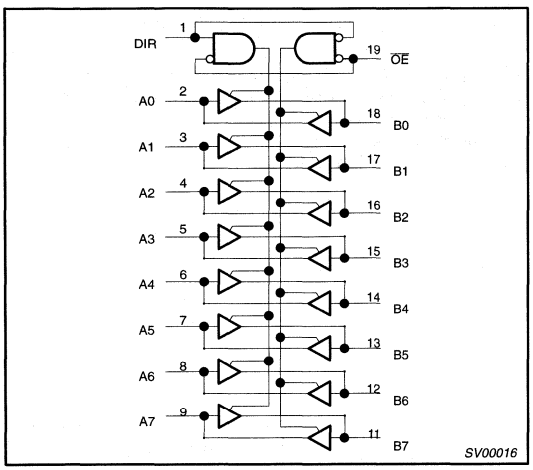
PIN CONFIGURATION



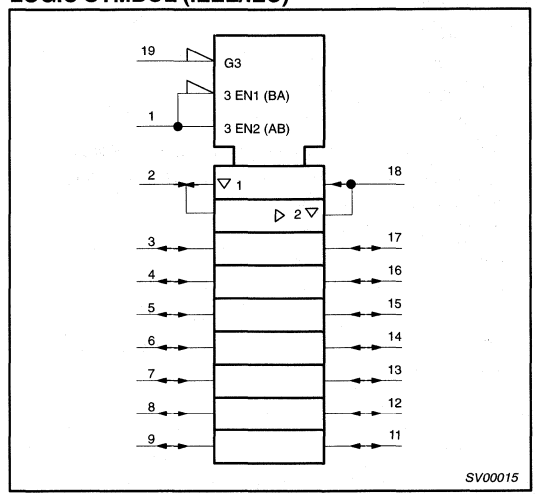
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active–Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}n$	DIR	An	Bn
L	L	An= Bn	Inputs
L	H	Inputs	Bn =An
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V	Control pins		1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±0.1	±1	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = +25°C only.
4. Unused pins at V_{CC} or GND.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

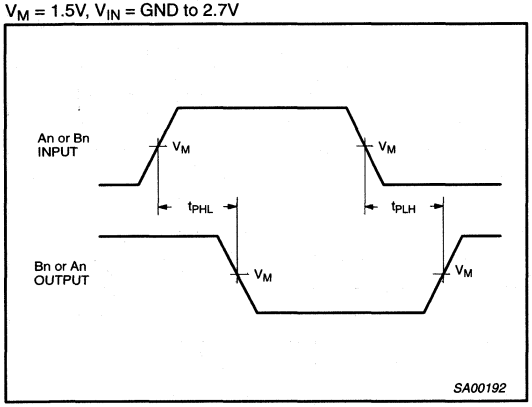
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V +0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.4 2.4	4.0 4.0	4.7 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.5	3.3 3.2	5.5 5.5	7.1 6.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	2.2 2.0	3.6 3.4	5.9 4.8	6.5 4.8	ns

NOTES:

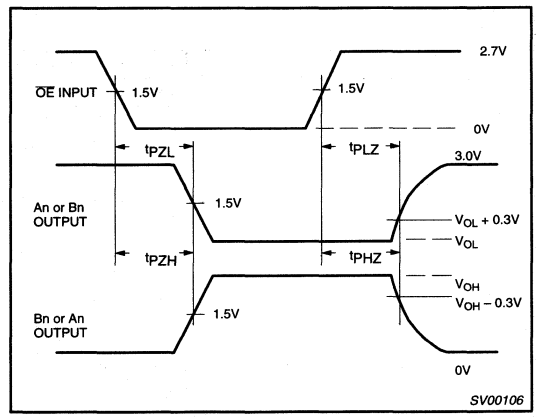
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

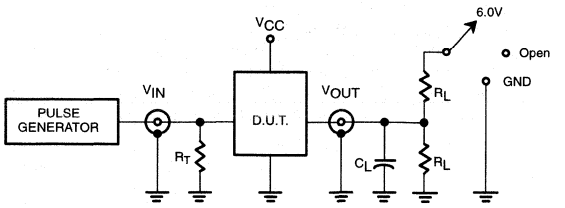


Waveform 1. Input (An or Bn) to Output (Bn or An) Propagation Delays

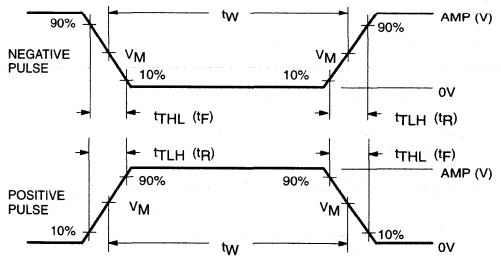


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal transceiver with 30Ω termination resistors (3-State)

74LVT2245

FEATURES

- 30Ω output termination resistors
- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT2245 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

The 74LVT2245 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

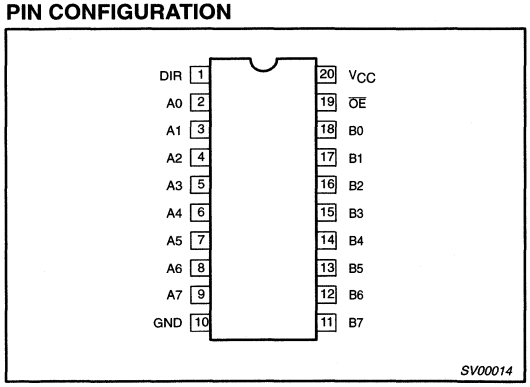
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	3.2 3.1	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

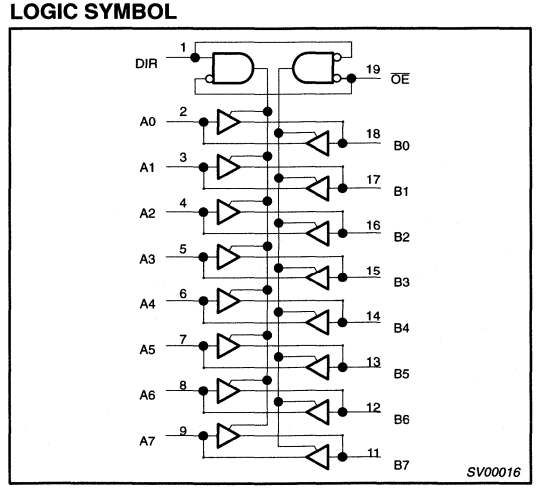
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SO	–40°C to +85°C	74LVT2245 D	74LVT2245 D	SOT163-1
20-Pin Plastic SSOP	–40°C to +85°C	74LVT2245 DB	74LVT2245 DB	SOT339-1
20-Pin Plastic TSSOP	–40°C to +85°C	74LVT2245 PW	7LVT2245PW DH	SOT360-1

PIN CONFIGURATION



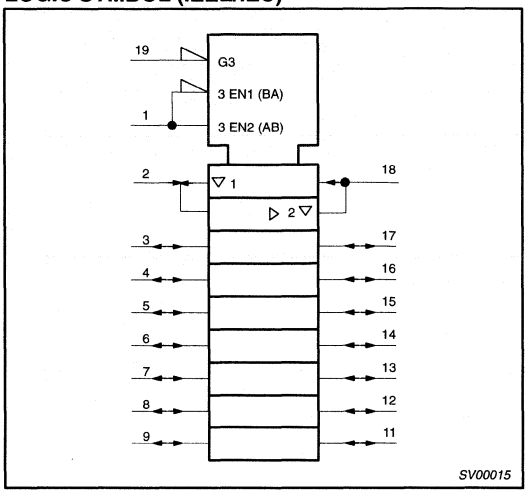
LOGIC SYMBOL



3.3V Octal transceiver with 30Ω termination resistors (3-State)

74LVT2245

LOGIC SYMBOL (IEEE/IEC)

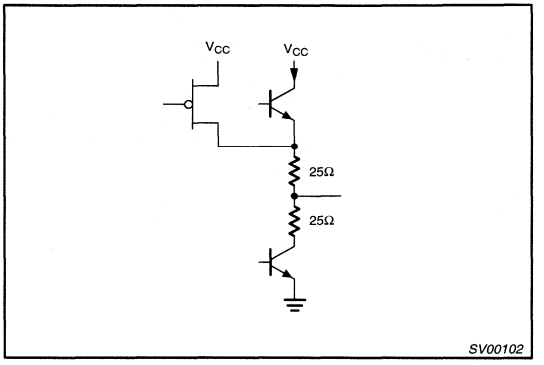


FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}n$	DIR	An	Bn
L	L	An= Bn	Inputs
L	H	Inputs	Bn =An
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

SCHEMATIC OF EACH OUTPUT



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active–Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = –40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0	2.2		V
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA				0.8	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V	Control pins		1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	µA
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	µA
		V_{CC} = 3.6V; V_I = V_{CC}	I/O Data pins[4]		0.1	1	µA
		V_{CC} = 3.6V; V_I = 0	I/O Data pins[4]		–1	-5	µA
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		µA
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			µA
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}	Quiescent supply current	V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	mA
I_{CCZ}	Quiescent supply current	V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.13	0.19	mA
ΔI_{CC}	Additional supply current per input pin[3]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = +25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or down to GND
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

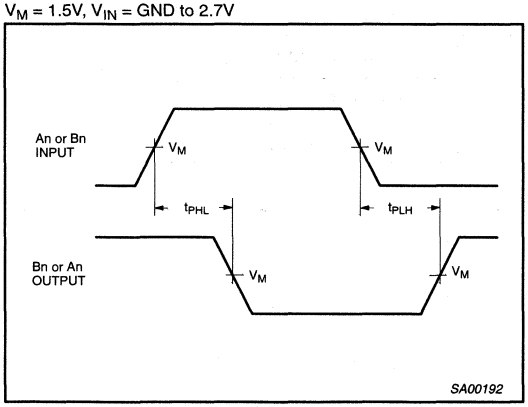
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V +0.3V			V_{CC} = 2.7V	
			MIN	TYP	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	3.2 3.1	4.6 4.5	5.3 4.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.5	4.5 4.3	7.0 6.5	9.1 7.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	2.2 2.0	3.7 3.6	5.2 5.0	5.6 5.0	ns

NOTE:

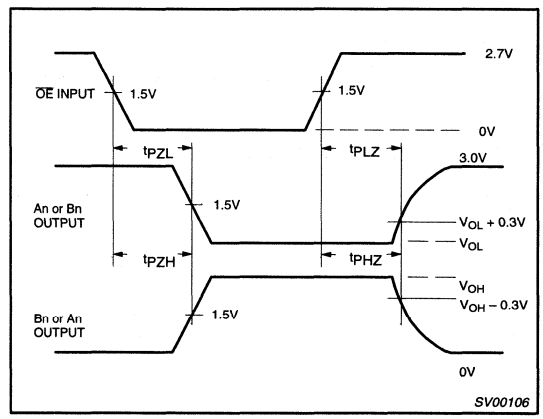
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

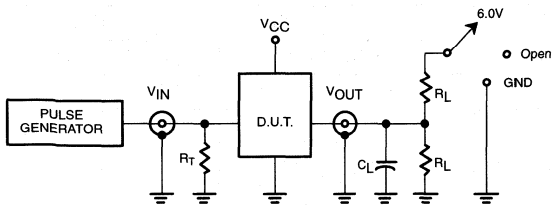


Waveform 1. Input (An or Bn) to Output (Bn or An) Propagation Delays

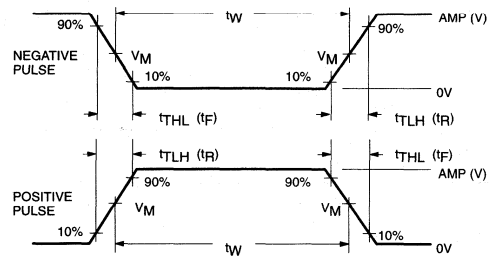


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV00092

3.3V Octal D flip-flop | 74LVT273

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latchup protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000V per Mil Std 883 Method 3015 and 200V per Machine Model.

DESCRIPTION

The LVT273 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

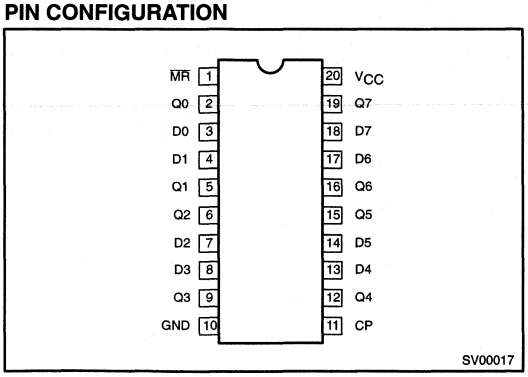
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 3.3V	3.5 3.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF

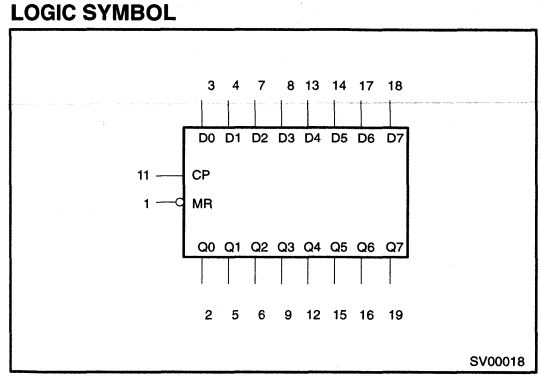
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT273 D	74LVT273 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT273 DB	74LVT273 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT273 PW	74LVT273PW DH	SOT360-1

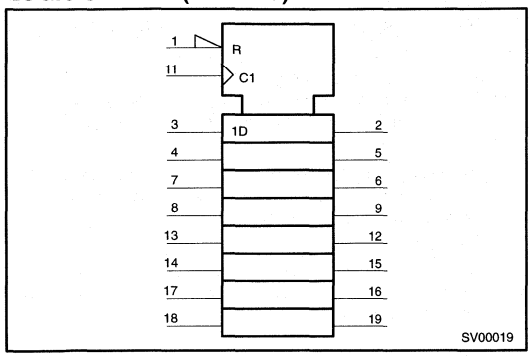
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

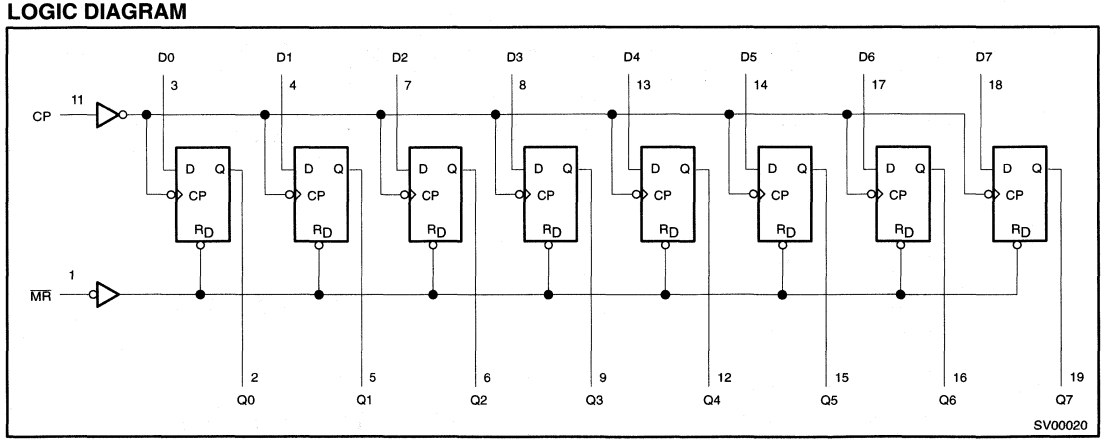
INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D_n	Q0 – Q7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"
H	L	X	Q_0	Retain state

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Q_0 = Output as it was

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock pulse input (active rising edge)
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Data outputs
1	$\overline{MR}$	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High State	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}–0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[4]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[3]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. Unused pins at V_{CC} or GND.
4. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.7 1.9	3.5 3.5	5.5 5.5	6.3 5.9	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2	1.3	3.2	6.2	6.2	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

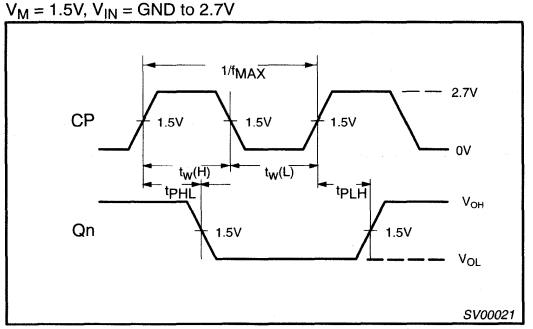
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω, T_{amb} = –40°C to +85°C.

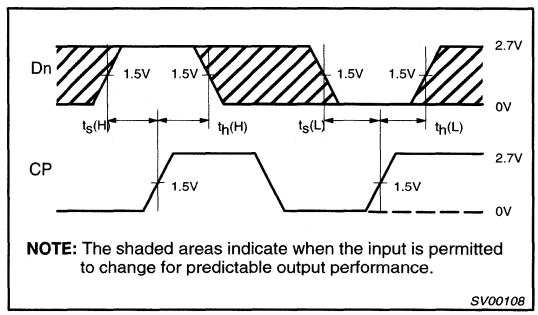
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = +3.3 ± 0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	3	2.3 2.3	1.0 1.0	2.7 2.7	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	3	0 0	–0.6 –0.6	0 0	ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	1	3.3 3.3	1.5 1.5	3.3 3.3	ns
$t_w(L)$	Master Reset pulse width, Low	2	3.3	1.5	3.3	ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	2.7	1.0	3.2	ns

AC WAVEFORMS

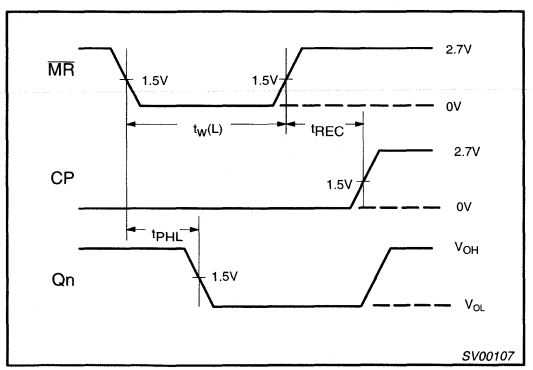
V_M = 1.5V, V_{IN} = GND to 2.7V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

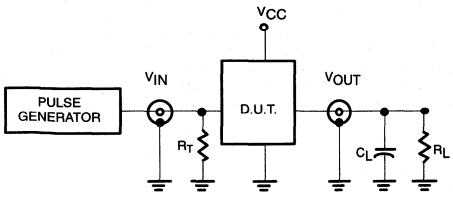


Waveform 3. Data Setup and Hold Times

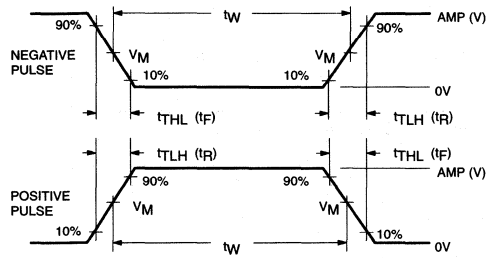


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00022

3.3V Octal D-type flip-flop; positive-edge trigger (3-State)

74LVT374

FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT374 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT374 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

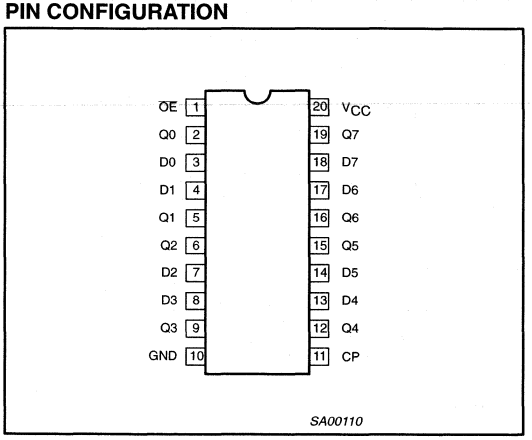
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 3.3V	3.2 3.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT374 D	74LVT374 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT374 DB	74LVT374 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT374 PW	74LVT374PW DH	SOT360-1

PIN CONFIGURATION

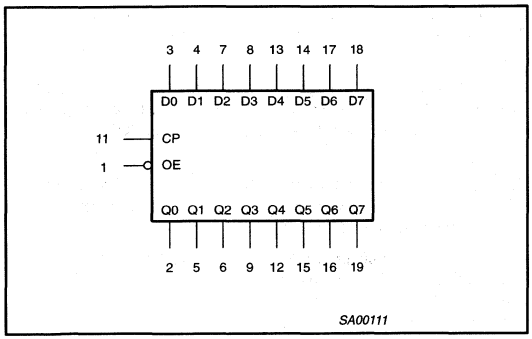


PIN DESCRIPTION

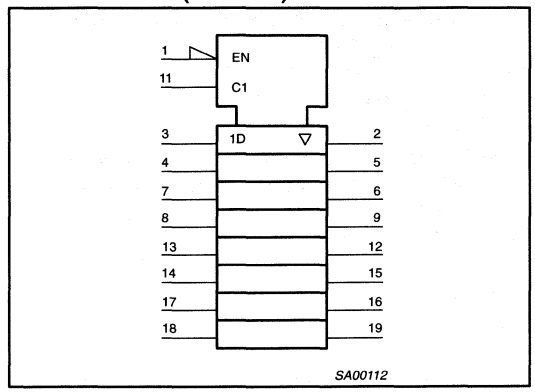
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

3.3V Octal D-type flip-flop; positive-edge trigger (3-State) 74LVT374

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

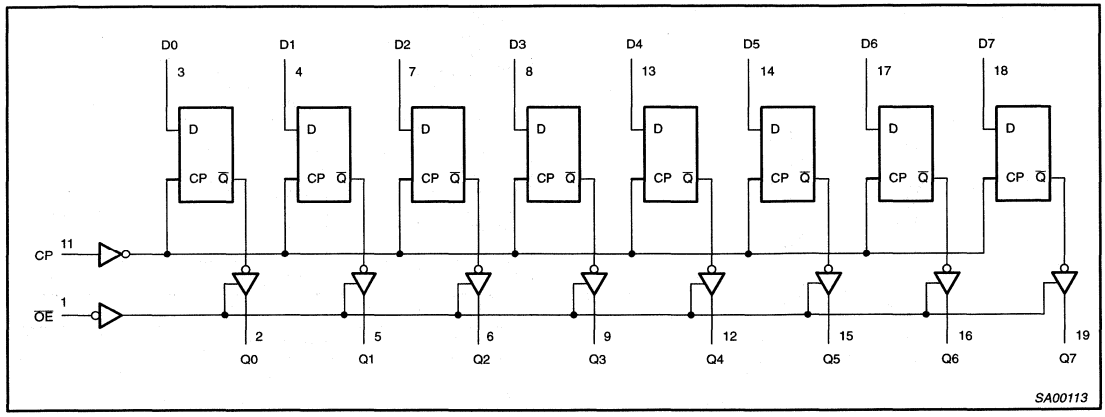


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn		Q0 – Q7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	X	X	NC	Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC}= 3.6V; V_O = 3V; V_I = V_{IL} or V_{IH}			1	5	µA
I_{OZL}	3-State output Low current	V_{CC}= 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			1	–5	µA
I_{CCH}	Quiescent supply current[3]	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or down to GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	125	200		125		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.7 2.2	3.2 3.5	5.1 5.2		5.8 5.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.5 2.0	3.2 3.4	5.3 5.2		7.3 6.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.9 2.0	4.3 3.4	6.7 5.1		7.1 5.1	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

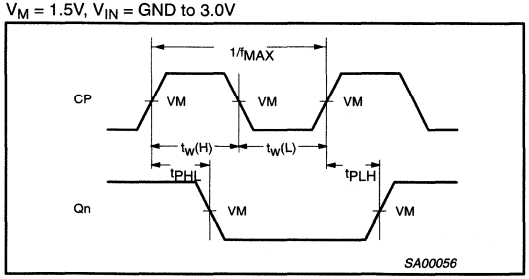
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

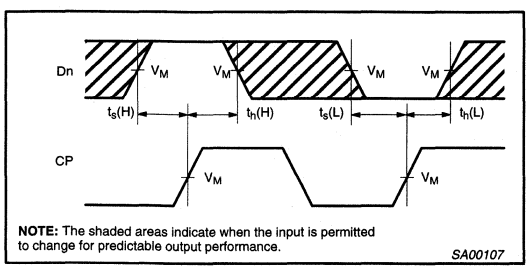
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low, Dn to CP	2	2.0 2.0	0.7 0.7	2.0 2.0	ns
$T_H(H)$ $T_H(L)$	Hold time, High or Low, Dn to CP	2	0.3 0.3	–0.5 –0.5	0 0	ns
$T_W(H)$	CP pulse width High or Low	1	1.5 2.5	0.8 1.7	1.5 3.0	ns

AC WAVEFORMS

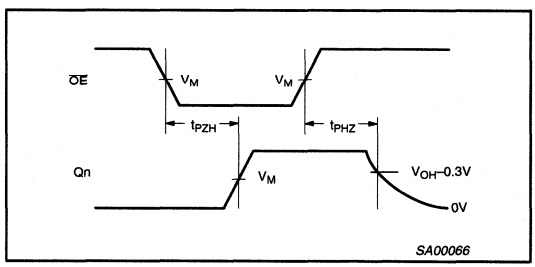
V_M = 1.5V, V_{IN} = GND to 3.0V



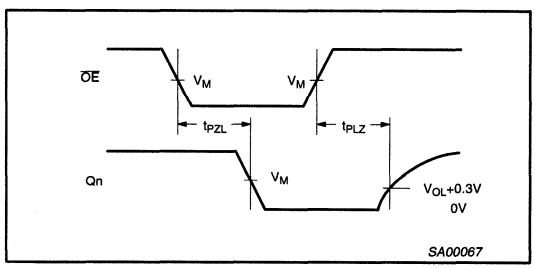
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

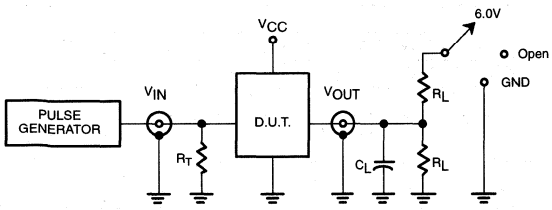


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

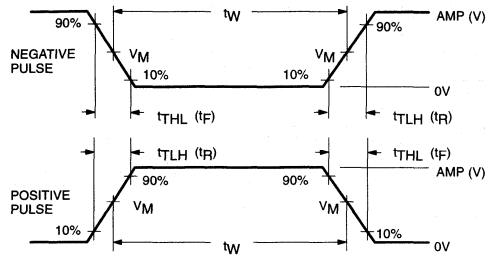


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV00092

3.3V Octal D-type flip-flop, inverting (3-State) 74LVT534

FEATURES

- 3-State outputs for bus interfacing
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT534 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The state of each D input (one set-up time before the Low-to-High clock transition) is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "off" state, which means they will neither drive nor load the bus.

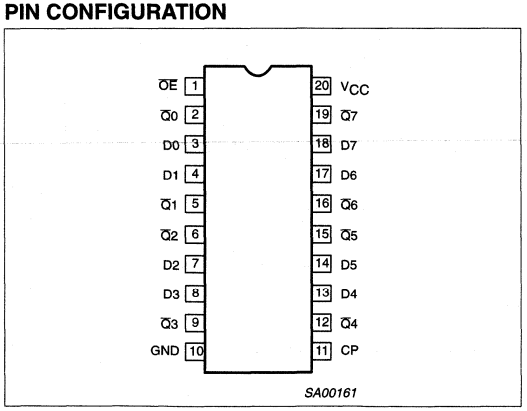
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 3.3V	3.0 3.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

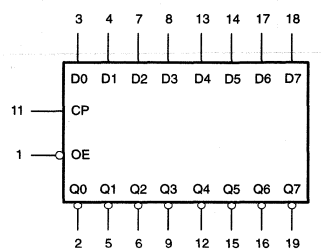
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT534 D	74LVT534 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT534 DB	74LVT534 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT534 PW	74LVT534PW DH	SOT360-1

PIN CONFIGURATION



SA00161

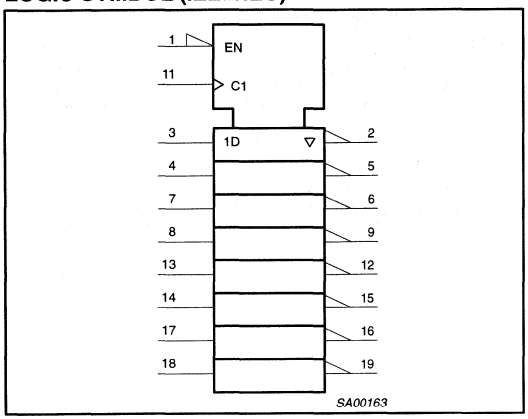
LOGIC SYMBOL



SA00162

3.3V Octal D-type flip-flop, inverting (3-State) 74LVT534

LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

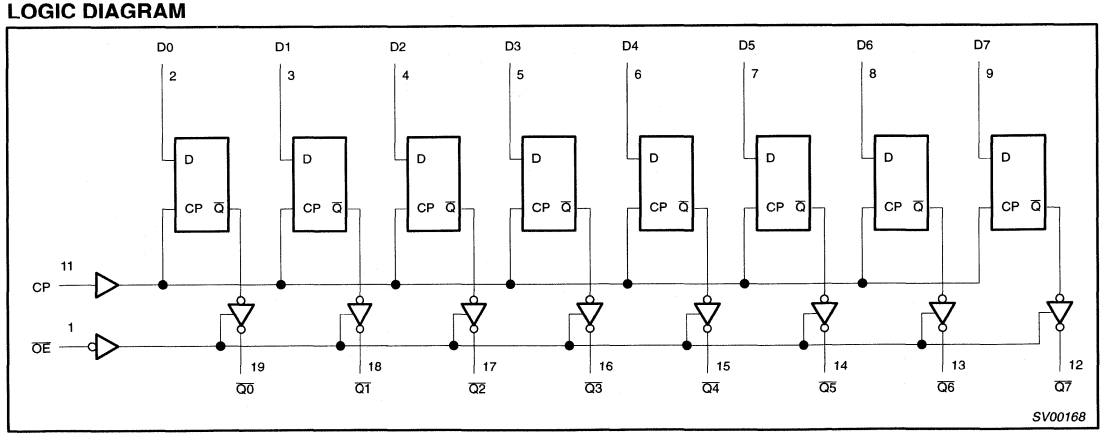
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}0$-$\overline{Q}7$	Inverting 3-State outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	$\overline{Q}0 - \overline{Q}7$	
L	↑	l	L	H	Latch and read register
L	↑	h	H	L	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC}= 3.6V; V_O = 3V; V_I = V_{IL} or V_{IH}			1	5	µA
I_{OZL}	3-State output Low current	V_{CC}= 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			1	–5	µA
I_{CCH}	Quiescent supply current[3]	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or down to GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ± 0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MIN	MAX	UNIT
f_{MAX}	Maximum clock frequency	1	100	150		100		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.7 2.2	3.0 3.5	4.6 4.9		5.4 5.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.7 1.7	3.2 3.3	5.4 5.5		7.0 5.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	2.1 2.1	3.5 3.4	3.0 4.8		5.3 4.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

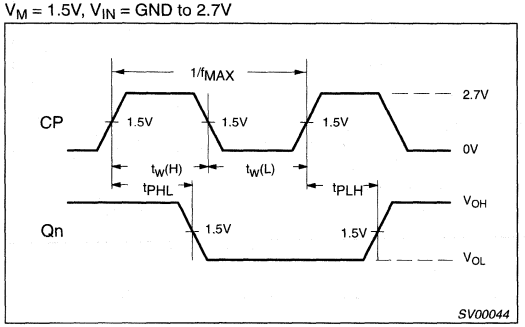
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = −40°C to +85°C.

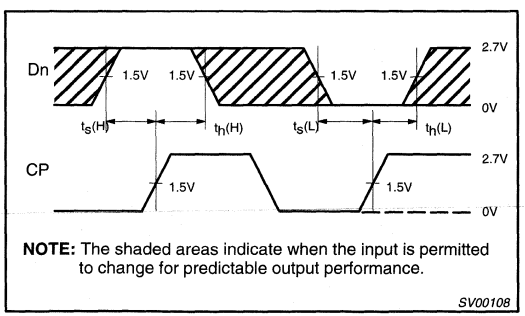
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low, Dn to CP	2	2.0 2.6	1.0 1.3	2.0 3.2	ns
$T_H(H)$ $T_H(L)$	Hold time, High or Low, Dn to CP	2	0 0	−1.3 −0.9	0 0	ns
$T_W(H)$ $T_W(L)$	CP pulse width High or Low	1	1.5 4.2	0.8 3.0	1.5 5.0	ns

AC WAVEFORMS

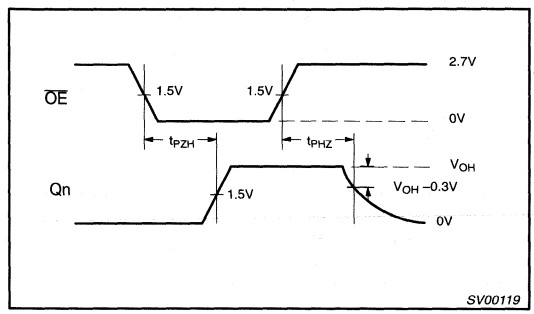
V_M = 1.5V, V_{IN} = GND to 2.7V



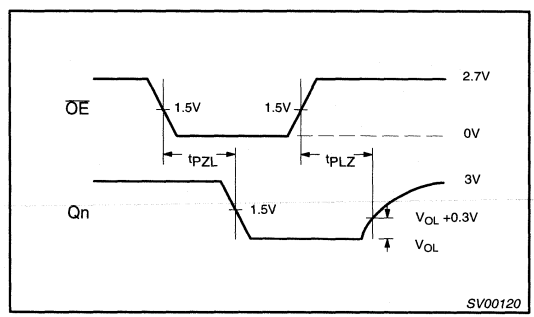
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

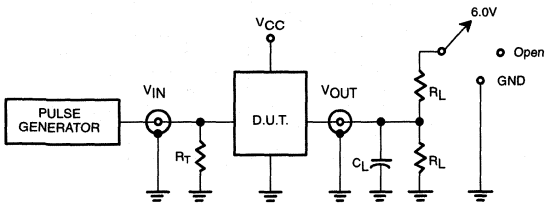


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

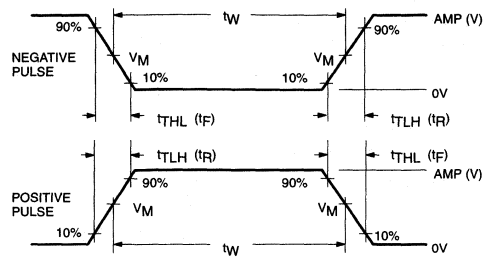


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV00092

3.3V Octal latched transceiver with dual enable (3-State)

74LVT543

FEATURES

- Combines 74LVT245 and 74LVT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT543 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 74LVT543 contains two sets of eight D–type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

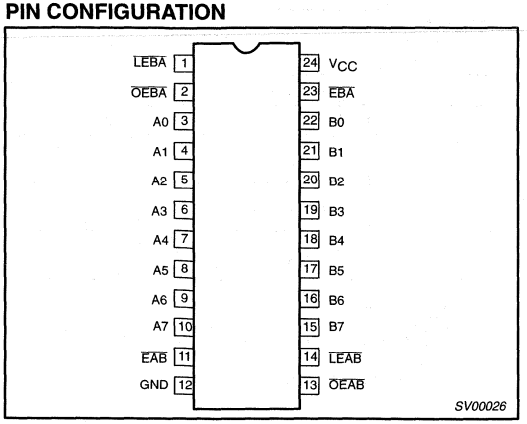
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.3 3.0	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

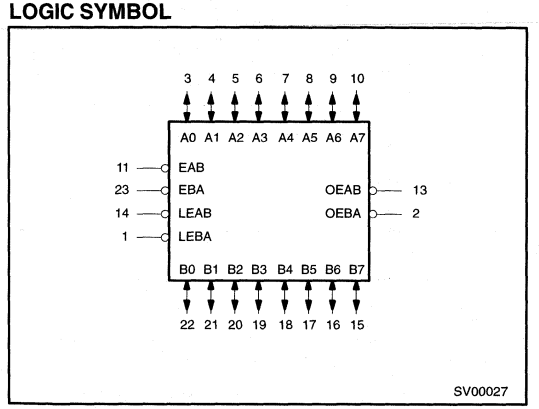
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic SOL	–40°C to +85°C	74LVT543 D	74LVT543 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT543 DB	74LVT543 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT543 PW	74LVT543PW DH	SOT355-1

PIN CONFIGURATION



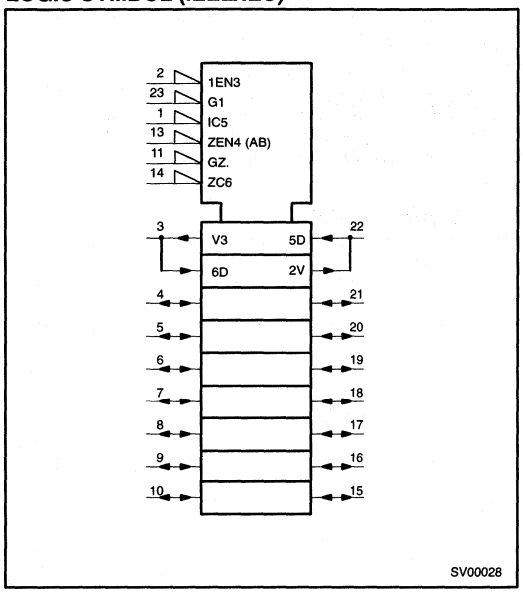
LOGIC SYMBOL



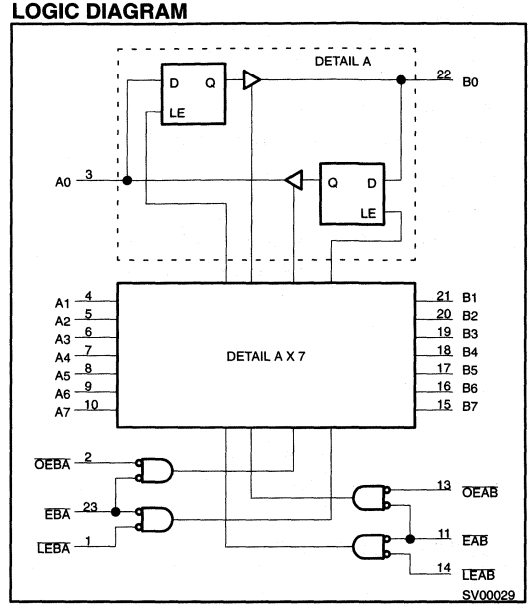
3.3V Octal latched transceiver with dual enable (3-State)

74LVT543

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (active-Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (active-Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable Input (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	A0 – A7	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	B0 – B7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	EXX	$\overline{LEXX}$	An or Bn	Bn or An	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	2	1.0 1.0	2.3 3.0	4.7 4.6	5.5 5.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	1 2	1.0 1.0	3.6 4.2	5.9 5.7	7.3 7.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	1.0 1.1	3.8 3.8	5.8 6.4	7.6 8.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	2.4 2.0	3.7 3.5	6.5 5.8	7.1 5.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	1.0 1.4	4.0 4.1	6.0 6.7	7.6 8.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	2.3 2.0	3.7 3.5	6.4 5.4	7.1 5.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

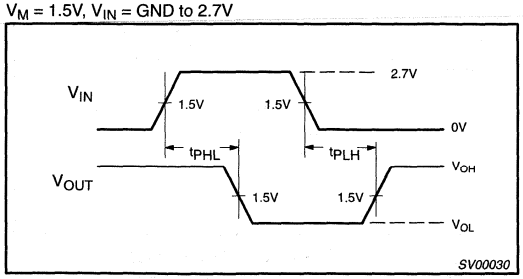
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

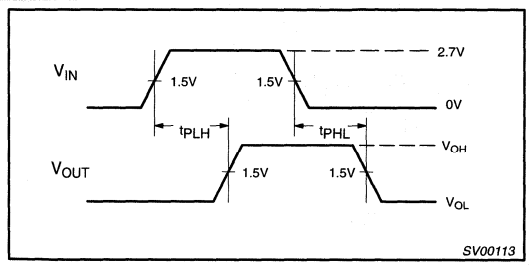
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	MAX	MIN	
t_s(H) t_s(L)	Setup time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	0 0.8		0 1.1	ns
t_h(H) t_h(L)	Hold time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	1.7 1.7		1.7 1.7	ns
t_s(H) t_s(L)	Setup time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	0 0.9		0 1.2	ns
t_h(H) t_h(L)	Hold time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	1.8 1.8		1.8 1.8	ns
t_w(L)	Latch enable pulse width, Low	3	3.3		3.3	ns

AC WAVEFORMS

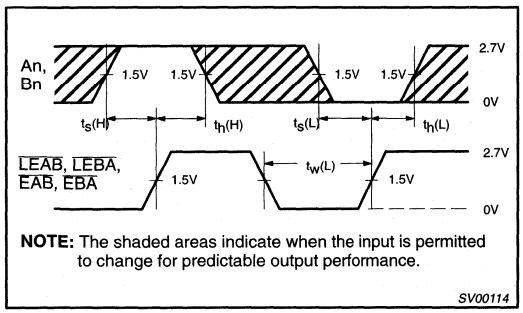
V_M = 1.5V, V_{IN} = GND to 2.7V



Waveform 1. Propagation Delay For Inverting Output

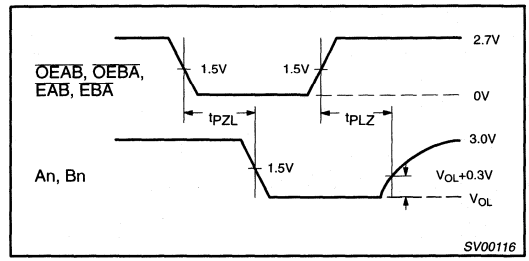


Waveform 2. Propagation Delay For Non-Inverting Output

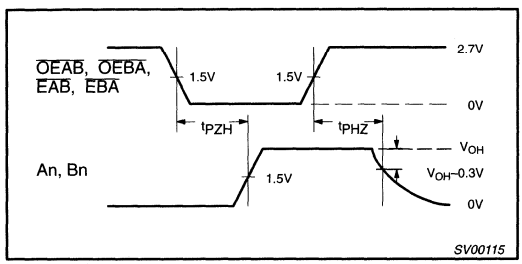


NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data Setup and Hold Times And Latch Enable Pulse Width

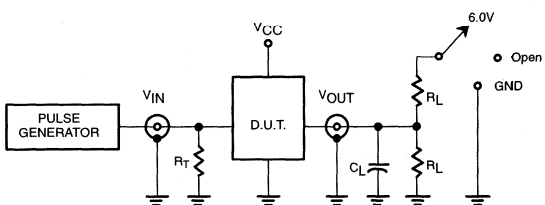


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

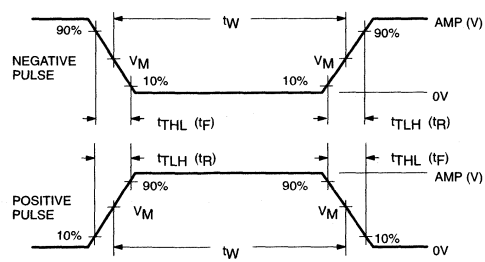


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal D-type transparent latch (3-State)

74LVT573

FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State output buffers
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- Power-up 3-State
- Power-up reset
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT573 is a high-performance BiCMOS product designed for VCC operation at 3.3V. This device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 74LVT573 has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

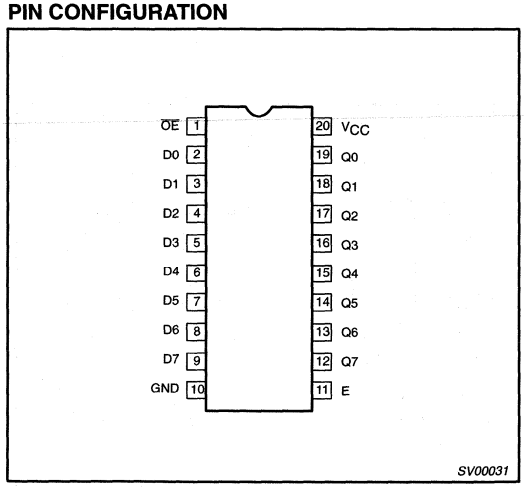
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 3.3V	2.5 2.7	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT573 D	74LVT573 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT573 DB	74LVT573 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT573 PW	74LVT573PW DH	SOT360-1

PIN CONFIGURATION



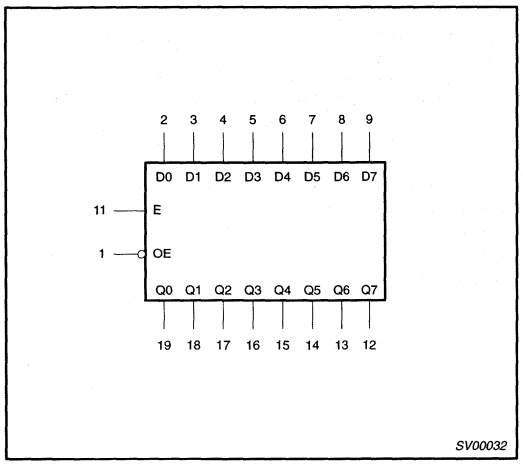
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

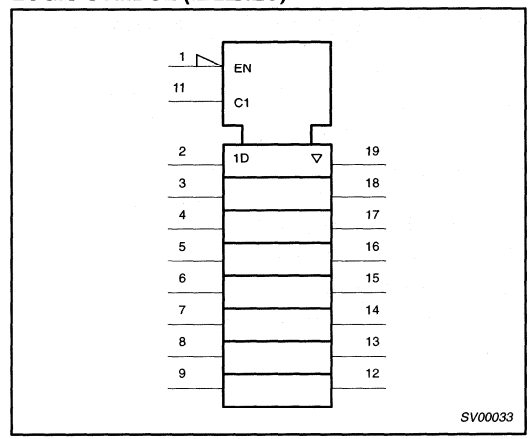
3.3V Octal D-type transparent latch (3-State)

74LVT573

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

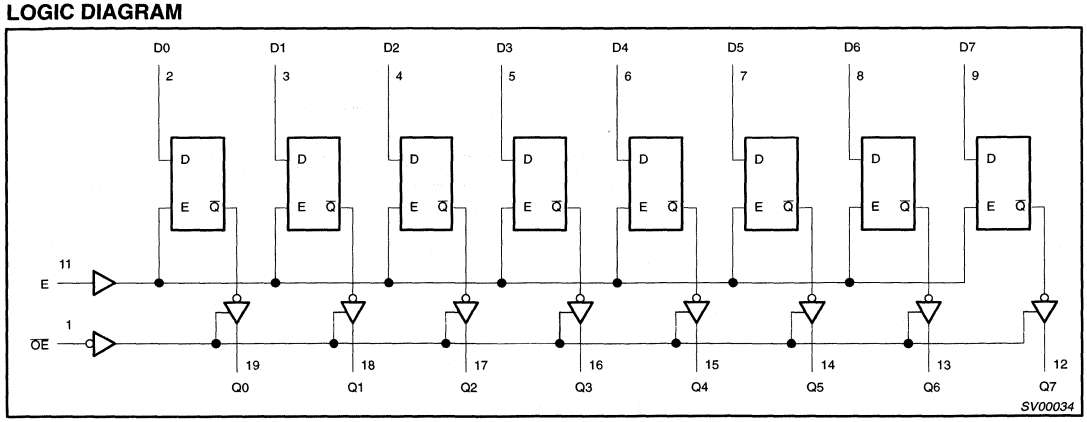


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn		Q0 – Q7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H	X	X	NC	Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC}= 3.6V; V_O = 3V; V_I = V_{IL} or V_{IH}			1	5	µA
I_{OZL}	3-State output Low current	V_{CC}= 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1	–5	
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	2	1.0 1.0	2.5 2.7	4.2 4.3	4.7 5.2	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	1	1.6 2.5	3.5 4.3	5.6 6.5	6.3 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.0 1.3	2.8 3.3	5.1 5.5	6.2 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	2.0 1.5	3.7 3.0	5.7 4.6	6.7 5.1	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

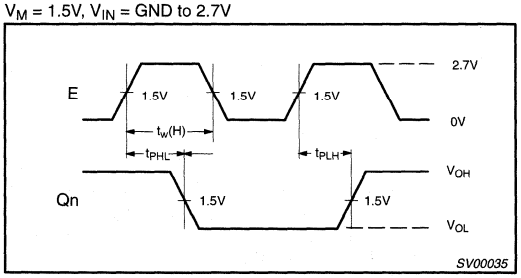
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

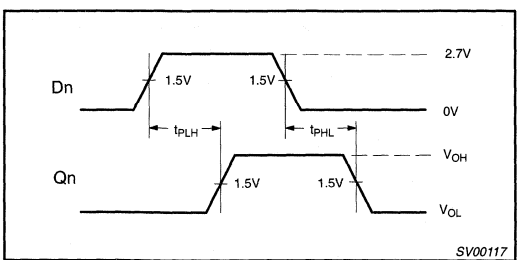
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V	
			MIN	MAX	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low, Dn to E	3	0.7 0.7		0.6 0.6	ns
$T_H(H)$ $T_H(L)$	Hold time, High or Low, Dn to E	3	1.6 1.6		1.8 1.8	ns
$T_W(H)$	E pulse width High	1	3.3		3.3	ns

AC WAVEFORMS

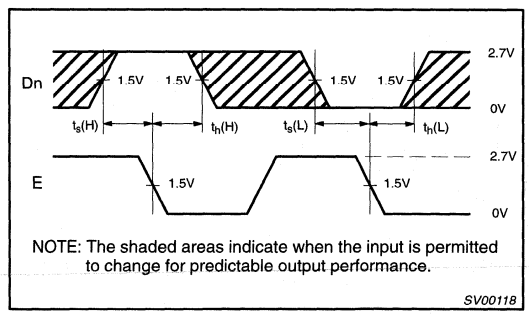
V_M = 1.5V, V_{IN} = GND to 2.7V



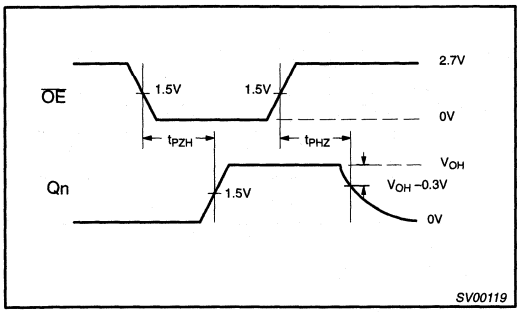
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



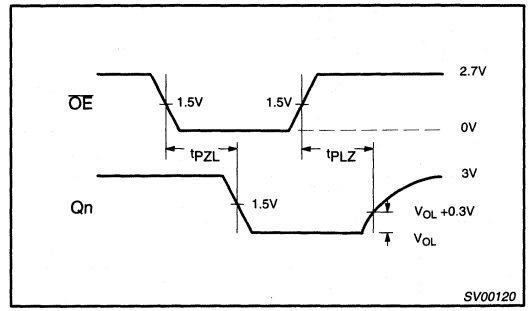
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

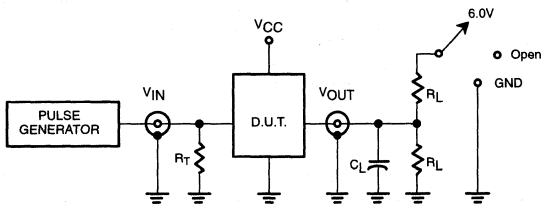


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

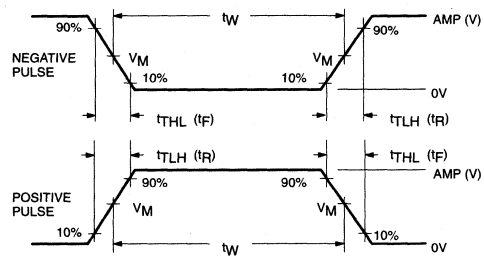


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal D-type flip-flop (3-State) 74LVT574

FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT574 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The state of each D input (one set-up time before the Low-to-High clock transition) is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "off" state, which means they will neither drive nor load the bus.

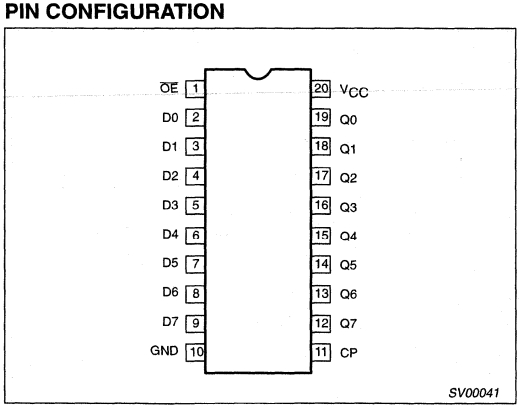
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 3.3V	3.6 4.3	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

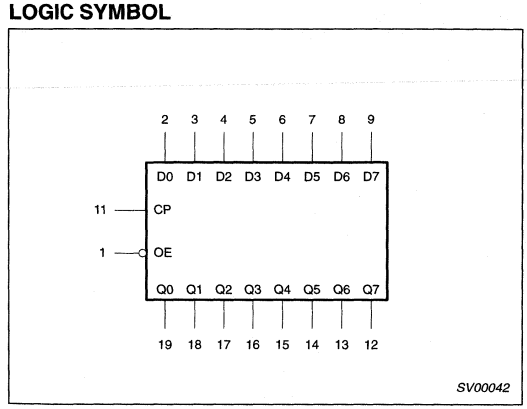
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT574 D	74LVT574 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT574 DB	74LVT574 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT574 PW	74LVT574PW DH	SOT360-1

PIN CONFIGURATION

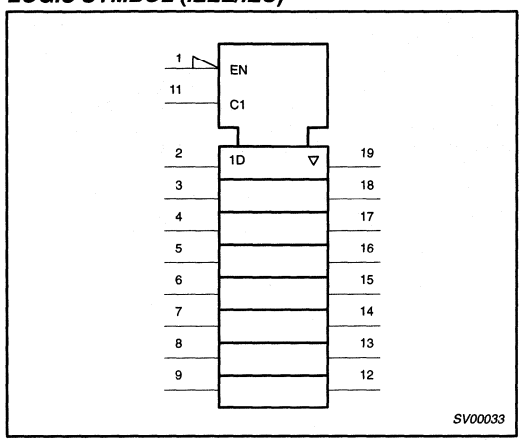


LOGIC SYMBOL



3.3V Octal D-type flip-flop (3-State) 74LVT574

LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

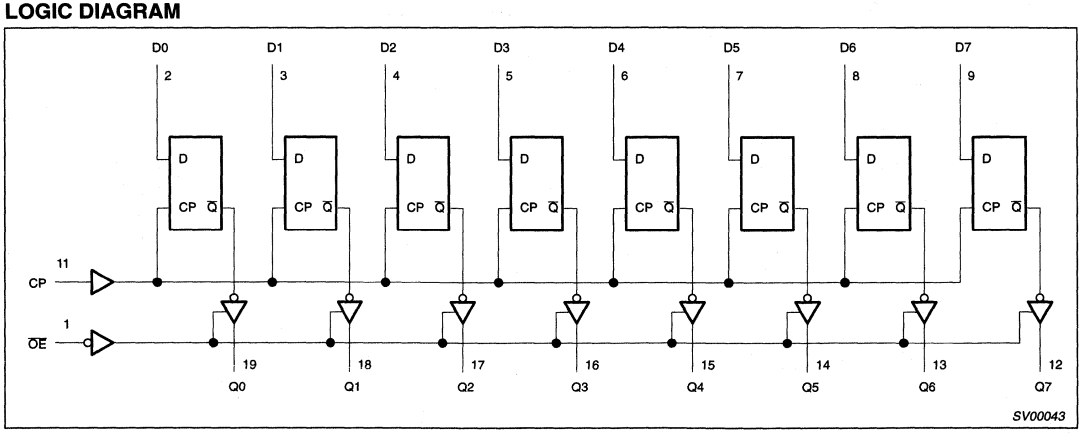
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING
$\overline{OE}$	CP	Dn	REGISTER	Q0 – Q7	MODE
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H	X	X	NC	Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage[3]		−0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC}= 3.6V; V_O = 3V; V_I = V_{IL} or V_{IH}			1	5	µA
I_{OZL}	3-State output Low current	V_{CC}= 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			1	–5	µA
I_{CCH}	Quiescent supply current[3]	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ± 0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MIN	MAX	UNIT
f_{MAX}	Maximum clock frequency	1	150			150		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.7 2.4	3.6 4.3	5.4 5.9		6.2 6.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.0 1.3	2.9 3.4	4.8 5.1		5.9 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.9 1.7	4.0 3.2	5.5 4.5		5.9 4.5	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

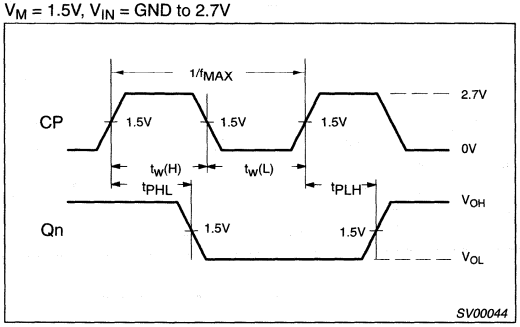
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

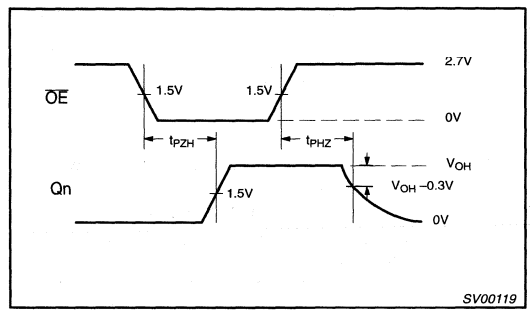
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V	
			MIN	MAX	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low, Dn to CP	2	2.0 2.0		2.4 2.4	ns
$T_H(H)$ $T_H(L)$	Hold time, High or Low, Dn to CP	2	0.3 0.3		0 0	ns
$T_W(H)$	CP pulse width High or Low	1	3.3 3.3		3.3 3.3	ns

AC WAVEFORMS

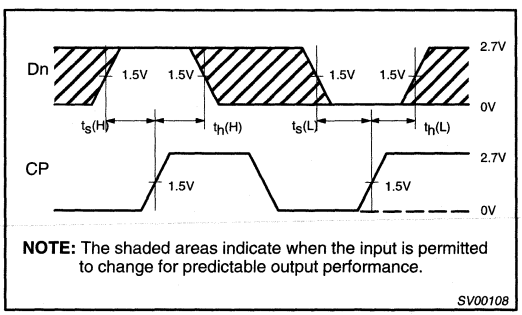
V_M = 1.5V, V_{IN} = GND to 2.7V



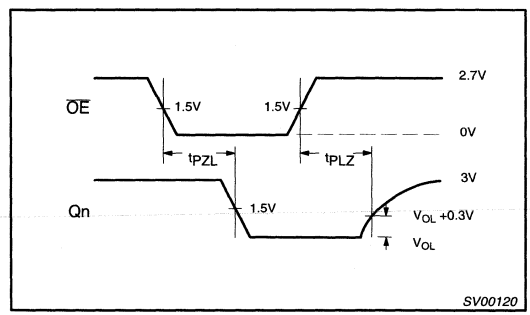
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

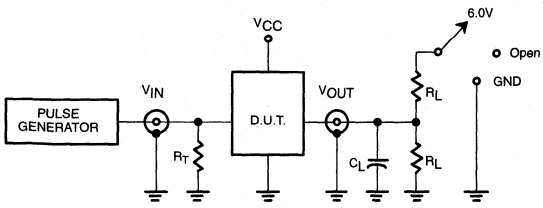


Waveform 2. Data Setup and Hold Times

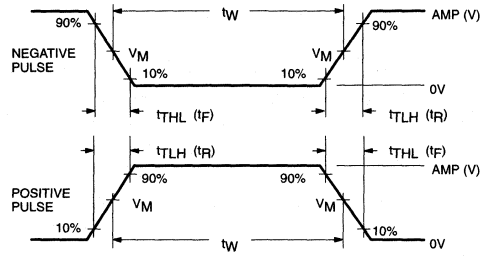


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal transceiver with direction pin; inverting (3-State)

74LVT640

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT640 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

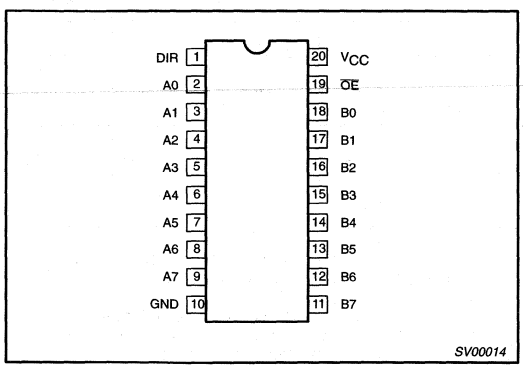
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.3 2.4	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic SO	–40°C to +85°C	74LVT640 D	74LVT640 D	SOT163-1
20-Pin Plastic SSOP	–40°C to +85°C	74LVT640 DB	74LVT640 DB	SOT339-1
20-Pin Plastic TSSOP	–40°C to +85°C	74LVT640 PW	74LVT640PW DH	SOT360-1

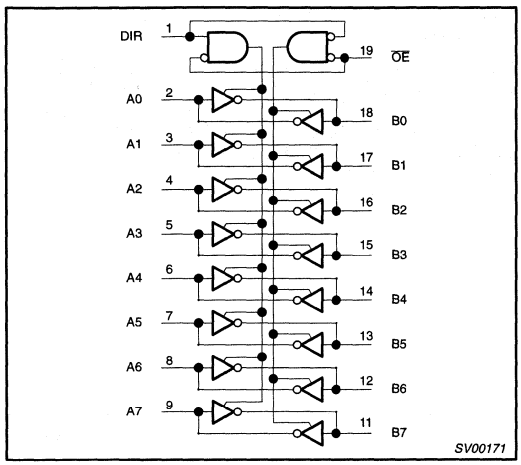
PIN CONFIGURATION



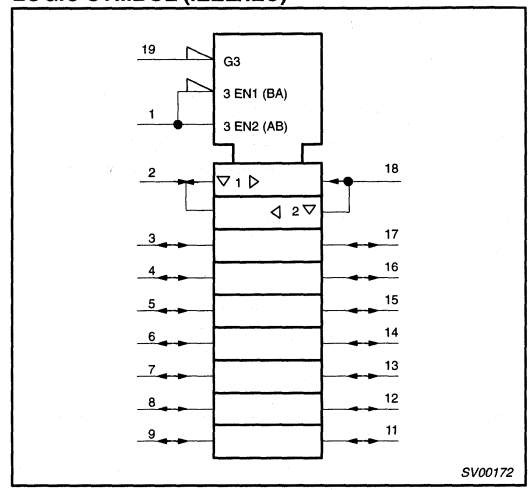
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active–Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}n$	DIR	An	Bn
L	L	$\overline{Bn}$	Inputs
L	H	Inputs	$\overline{An}$
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage[3]		−0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V	Control pins		1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±0.1	±1	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq 1.2V$; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = +25°C only.
4. Unused pins at V_{CC} or GND.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

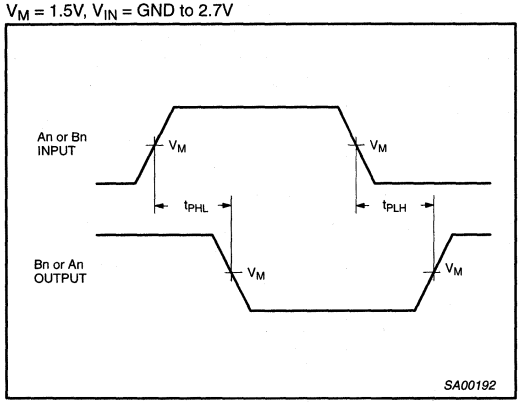
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V +0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.3 2.4	3.7 3.3	4.5 3.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.5	3.5 3.6	5.3 5.3	6.9 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	2.2 2.0	3.7 3.1	5.0 4.5	5.6 4.5	ns

NOTES:

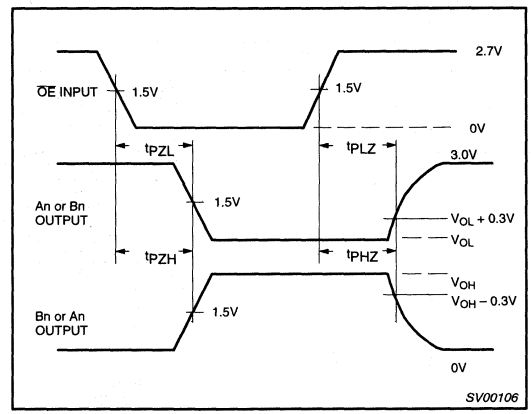
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

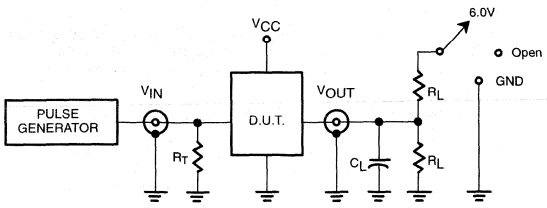


Waveform 1. Input (An or Bn) to Output (Bn or An) Propagation Delays

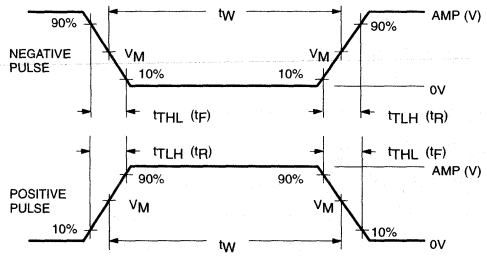


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal bus transceiver/register (3-State) 74LVT646

FEATURES

- Combines 74LVT245 and 74LVT574 type functions in one device
- Independent registers for A and B buses
- Multiplexed real–time and stored data
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- Power-up 3-State
- Power-up reset
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT646 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High.

Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (Low).

In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74LVT646.

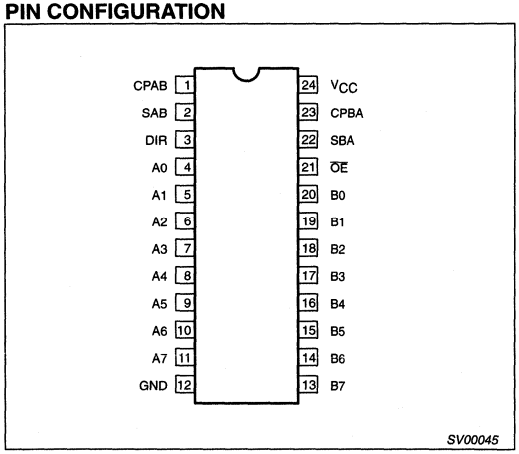
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.8 2.7	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	$V_{I/O}$ = 0V or 3.0V	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic SOL	–40°C to +85°C	74LVT646 D	74LVT646 D	SOT163-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT646 DB	74LVT646 DB	SOT399-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT646 PW	74LVT646PW DH	SOT360-1

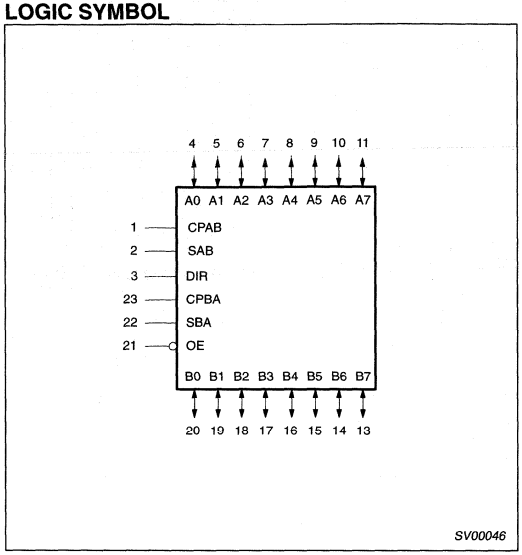
PIN CONFIGURATION



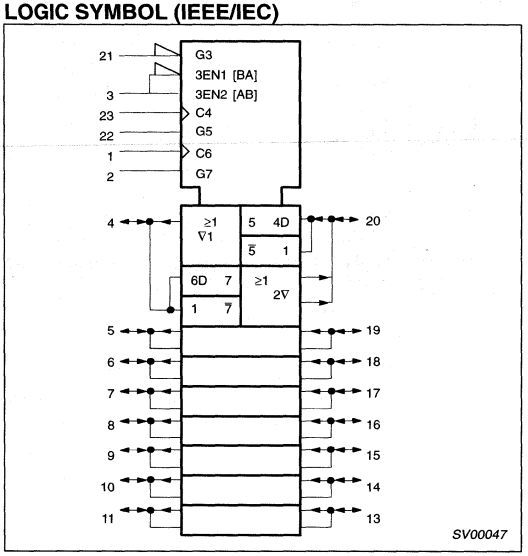
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

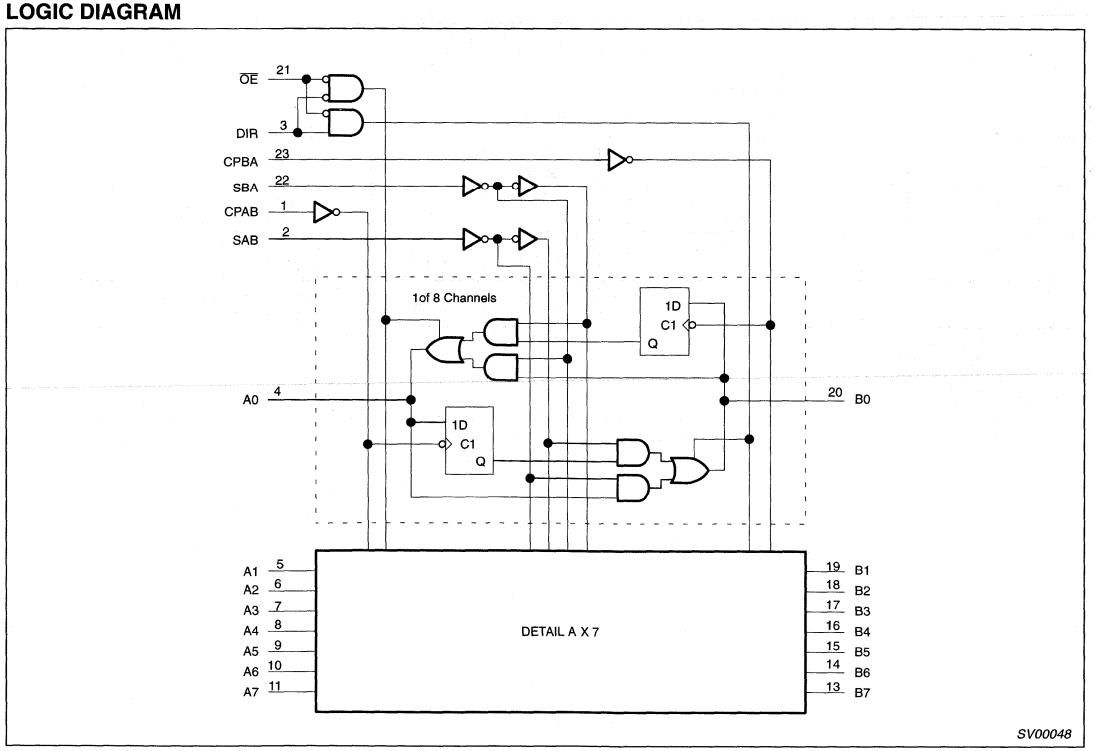
LOGIC SYMBOL

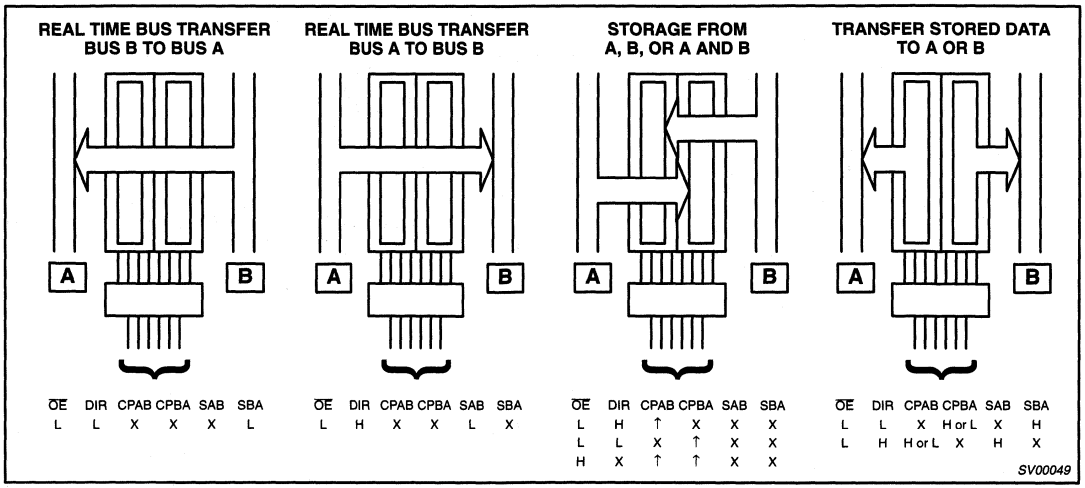


LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM





FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP NO TAG	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low–level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE =Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	180			MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.8 2.1	3.8 3.8	5.7 5.7	6.7 6.4	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.3 1.0	2.8 2.7	4.7 4.6	5.4 5.3	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	2 3	1.4 1.4	3.7 3.8	6.2 6.2	7.2 6.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	5 6	1.0 1.0	4.0 4.1	5.8 6.0	7.2 7.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	5 6	2.3 2.2	4.3 3.8	6.5 5.8	6.9 5.9	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	5 6	1.0 1.2	3.4 3.4	6.5 6.3	7.5 7.1	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	5 6	1.7 1.5	4.1 3.5	7.2 5.8	8.1 6.3	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS

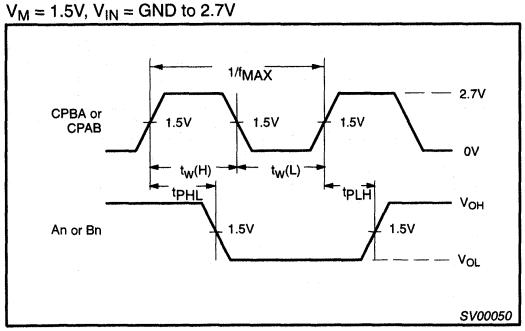
GND = 0V, t_R =2.5ns, t_F = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V± 0.3V		V_{CC} = 2.7V	
			Min	Typ	Min	
t_s(H) t_s(L)	Setup time[1] An to CPAB, Bn to CPBA	4	1.5 2.0	1.0 1.0	1.6 2.4	ns
t_h(H) t_h(L)	Hold time[1] An to CPAB, Bn to CPBA	4	0.0 0.0	–1.0 –1.0	0.0 0.0	ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	1	3.3 3.3	1.0 2.0	3.3 3.3	ns

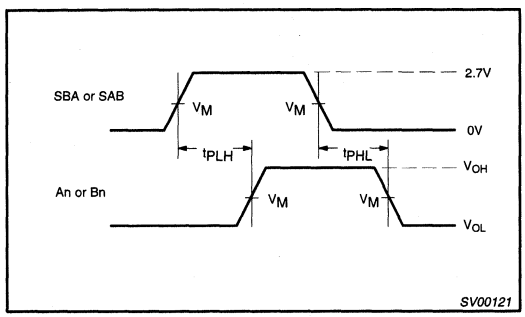
NOTE:
1. This data sheet limit may vary among suppliers.

AC WAVEFORMS

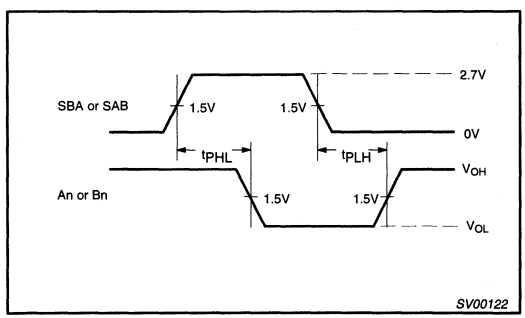
V_M = 1.5V, V_{IN} = GND to 2.7V



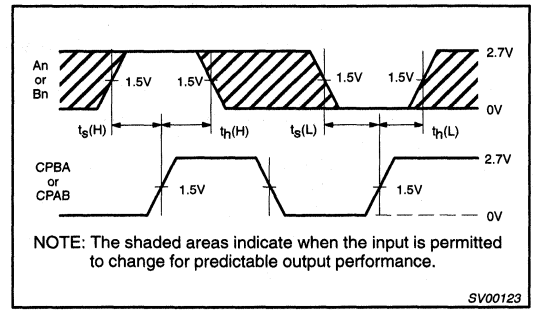
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



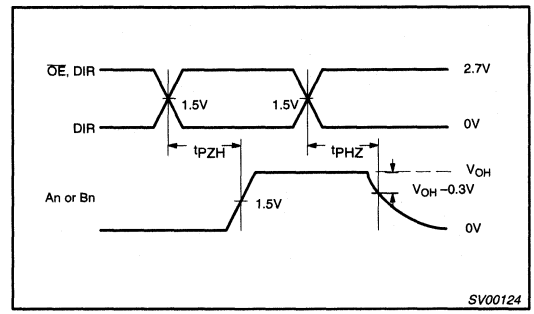
Waveform 2. Propagation Delay, SAB to Bn or SBA to An, An to Bn or Bn to An



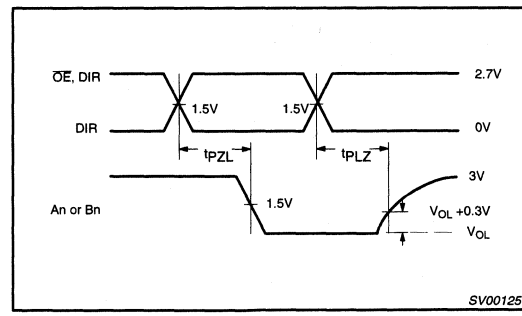
Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times

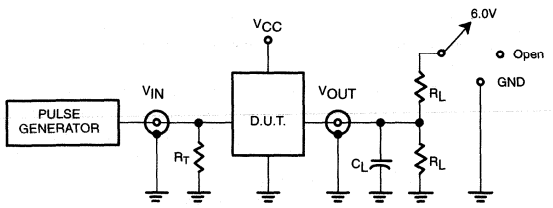


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

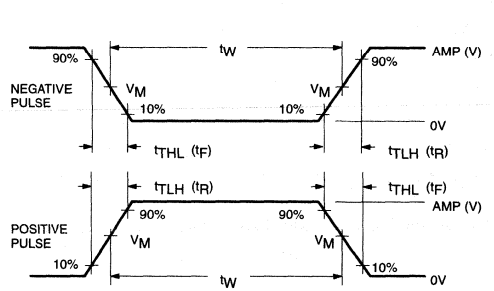


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

3.3V Octal transceiver/register, non-inverting (3-State)

74LVT652

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch–up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT652 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT652 transceiver/register consists of bus transceiver circuits with 3-State outputs, D–type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

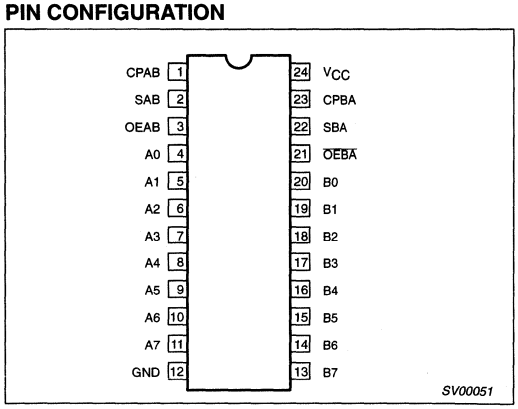
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.8 2.6	ns
C_{IN}	Input capacitance	V_I = 0V or 3V	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic SOL	–40°C to +85°C	74LVT652 D	74LVT652 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT652 DB	74LVT652 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT652 PW	74LVT652PW DH	SOT355-1

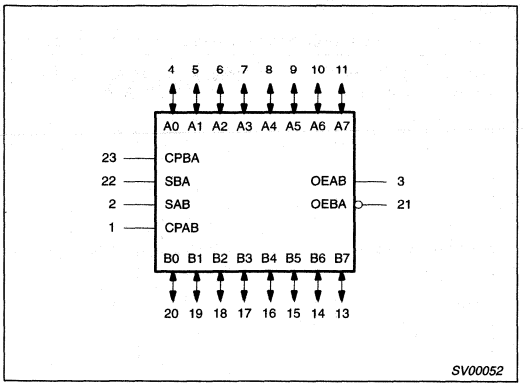
PIN CONFIGURATION



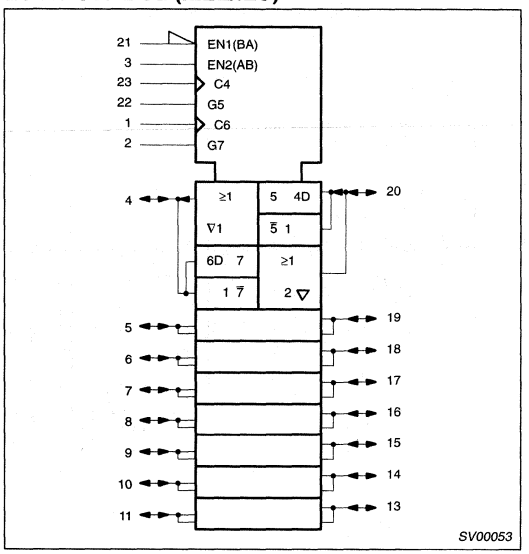
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / $\overline{OEBA}$	A to B Output Enable input (active-High) / B to A Output Enable input (active-Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

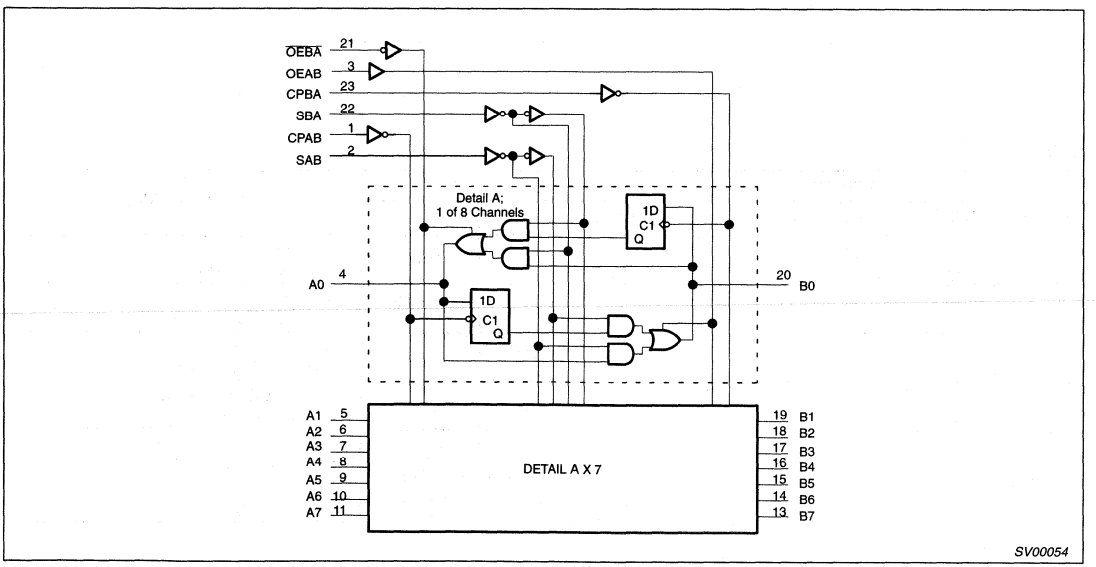
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



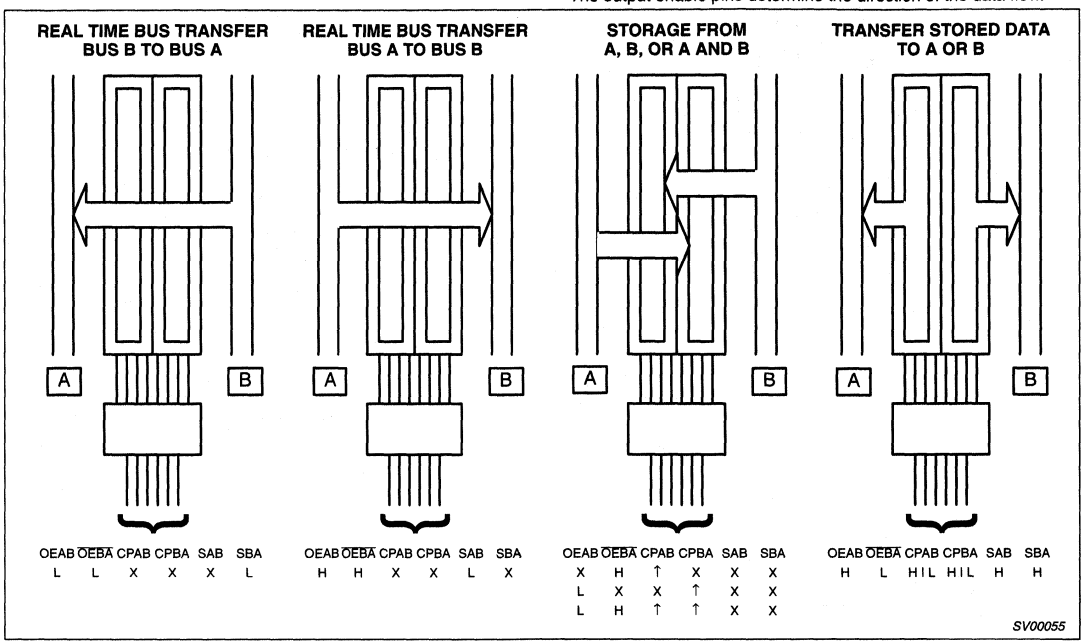
LOGIC DIAGRAM



The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74LVT652.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified** Output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified** Output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			1.0	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1.0	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	180			MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.8 2.0	3.7 3.7	6.0 5.7	6.9 6.4	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.2 1.0	2.8 2.6	4.7 4.6	5.5 5.3	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	3	1.4 1.4	3.7 4.0	6.4 6.2	7.6 6.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	5 6	1.0 1.0	2.9 3.0	5.8 6.0	7.2 7.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	5 6	2.2 1.8	3.9 3.2	6.5 5.8	6.9 5.9	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	5 6	1.0 1.2	3.3 3.4	6.5 6.3	7.5 7.1	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	5 6	1.7 1.5	4.5 3.8	7.2 5.8	8.1 6.3	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS

GND = 0V, t_R = 2.5ns, t_F = 2.5ns, C_L = 50pF, R_L = 500Ω, T_{amb} =40 °C to 85 °C

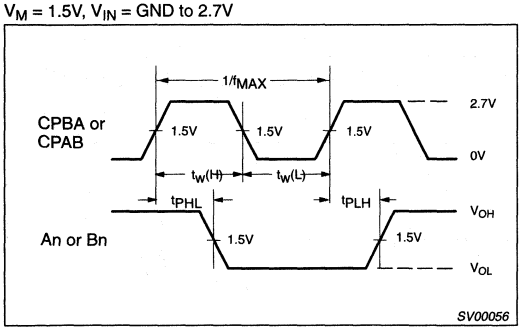
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time [1] An to CPAB, Bn to CPBA	4	1.5 2.2	0.9 1.1		1.6 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time [1] An to CPAB, Bn to CPBA	4	0 0	–1.0 –1.0		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	1	3.3 3.3	1.0 2.0		3.3 3.3		ns

NOTE:

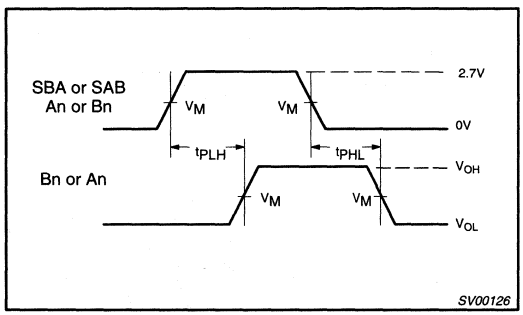
1. This data sheet limit may vary among suppliers.

AC WAVEFORMS

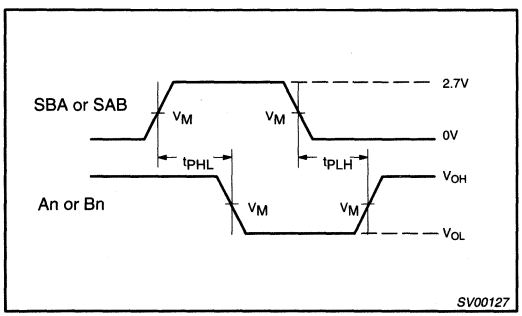
V_M = 1.5V, V_{IN} = GND to 2.7V



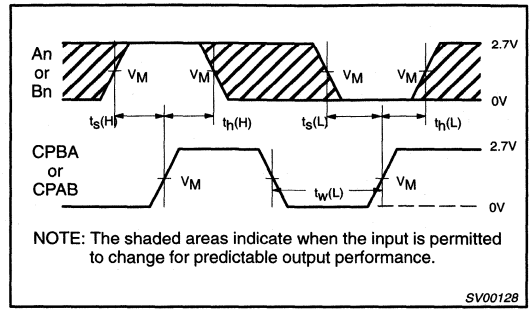
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



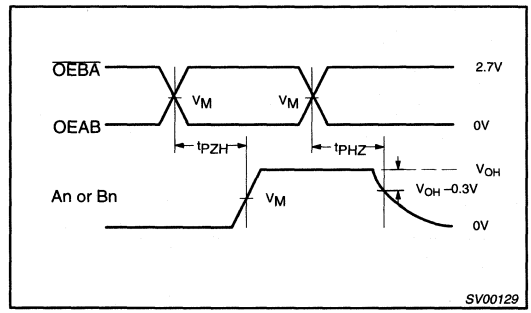
Waveform 2. Propagation Delay, An to Bn or Bn to An, SAB to Bn or SBA to An



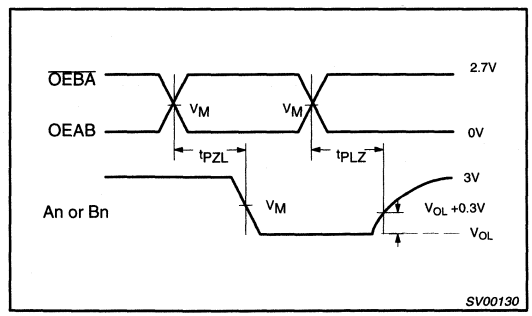
Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times

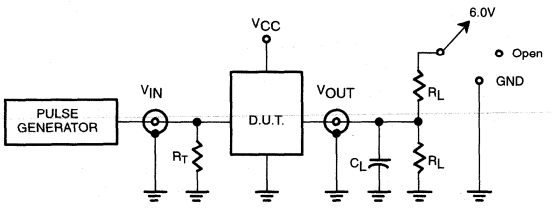


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

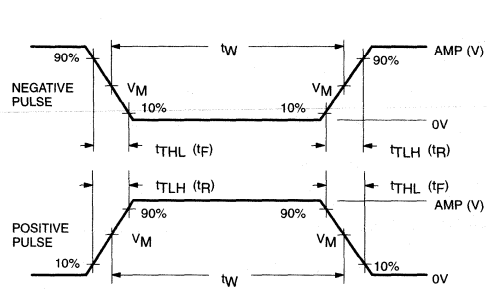


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV00092

3.3V Octal registered transceiver (3-State) 74LVT2952

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT2952 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses.

Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

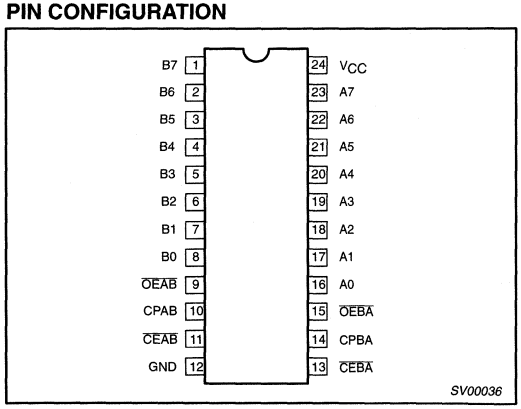
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50pF; V_{CC} = 3.3V	3.1 3.8	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic SOL	–40°C to +85°C	74LVT2952 D	74LVT2952 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT2952 DB	74LVT2952 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT2952 PW	7LVT2952PW DH	SOT355-1

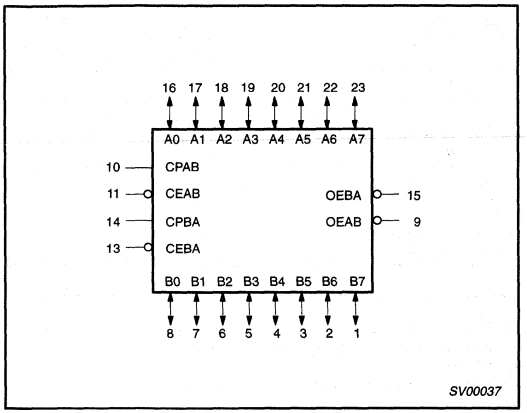
PIN CONFIGURATION



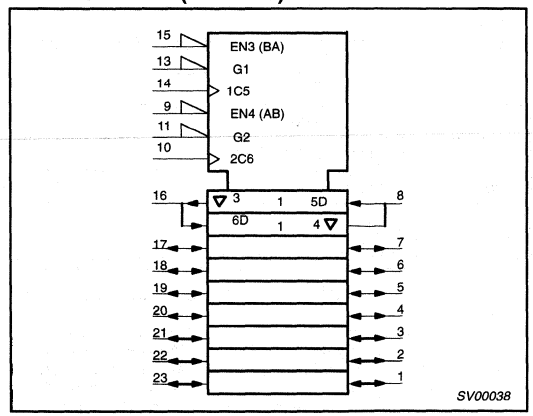
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
8, 7, 6, 5, 4, 3, 2, 1	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Output enable inputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

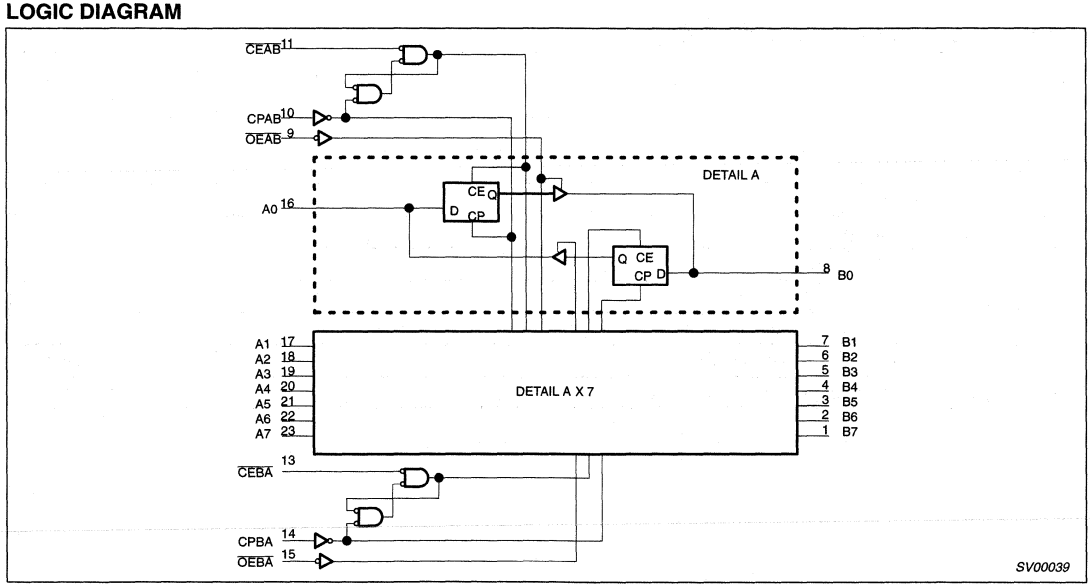
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OEXX}$			
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–64	mA
		Output in Low state	128	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}–0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1.0	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1.0	
		V_{CC} = 3.6V; V_I = 0			–1	-5.0	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} – 0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at V_{CC} = 0.6V.
3. This parameter is valid for any V_{CC} between 0V and 1.3V with a transition time of up to 10msec. From V_{CC} = 1.3V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	200			MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	1	1.3 1.8	3.1 3.8	6.1 6.0	7.1 6.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	3 4	1.0 1.2	3.4 3.6	5.6 6.5	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	3 4	1.0 1.6	3.7 3.4	6.3 5.1	6.9 5.3	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

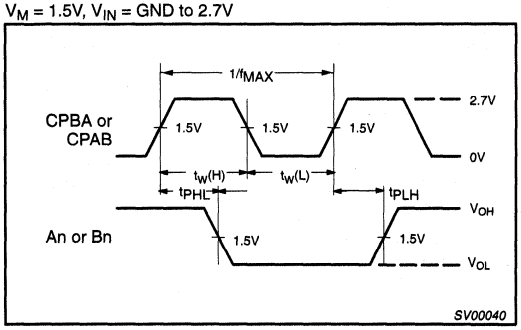
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

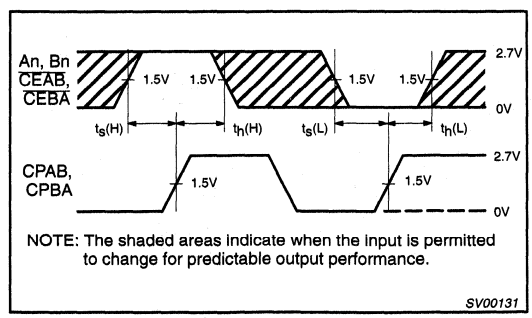
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V	
			MIN	TYP[1]	MIN	
t_s(H) t_s(L)	Setup time An to CPAB or Bn to CPBA	2	2.5 2.5	1 1	2.8 3.0	ns
t_h(H) t_h(L)	Hold time An to CPAB ro Bn to CPBA	2	1.5 2.5	–0.5 –0.5	0.7 2.6	ns
t_s(H) t_s(L)	Setup time $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA	2	0.9 2.4	0.3 –0.3	0.8 2.7	ns
t_h(H) t_h(L)	Hold time $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA	2	1.5 2.5	0.3 0	0.7 2.6	ns
t_W(H) t_W(L)	CPAB or CPBA pulse width High or Low	1	3.3 3.3	1 1	3.3 3.3	ns

AC WAVEFORMS

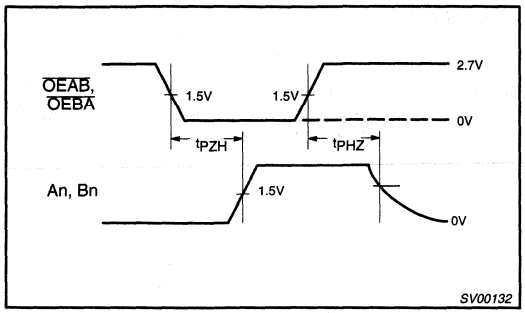
V_M = 1.5V, V_{IN} = GND to 2.7V



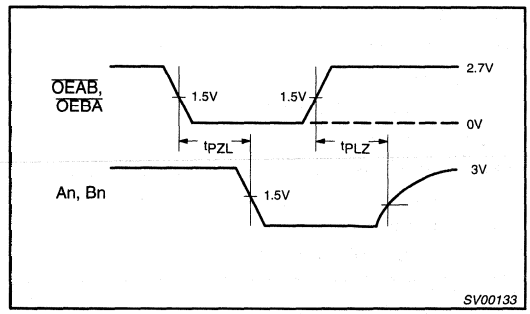
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

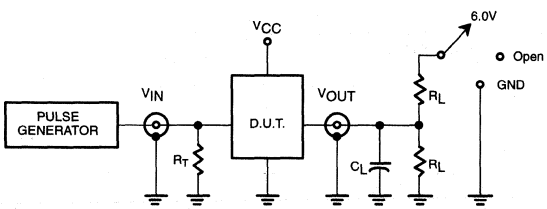


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

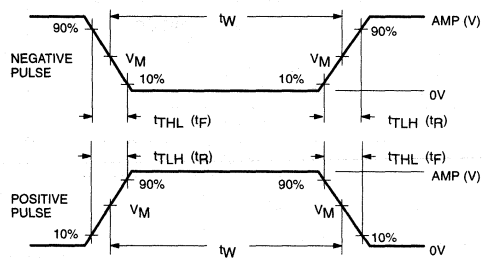


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV00092

3.3V 16-bit inverting buffer/driver (3-State) 74LVT16240A

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16240A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

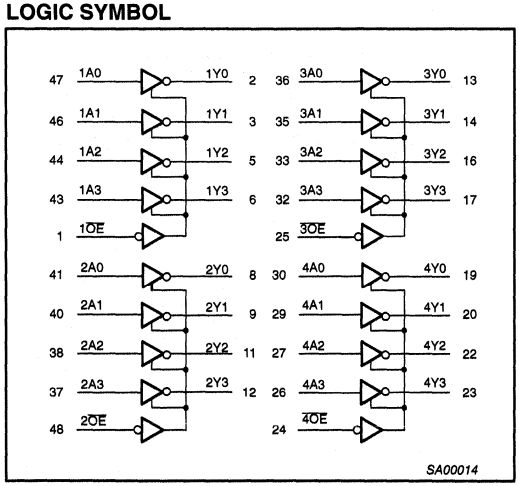
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

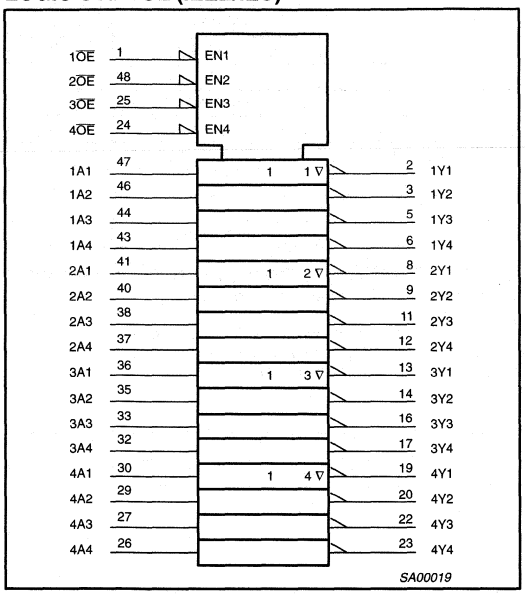
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16240A DL	VT16240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16240A DGG	VT16240A DGG	SOT362-1

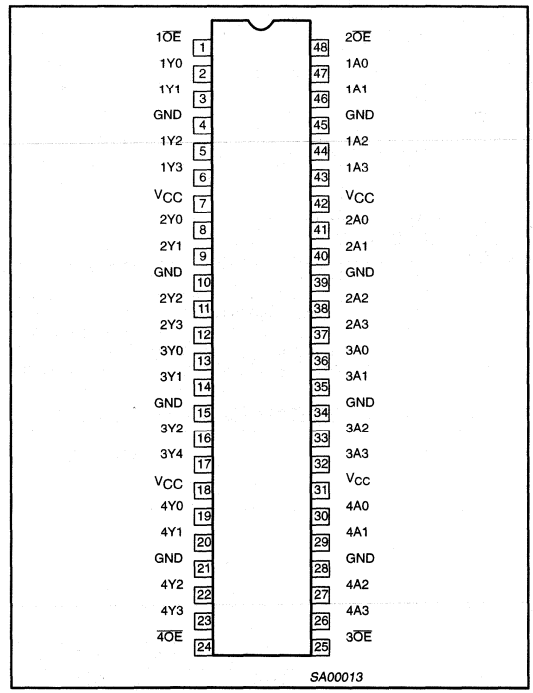
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0-1$\overline{Y}$3 2$\overline{Y}$0-2$\overline{Y}$3 3$\overline{Y}$0-3$\overline{Y}$3 4$\overline{Y}$0-4$\overline{Y}$3	Data outputs
1, 48, 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Outputs
n$\overline{OE}$	nAx	n$\overline{Y}$x
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = -18mA			–0.85	1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = -100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = -8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = -32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.03	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.30	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.40	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1.0	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.4	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			-0.4	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	135		µA
		V_{CC} = 3V; V_I = 2.0V		-75	-135		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	-5	
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.0	6.0	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.20	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

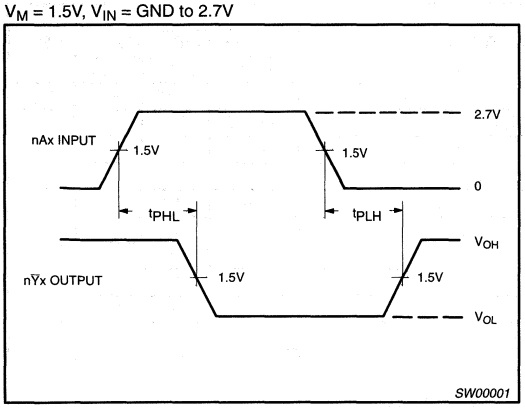
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	0.5 0.5	1.8 2.0	3.2 3.2	4.0 4.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.3 2.1	4.0 4.4	5.0 4.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.0 1.0	3.2 3.0	4.5 4.4	5.0 4.8	ns

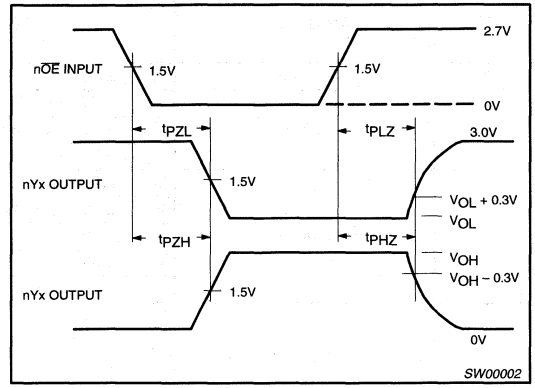
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

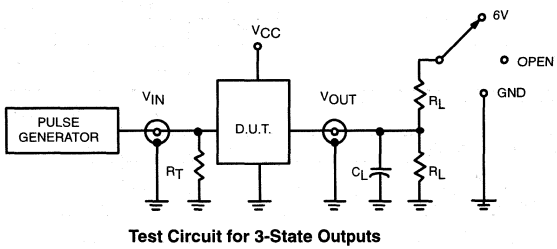


Waveform 1. Input (nAx) to Output (nȲx) Propagation Delays

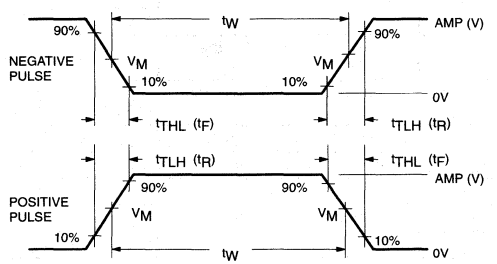


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit inverting buffer/driver with 30Ω termination resistors (3-State)

74LVT162240A

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same part as 74LVT16240A-1

DESCRIPTION

The 74LVT162240A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

The 74LVT162240A is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

The 74LVT162240A is the same as the 74LVT16240A-1. The part number has been changed to reflect industry standards.

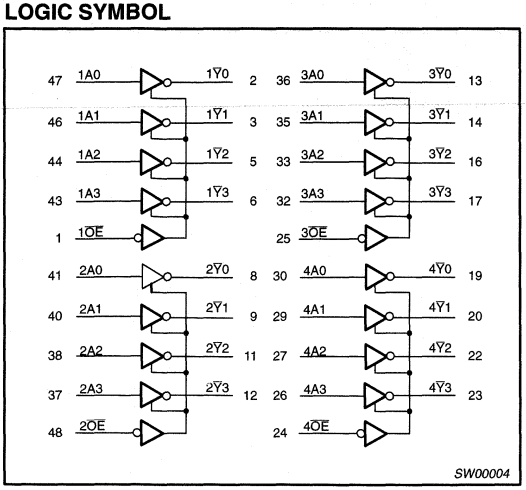
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 3.3V	2.6	ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT162240A DL	VT162240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT162240A DGG	VT162240A DGG	SOT362-1

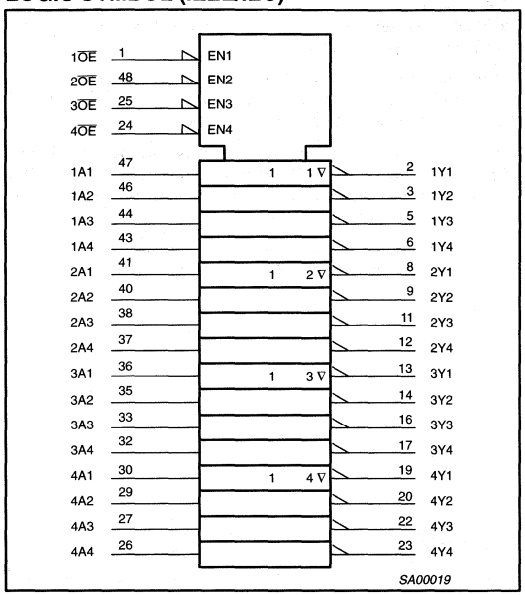
LOGIC SYMBOL



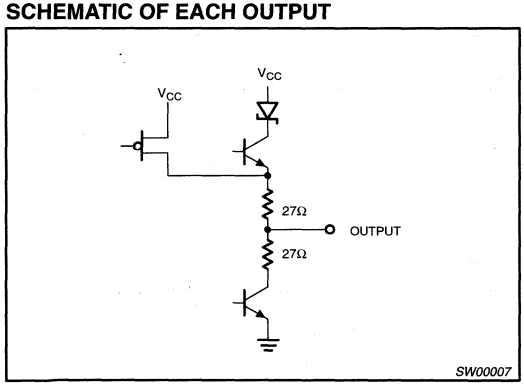
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0 - 1A3 2A0 - 2A3 3A0 - 3A3 4A0 - 4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0 - 1$\overline{Y}$3 2$\overline{Y}$0 - 2$\overline{Y}$3 3$\overline{Y}$0 - 3$\overline{Y}$3 4$\overline{Y}$0 - 4$\overline{Y}$3	Data outputs
1, 48 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

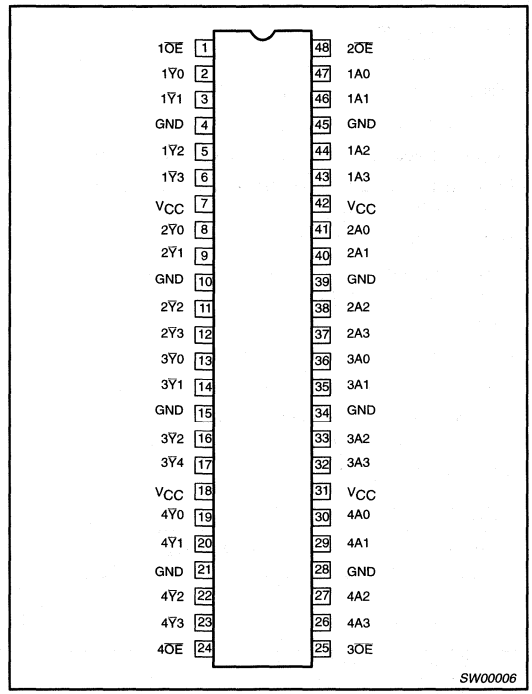
LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



PIN CONFIGURATION



FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	$n\overline{Y}x$
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-12	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = -18mA			–0.85	1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = -12mA		2.0			V
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA				0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.4	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			-0.4	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A outputs[6]	V_{CC} = 3V; V_I = 0.8V		75	135		µA
		V_{CC} = 3V; V_I = 2.0V		-75	-135		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	-5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.0	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.20	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

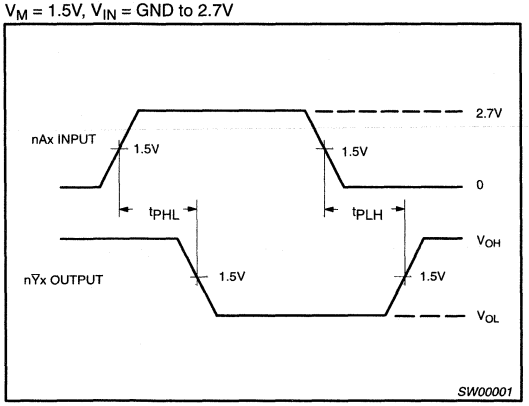
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	0.5 0.5	2.6 2.6	4.2 4.2	5.0 5.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.3 3.0	5.5 5.0	6.5 5.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.0 1.0	3.5 3.2	5.0 4.5	5.5 4.5	ns

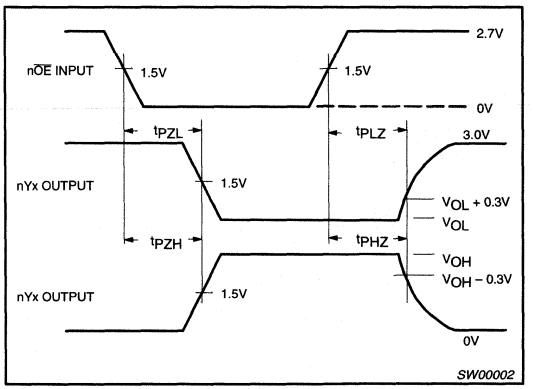
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

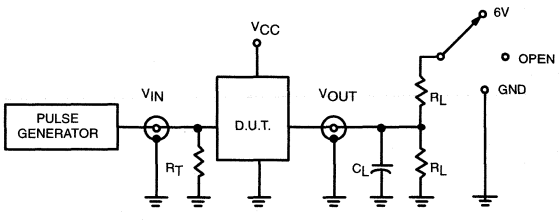


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

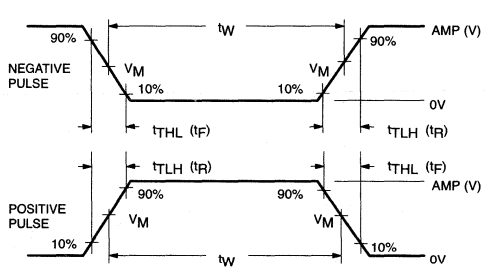


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit buffer/driver (3-State) 74LVT16244B

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16244B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-State bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

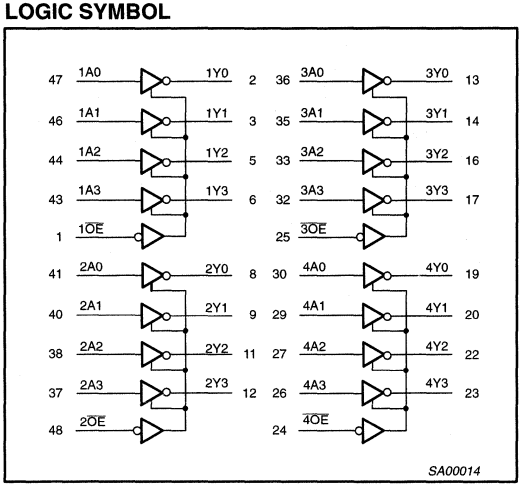
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	1.8	ns
C_{IN}	Input capacitance $n\overline{OE}$	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

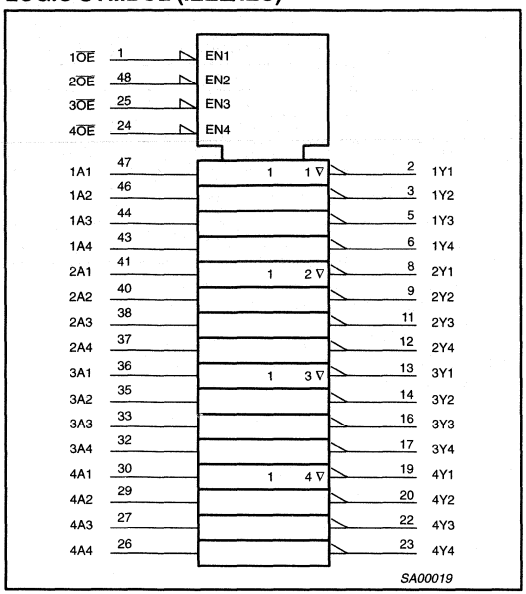
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16244B DL	VT16244B DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16244B DGG	VT16244B DGG	SOT362-1

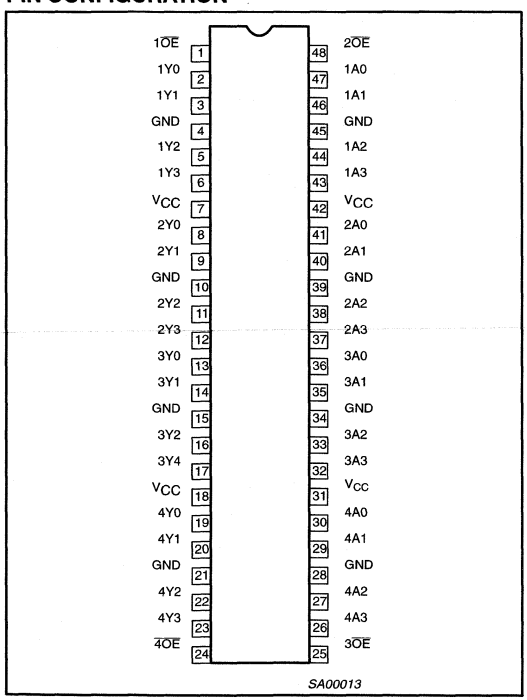
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 - 1A3, 2A0 - 2A3, 3A0 - 3A3, 4A0 - 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 - 1Y3, 2Y0 - 2Y3, 3Y0 - 3Y3, 4Y0 - 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = -18mA			-0.85	-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = -100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = -8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = -32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1.0	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.4	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			-0.4	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	135		µA
		V_{CC} = 3V; V_I = 2.0V		-75	-135		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	-5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.0	6.0	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

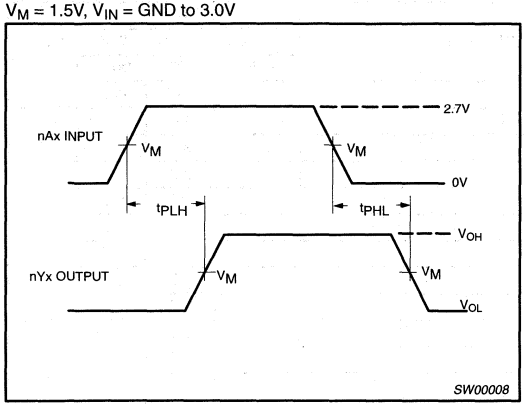
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	1.8 1.7	3.2 3.2	4.0 4.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.3 2.1	4.0 4.0	5.0 5.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.0 1.0	3.2 2.9	4.5 4.0	5.0 4.4	ns

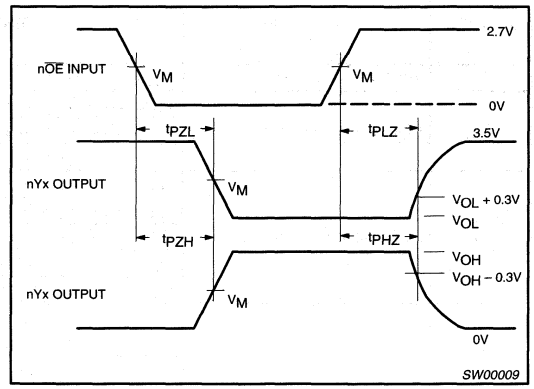
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

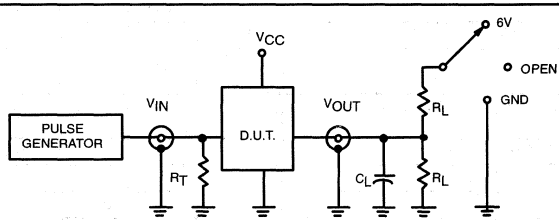


Waveform 1. Input (nAx) to Output (nȲx) Propagation Delays

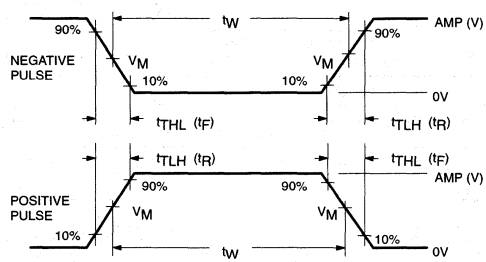


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit buffer/driver with 30Ω termination resistors (3-State)

74LVT162244B

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external terminating resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same part as 74LVT16244B-1

DESCRIPTION

The 74LVT162244B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

The 74LVT162244B is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

This device is a 16-bit buffer and line driver featuring non-inverting 3-State bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

The 74LVT162244B is the same as the 74LVT16244B-1. The part number has been changed to reflect industry standards.

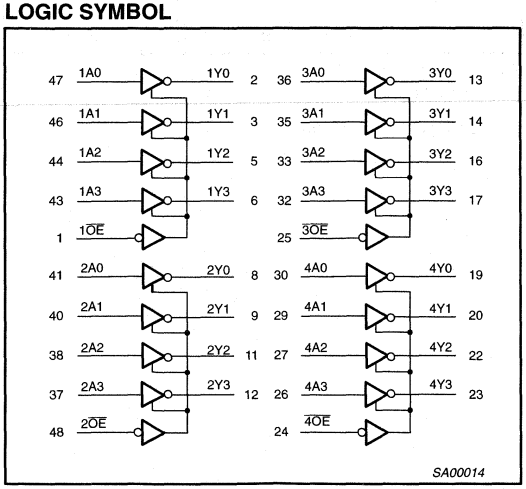
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	2.8	ns
C_{IN}	Input capacitance $n\overline{OE}$	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT162244B DL	VT162244B DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT162244B DGG	VT162244B DGG	SOT362-1

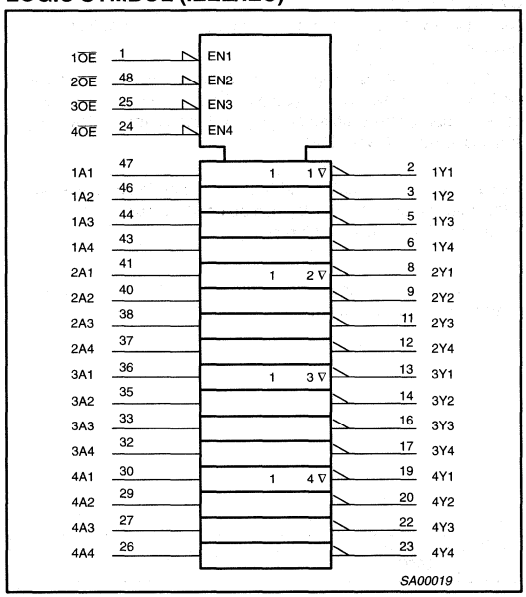
LOGIC SYMBOL



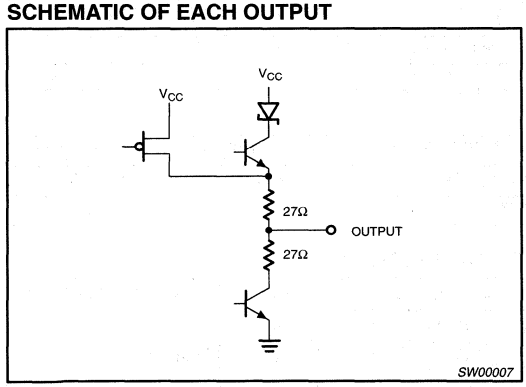
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 - 1A3, 2A0 - 2A3, 3A0 - 3A3, 4A0 - 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 - 1Y3, 2Y0 - 2Y3, 3Y0 - 3Y3, 4Y0 - 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

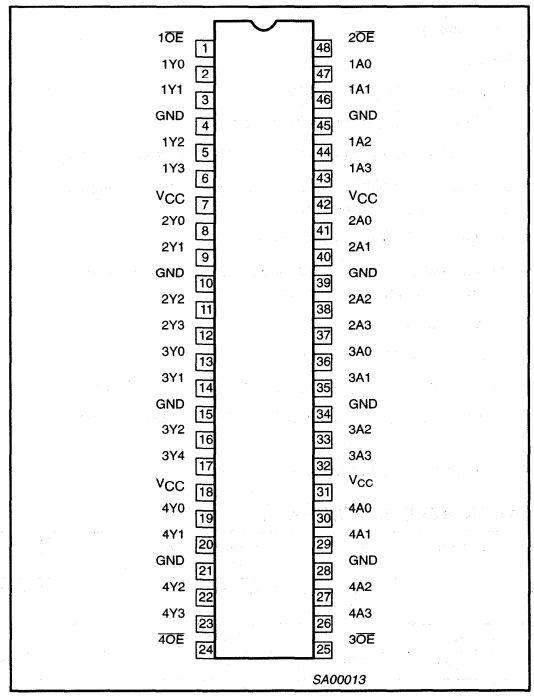
LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



PIN CONFIGURATION



FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-12	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = -18mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = -12mA		2.0			V
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA				0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1.0	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.4	10	µA
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		*0.1*	*1*	µA
		V_{CC} = 3.6V; V_I = 0	Data pins[4]		-0.4	-5	µA
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	135		µA
		V_{CC} = 3V; V_I = 2.0V		-75	-135		µA
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	-5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.0	6.0	mA
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.12	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

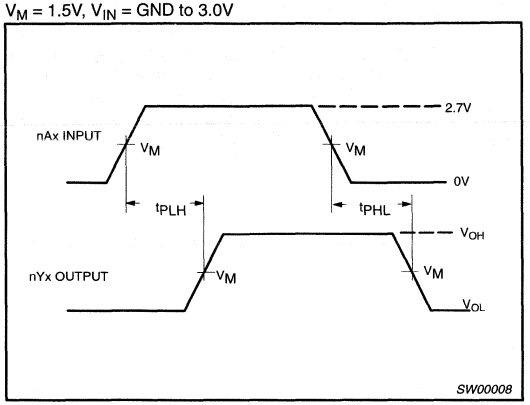
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	2.8 2.5	4.2 4.2	5.0 5.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.5 3.1	5.5 5.5	7.0 6.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.0 1.0	3.6 3.1	5.5 5.5	6.0 6.0	ns

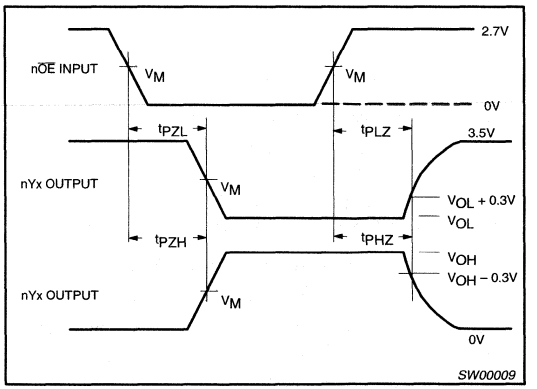
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

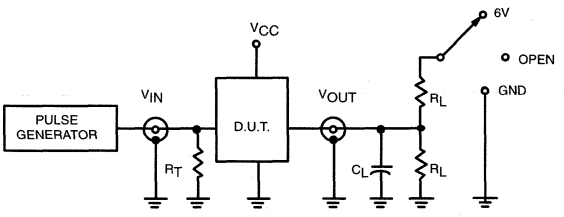


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

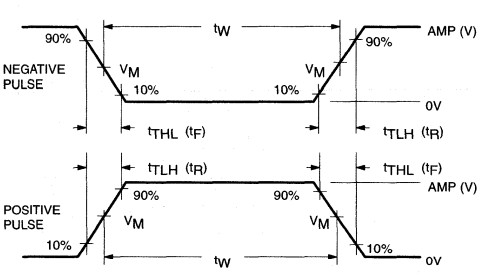


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit transceiver (3-State) 74LVT16245B

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16245B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

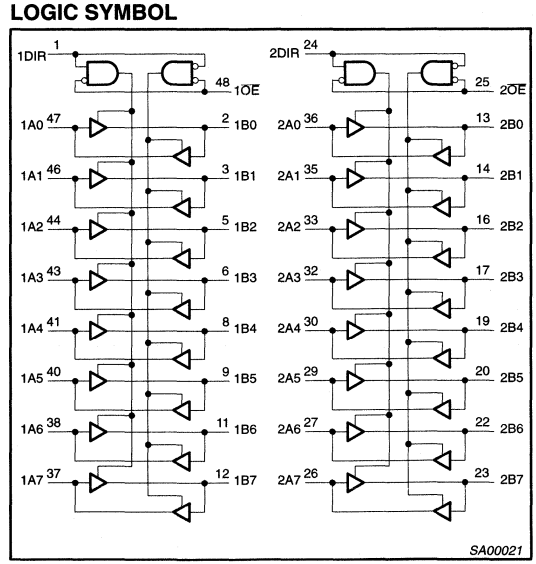
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16245B DL	VT16245B DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16245B DGG	VT16245B DGG	SOT362-1

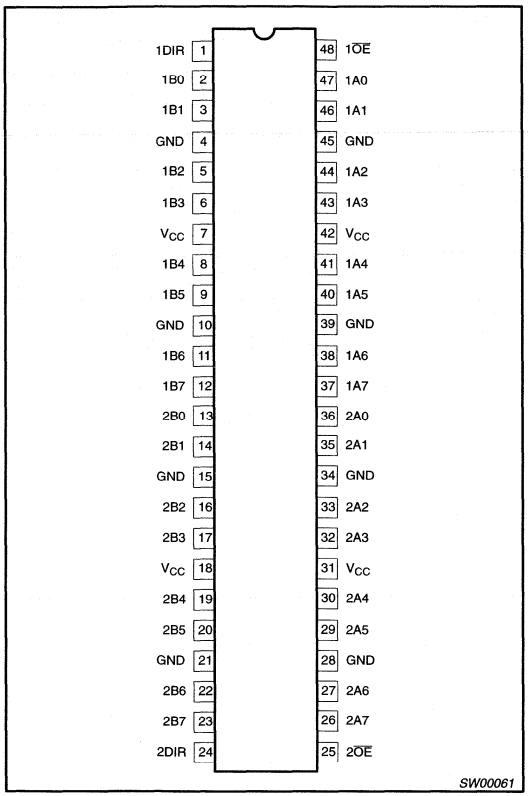
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	n$\overline{OE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

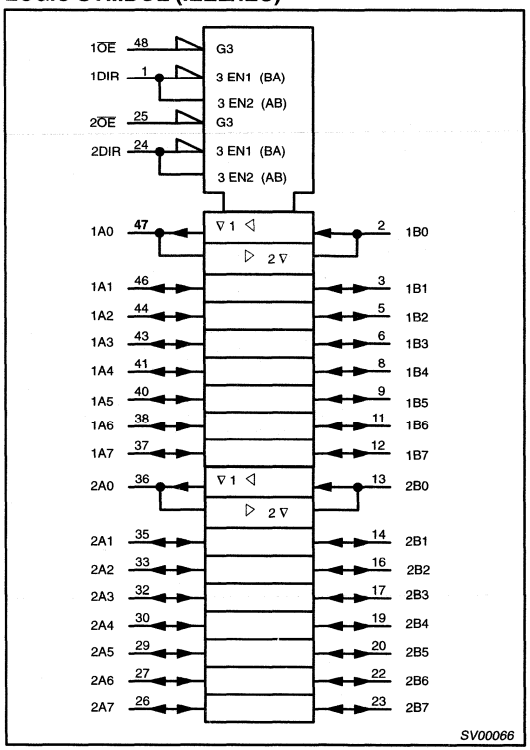
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
nOE	nDIR	nAx	nBx
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage[3]		−0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B outputs[6]	V_{CC} = 3V; V_I = 0.8V		75	135		µA
		V_{CC} = 3V; V_I = 2.0V		-75	-135		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			75	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.7	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

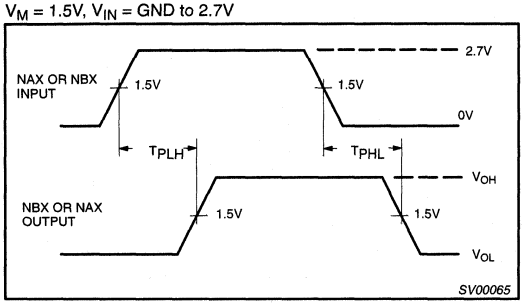
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V +0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.0 1.0	1.9 1.7	3.3 3.3	3.5 3.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.8 2.8	4.5 4.1	5.3 5.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.2 3.0	5.1 4.6	5.7 4.6	ns

NOTE:

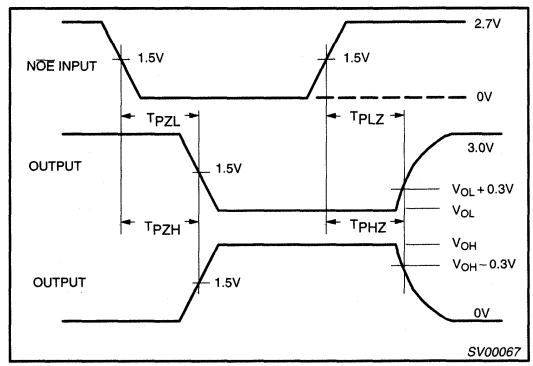
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

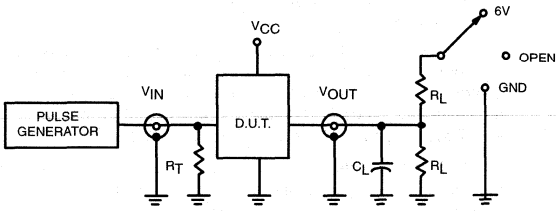


Waveform 1. Input to Output Propagation Delays

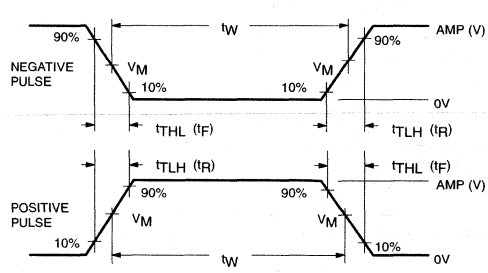


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit transceiver with 30Ω termination resistors (3-State)

74LVT162245B

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same part as 74LVT16245B-1

DESCRIPTION

The 74LVT162245B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($n\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

The 74LVT162245B is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74LVT162245B is the same as the 74LVT16245B-1. The part number has been changed to reflect industry standards.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	2.5	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

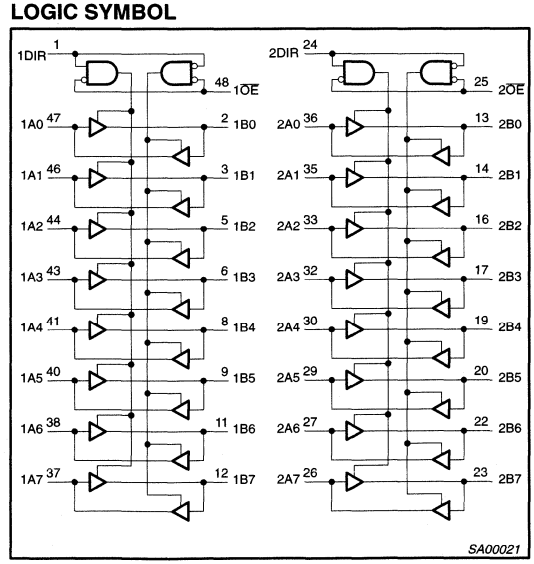
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT162245B DL	VT162245B DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT162245B DGG	VT162245B DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	$n\overline{OE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

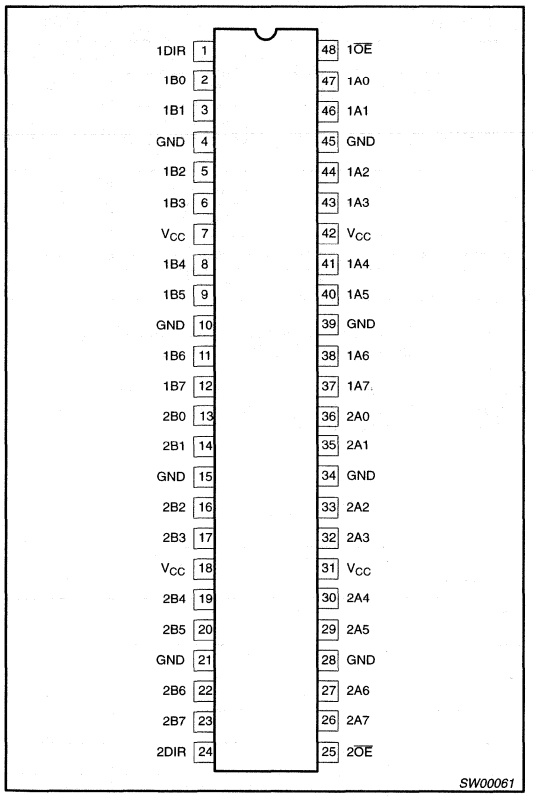
LOGIC SYMBOL



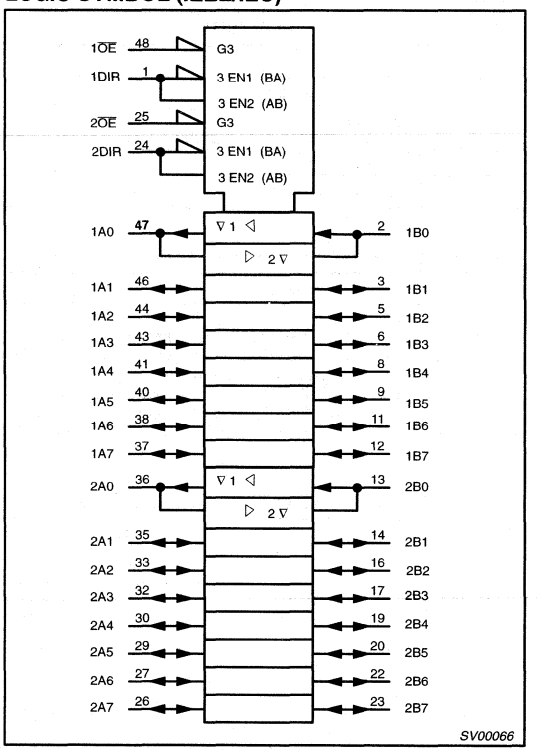
3.3V 16-bit transceiver with 30Ω termination resistors (3-State)

74LVT162245B

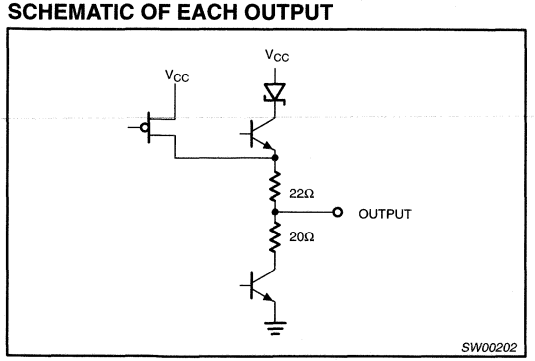
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
nOE	**nDIR**	**nAx**	**nBx**
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = –40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			0.8	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0	2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA			0.3	0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	I/O Data pins[4]		0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B outputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–130		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			75	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.2	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

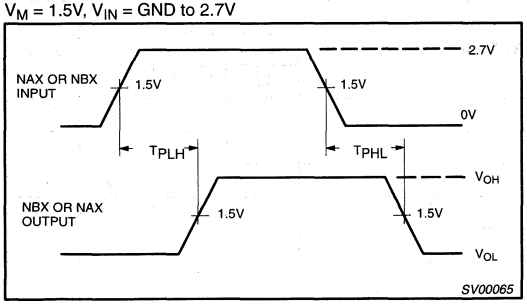
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to bBx or bBx to nAx	1	1.0 1.0	2.5 2.2	3.5 3.5	3.9 3.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	3.5 3.2	5.3 4.4	6.4 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.5 4.3	4.8 6.7	5.1 5.9	ns

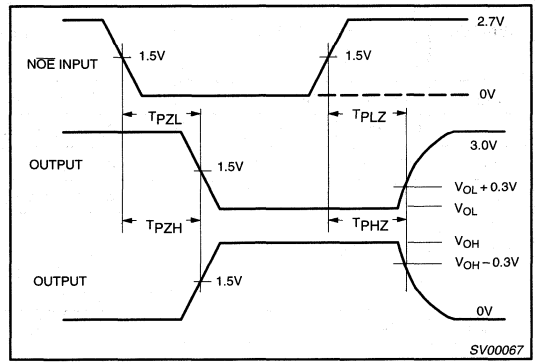
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

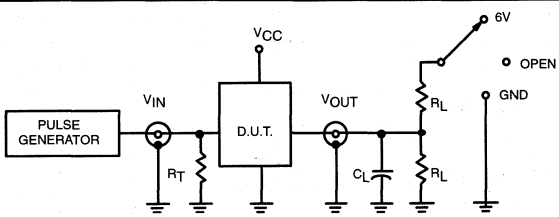


Waveform 1. Input to Output Propagation Delays

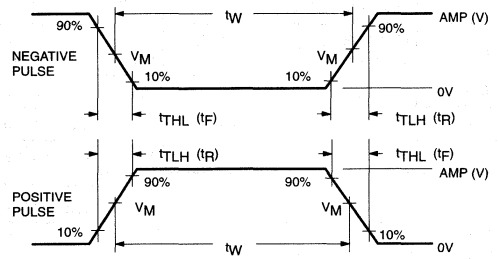


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit transparent D-type latch (3-State) 74LVT16373A

FEATURES

- 16-bit transparent latch
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16373A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When enable (E) input is High, the Q outputs follow the data (D) inputs. When enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

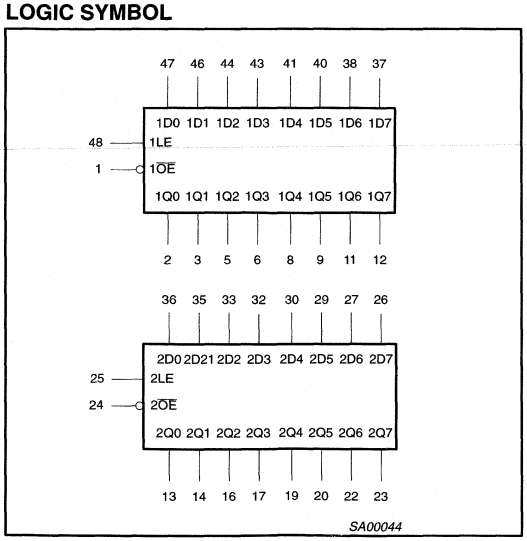
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16373A DL	VT16373A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16373A DGG	VT16373A DGG	SOT362-1

LOGIC SYMBOL

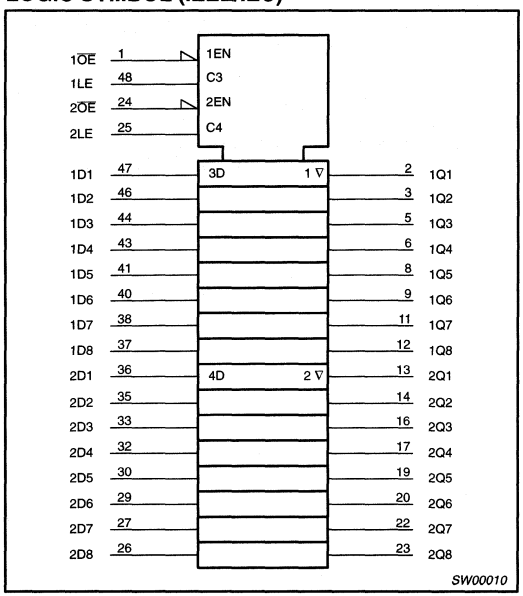


PIN DESCRIPTION

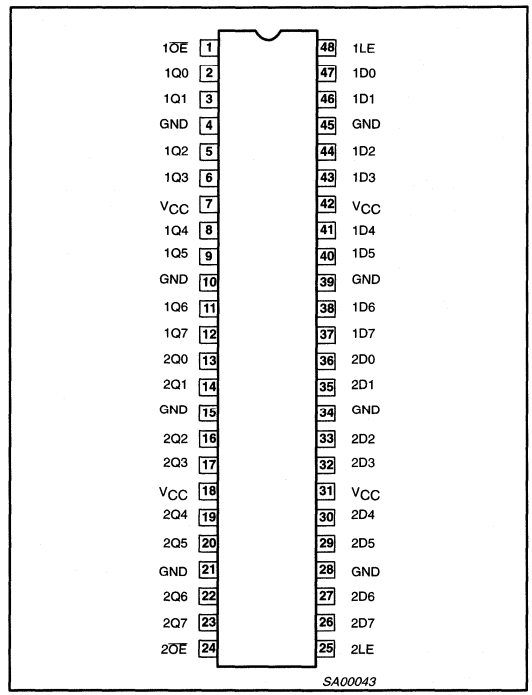
PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1E, 2E	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

3.3V 16-bit transparent D-type latch (3-State) 74LVT16373A

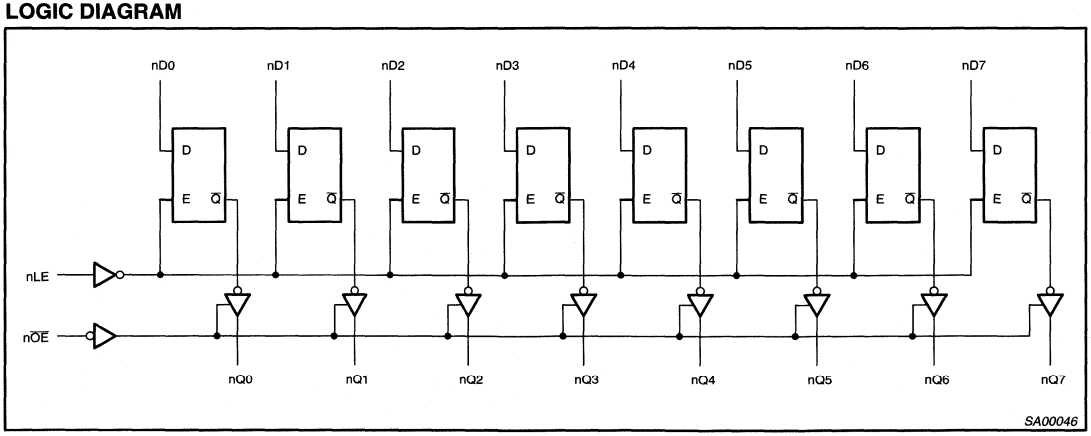
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nE	nDx		nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output Low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.1	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.4	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			-0.4	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current D inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	135		µA
		V_{CC} = 3V; V_I = 2.0V		–75	-135		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IH} or V_{IL}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IH} or V_{IL}			0.5	–5	
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.0	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	0.5 0.5	1.8 1.9	3.9 3.9	4.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay nE to nQx	1	0.5 0.5	2.1 2.2	4.8 4.8	5.4 5.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	0.1 0.1	2.8 2.6	4.5 4.3	5.1 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5	0.1 0.1	3.3 3.0	4.5 4.3	5.1 4.7	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

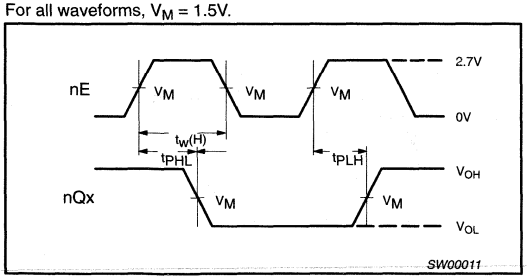
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

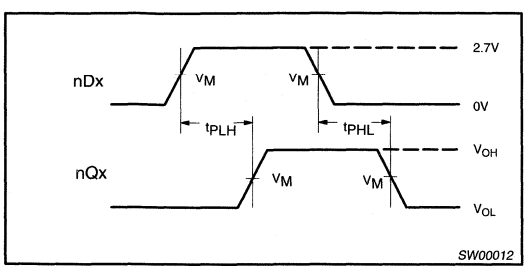
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
$t_S(H)$ $t_S(L)$	Setup time nDx to nE	3	1.5 2.0	0.1 0.2	1.0 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time nDx to nE	3	1.0 1.5	0 0	1.0 2.0	ns
$t_W(H)$	nE pulse width High	1	1.5	0.5	1.5	ns

AC WAVEFORMS

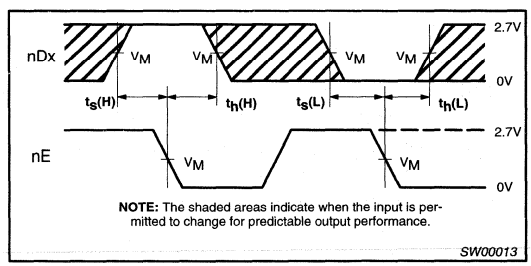
For all waveforms, V_M = 1.5V.



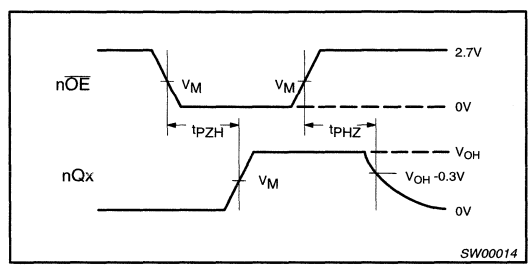
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



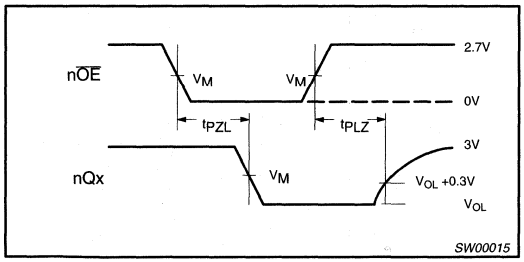
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

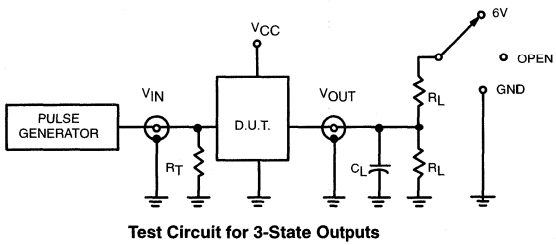


Waveform 4. 3-State Output Enable time to High Level and Output Disable Time from High Level

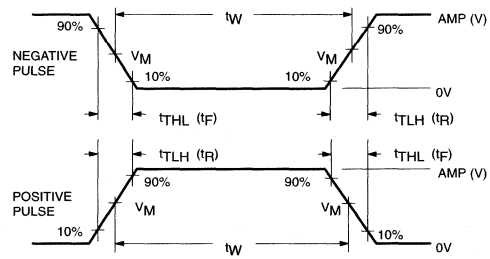


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

FEATURES

- 16-bit edge-triggered flip-flop
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16374A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit edge-triggered D-type flip-flop featuring non-inverting 3-State outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

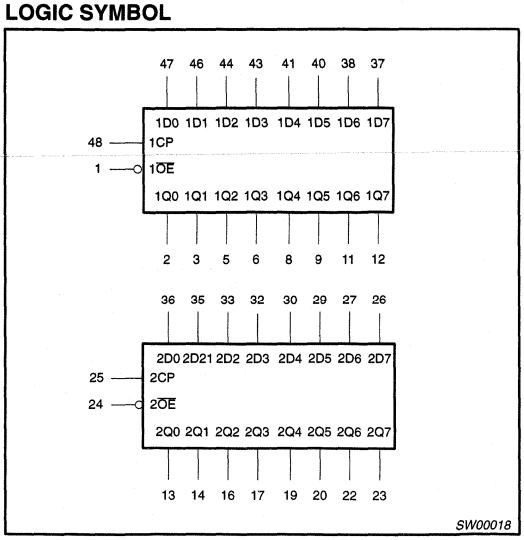
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 3.3V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output pin capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16374A DL	VT16374A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16374A DGG	VT16374A DGG	SOT362-1

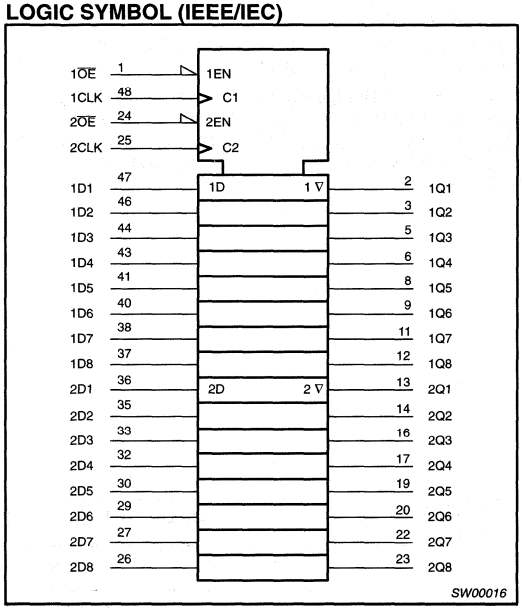
LOGIC SYMBOL



3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

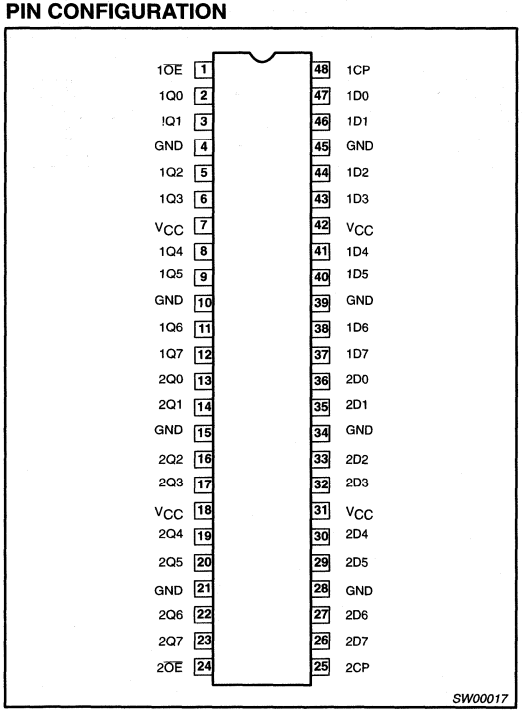
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	1D0 - 1D7 2D0 - 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12 13, 14, 16, 17, 19, 20, 22, 23	1Q0 - 1Q7 2Q0 - 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

PIN CONFIGURATION

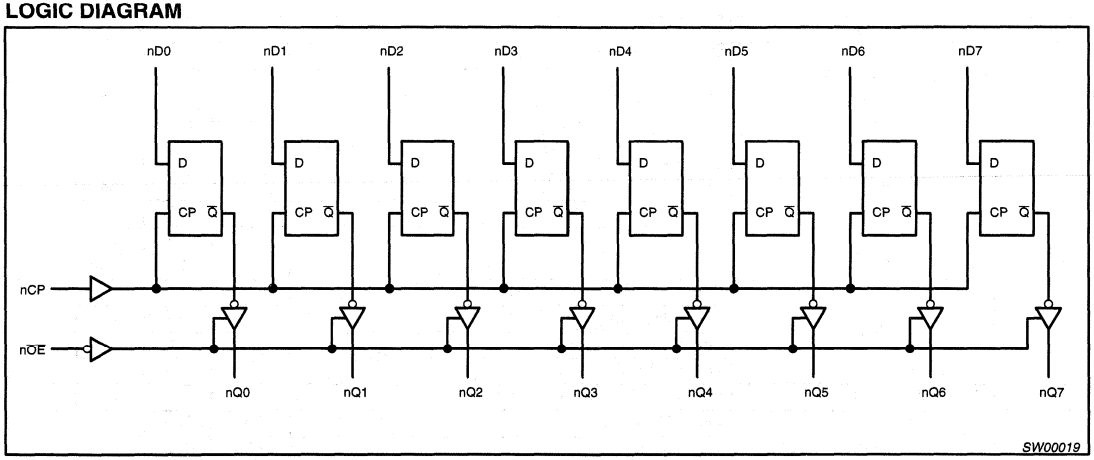


FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx	REGISTER	nQ0 - nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = -18mA			-.85	-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = -100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = -8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = -32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output Low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.1	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.4	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			-0.4	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current D inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	135		µA
		V_{CC} = 3V; V_I = 2.0V		-75	-135		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IH} or V_{IL}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IH} or V_{IL}			0.5	-5	
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{max}	Maximum clock frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nDx	1	1.5 1.5	2.9 3.0	5.0 5.0	5.6 5.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.5 1.5	3.2 3.0	4.8 4.6	6.0 5.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	3 4	1.5 1.5	3.9 3.4	5.4 4.6	6.0 5.0	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

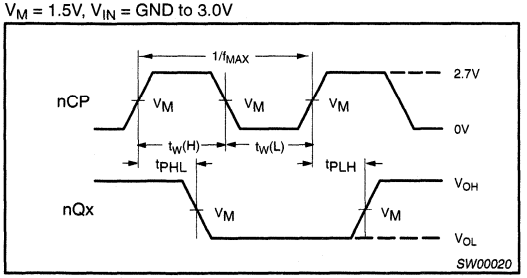
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

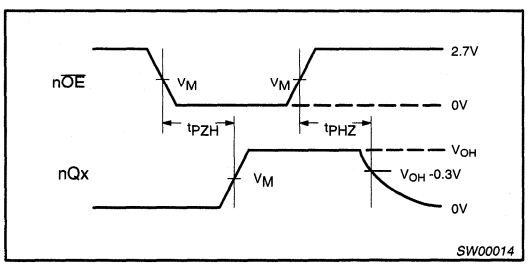
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
$t_S(H)$ $t_S(L)$	Setup time nDx to nE	3	2.5 2.5	0.7 0.7	2.5 2.5	ns
$t_h(H)$ $t_h(L)$	Hold time nDx to nE	3	0.5 0.5	0 0	0 0	ns
$t_W(H)$ tw(L)	nE pulse width High or Low	1	1.5 3.0	0.6 1.6	1.5 3.0	ns

AC WAVEFORMS

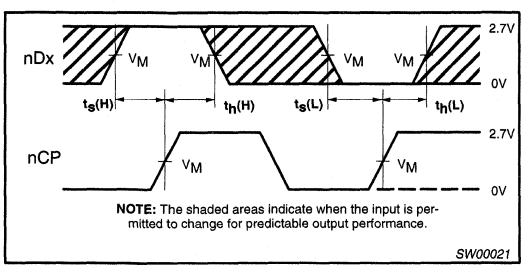
V_M = 1.5V, V_{IN} = GND to 3.0V



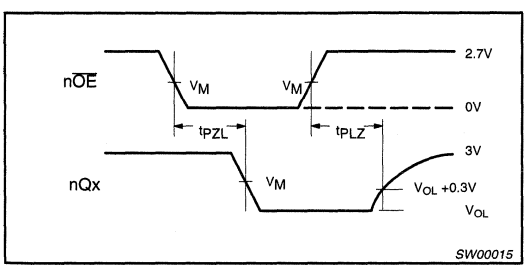
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

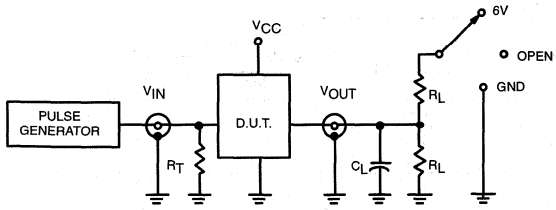


Waveform 2. Data Setup and Hold Times

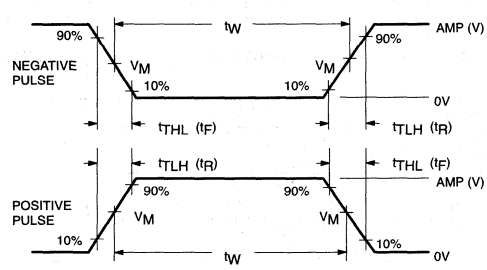


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 18-bit universal bus transceiver (3-State) 74LVT16500A

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Negative edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16500A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock ($\overline{CPAB}$ and $\overline{CPBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if $\overline{CPAB}$ is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of $\overline{CPAB}$. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and $\overline{CPBA}$. The output enables are complimentary (OEAB is active High, and $\overline{OEBA}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or 3.0V	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

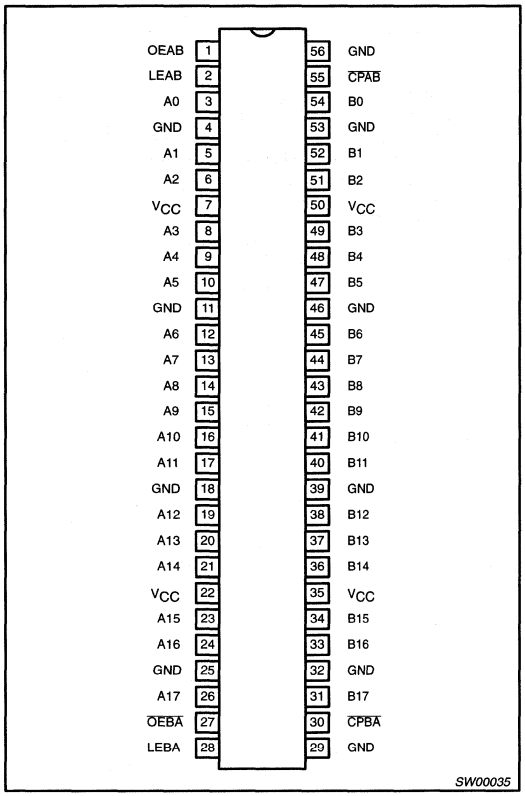
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16500A DL	VT16500A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16500A DGG	VT16500A DGG	SOT364-1

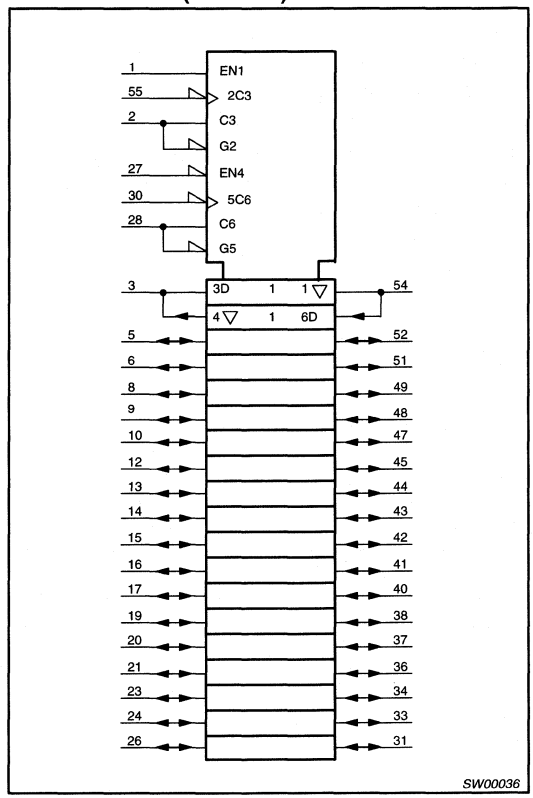
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	$\overline{CPAB}$/$\overline{CPBA}$	A-to-B/B-to-A Clock input (active falling edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

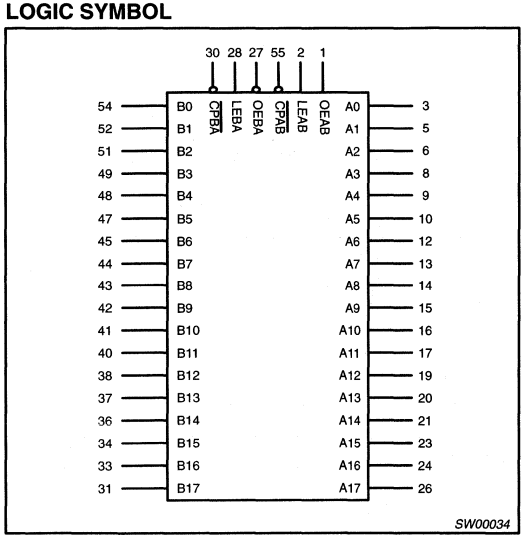
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



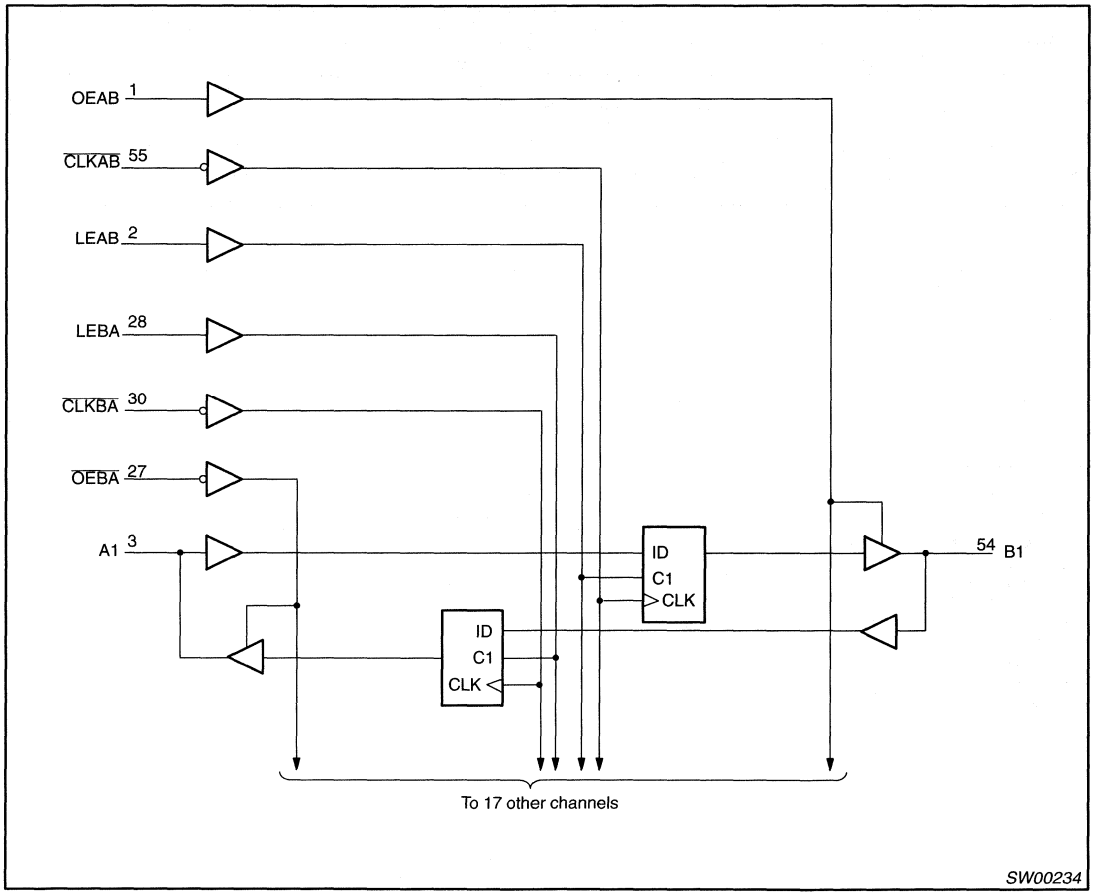
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	$\overline{CPAB}$	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↓	h	H	Z	Disabled, Clock data
L	L	↓	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↓	h	H	H	Clock data & display
H	L	↓	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CPBA}$.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.55		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.30		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.36	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.1	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1.0	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1.0	±100	µA
I_{HOLD}	Bus Hold current A or B outputs6	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		-75	–130		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	350			MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	0.5 0.5	1.9 1.9	4.2 4.2	5.4 5.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An	1	1.0 1.0	3.2 3.2	5.4 5.4	6.4 6.4	ns
t_{PLH} t_{PHL}	Propagation delay LEAB to Bn or LEBA to An	3	1.0 1.0	2.4 2.9	5.4 5.4	6.4 6.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.0 1.0	2.4 2.2	3.9 3.9	4.6 5.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.0 1.0	2.8 3.2	5.2 5.2	5.6 5.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

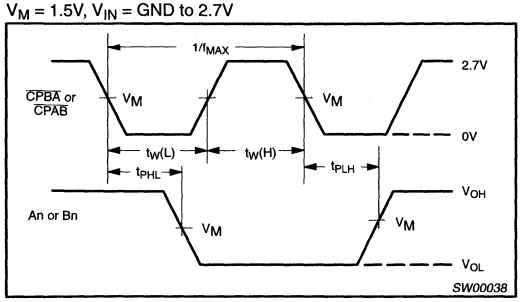
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

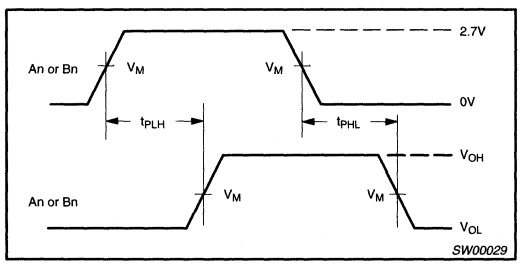
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
ts(H) ts(L)	Setup time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	1.8 1.8	1.0 0.7	1.5 1.5	ns
th(H) th(L)	Hold time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	0 0	0 0	0 0	ns
ts(H) ts(L)	Setup time, High or Low An to LEAB or Bn to $\overline{CPBA}$	4	1.8 1.8	1.1 0.8	1.5 1.5	ns
th(H) th(L)	Hold time, High or Low An to LEAB or Bn to LEBA	4	0 0	0 0	0 0	ns
tw(H) tw(L)	Pulse width, High or Low $\overline{CPAB}$ or $\overline{CPBA}$	1	1.2 1.2	0.8 0.8	1.5 1.5	ns
tw(H)	LEAB or LEBA pulse width, High	3	1.2	0.8	1.5	ns

AC WAVEFORMS

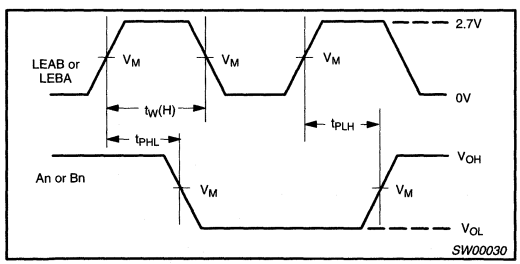
V_M = 1.5V, V_{IN} = GND to 2.7V



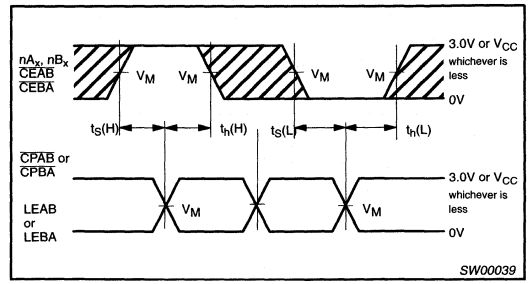
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



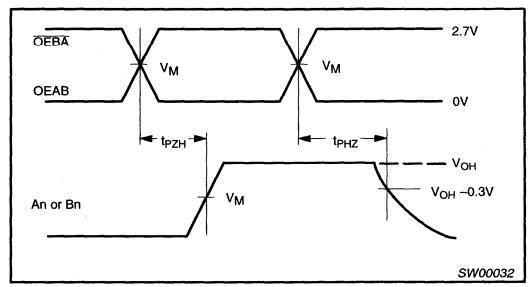
Waveform 2. Propagation Delay, Transparent Mode



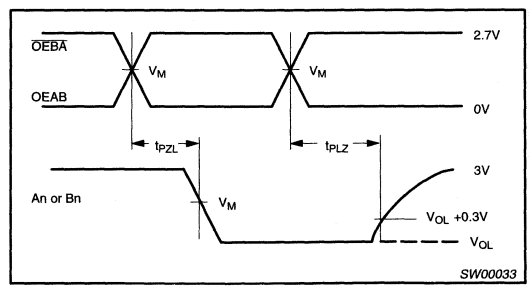
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 4. Data Setup and Hold Times

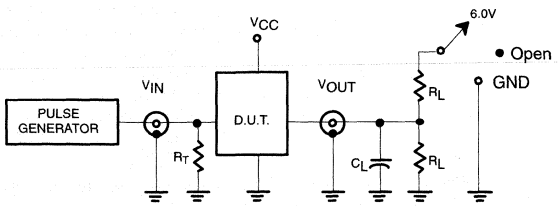


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

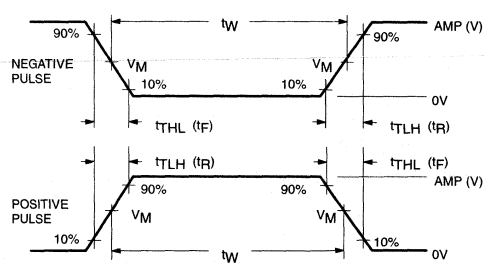


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00040

3.3V 18-bit universal bus transceiver (3-State) 74LVT16501A

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Positive edge triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16501A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and CPBA. The output enables are complimentary (OEAB is active High, and $\overline{OEBA}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or 3.0V	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

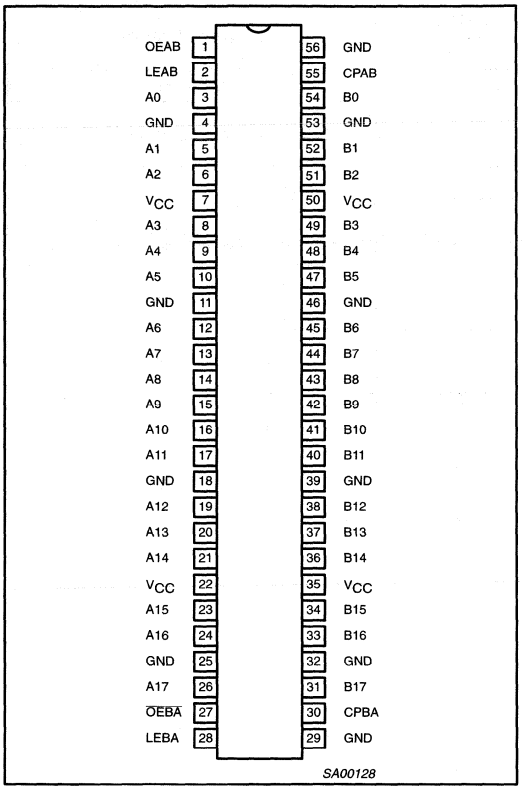
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16501A DL	VT16501A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16501A DGG	VT16501A DGG	SOT364-1

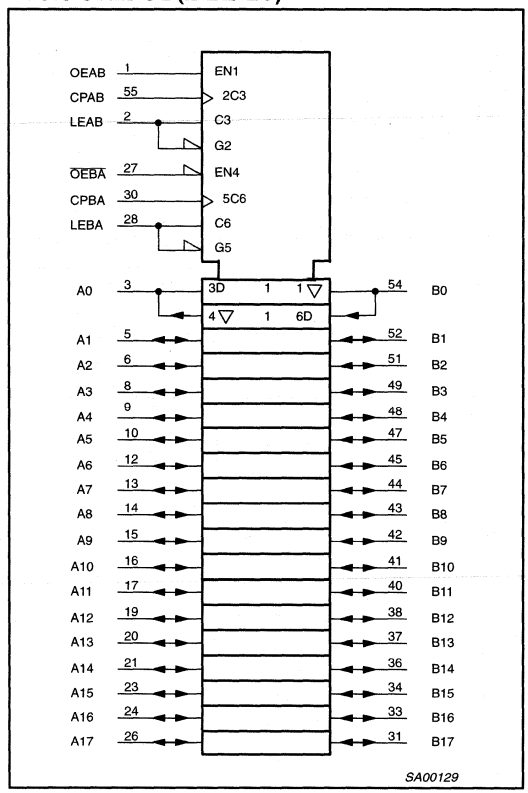
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

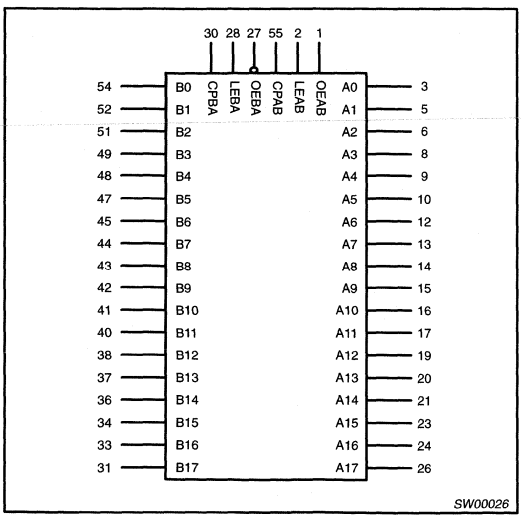
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



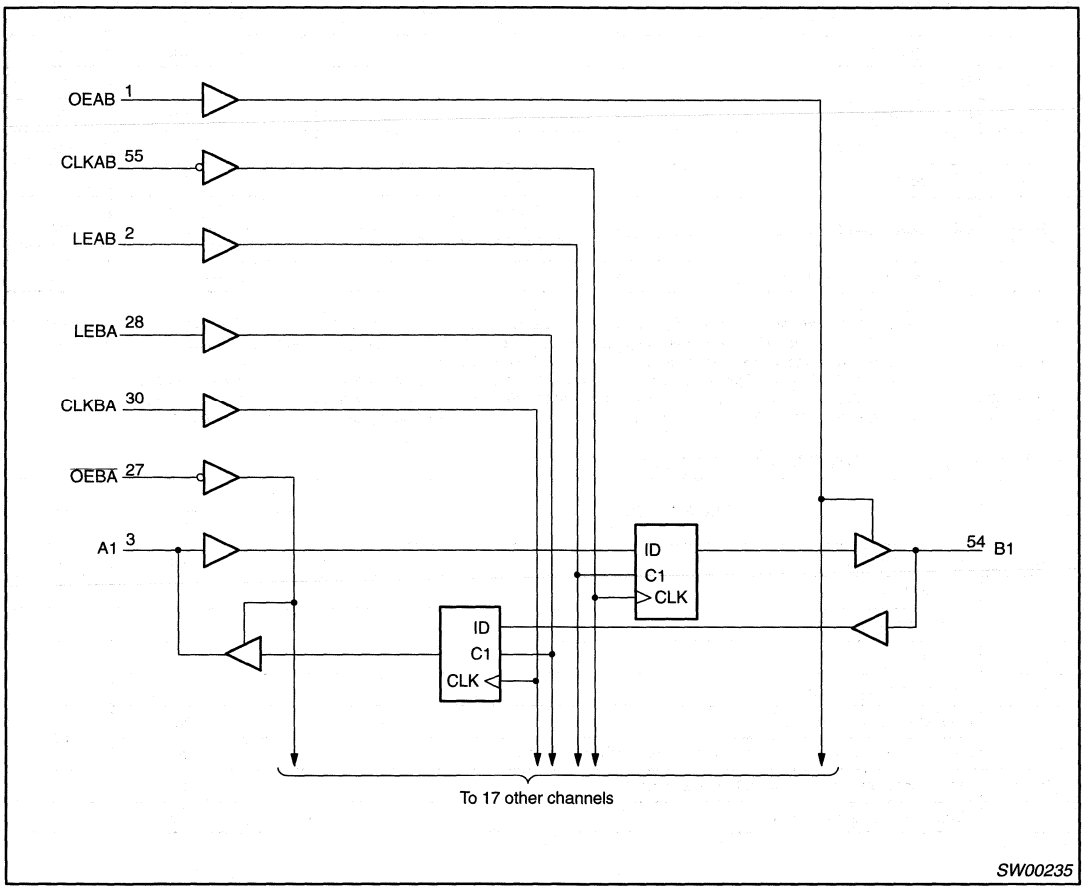
FUNCTION TABLE

INPUTS				INTERNAL REGISTER	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↑	h	H	Z	Disabled, Clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↑	h	H	H	Clock data & display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CPBA.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedence "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS [1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.55		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.36	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.1	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1.0	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1.0	±100	µA
I_{HOLD}	Bus Hold current A or B outputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–130		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	0.5 0.5	1.9 1.9	4.2 4.2	5.4 5.4	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.0 1.0	3.2 3.2	5.4 5.4	6.4 6.4	ns
t_{PLH} t_{PHL}	Propagation delay LEAB to Bn or LEBA to An	3	1.0 1.0	2.4 2.9	5.4 5.4	6.4 6.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.0 1.0	2.4 2.2	3.9 3.9	4.6 5.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.0 1.0	2.8 3.2	5.2 5.2	5.6 5.6	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

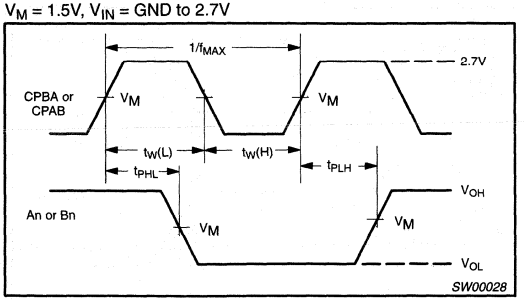
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

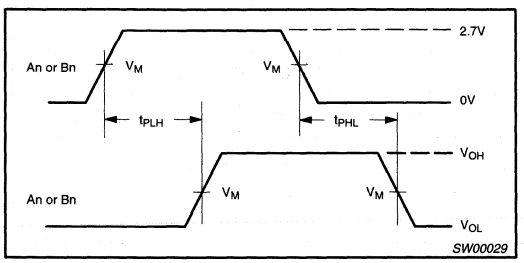
SYMBOL	PARAMETER	WAVEFORM	V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	UNIT
			MIN	TYP	MIN	
ts(H) ts(L)	Setup time, High or Low An to CPAB or Bn to CPBA	4	1.8 1.8	1.0 0.7	1.5 1.5	ns
th(H) th(L)	Hold time, High or Low An to CPAB or Bn to CPBA	4	0 0	0 0	0 0	ns
ts(H) ts(L)	Setup time, High or Low An to LEAB or Bn to CPBA	4	1.8 1.8	1.1 1.8	1.5 1.5	ns
th(H) th(L)	Hold time, High or Low An to LEAB or Bn to LEBA	4	0 0	0 0	0 0	ns
tw(H) tw(L)	Pulse width, High or Low CPAB or CPBA	1	1.2 1.2	0.8 0.8	1.5 1.5	ns
tw(H)	LEAB or LEBA pulse width, High	3	1.2	0.8	1.5	ns

AC WAVEFORMS

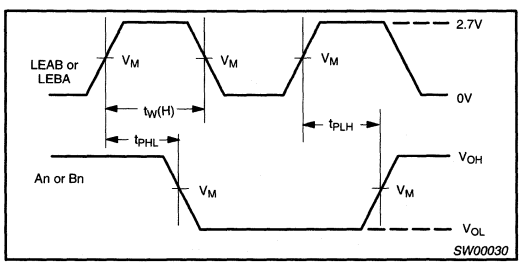
V_M = 1.5V, V_{IN} = GND to 2.7V



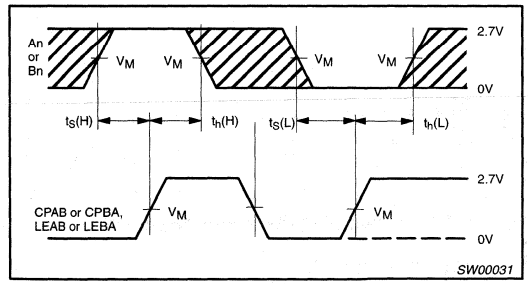
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



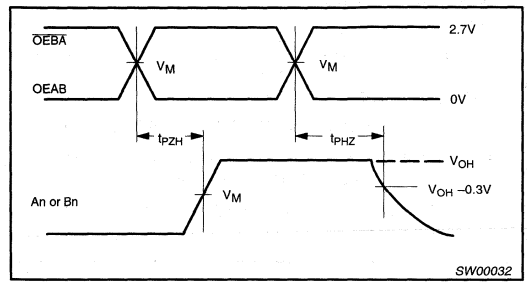
Waveform 2. Propagation Delay, Transparent Mode



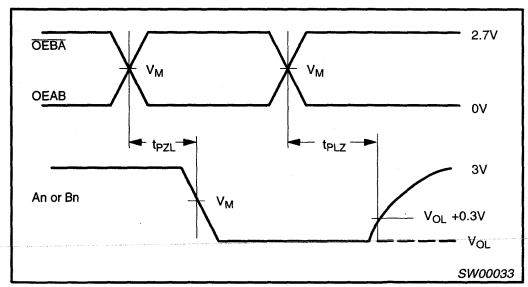
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 4. Data Setup and Hold Times

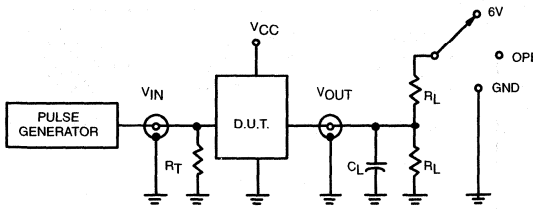


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

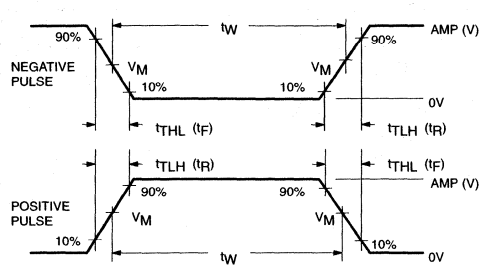


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit registered transceiver (3-State) 74LVT16543A

FEATURES

- 16-bit universal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16543A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVT16543A contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are Low, the A-to-B path is transparent.

A subsequent Low-to-High transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $n\overline{EAB}$ and $n\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

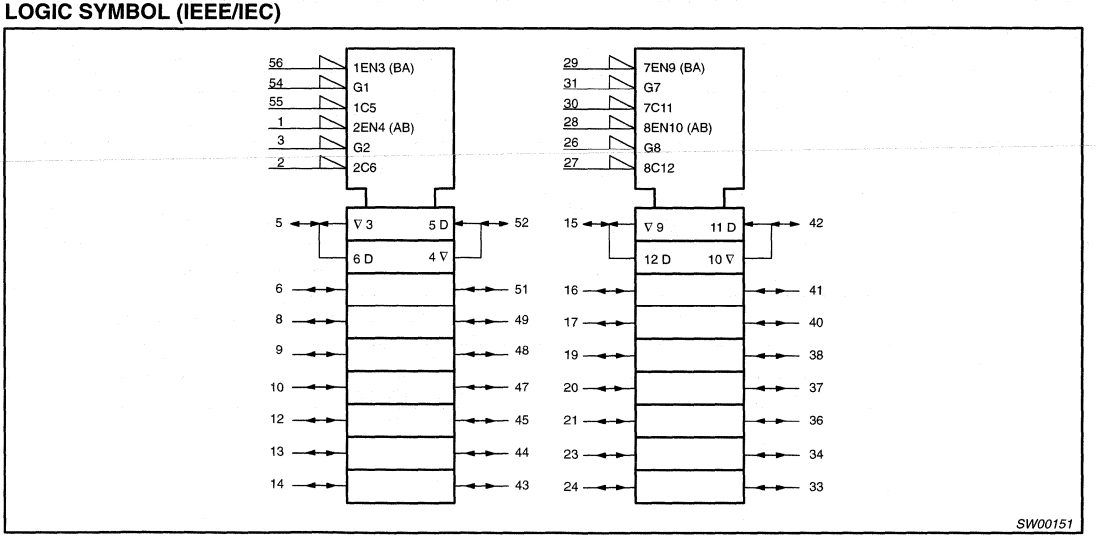
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	2.2	ns
C_{IN}	Input capacitance control pins	V_I = 0V or 3.0V	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

ORDERING INFORMATION

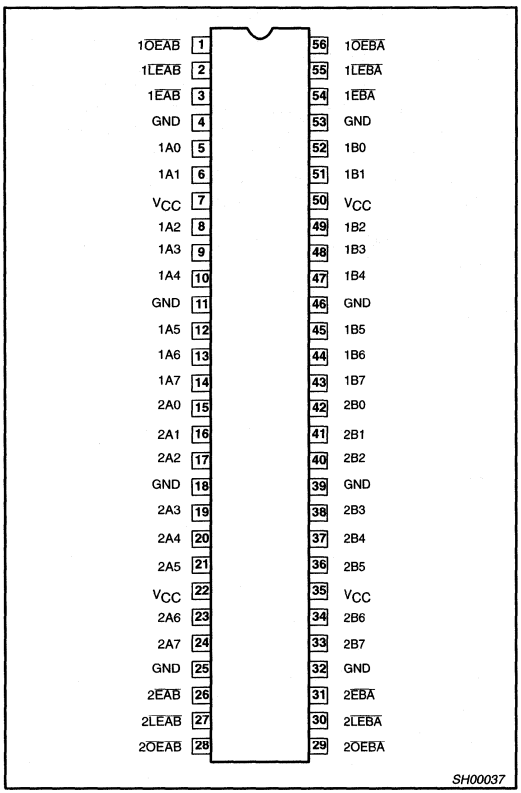
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16543A DL	VT16543A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16543A DGG	VT16543A DGG	SOT364-1

LOGIC SYMBOL (IEEE/IEC)

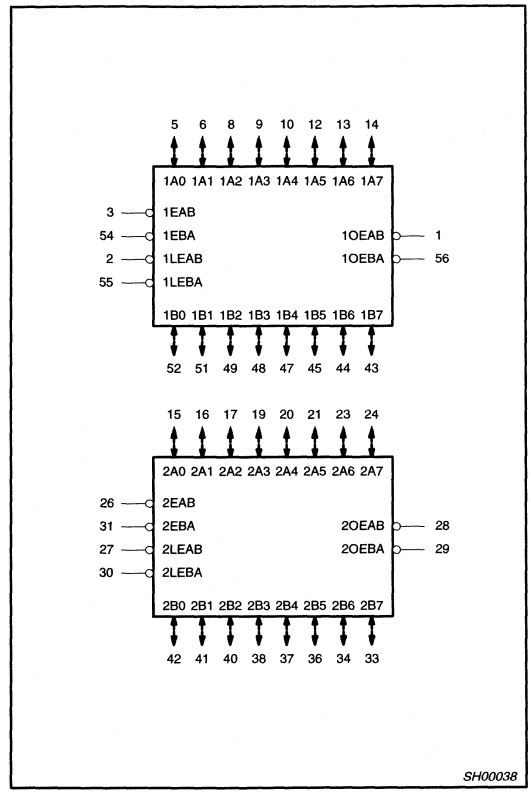


3.3V 16-bit registered transceiver (3-State) 74LVT16543A

PIN CONFIGURATION



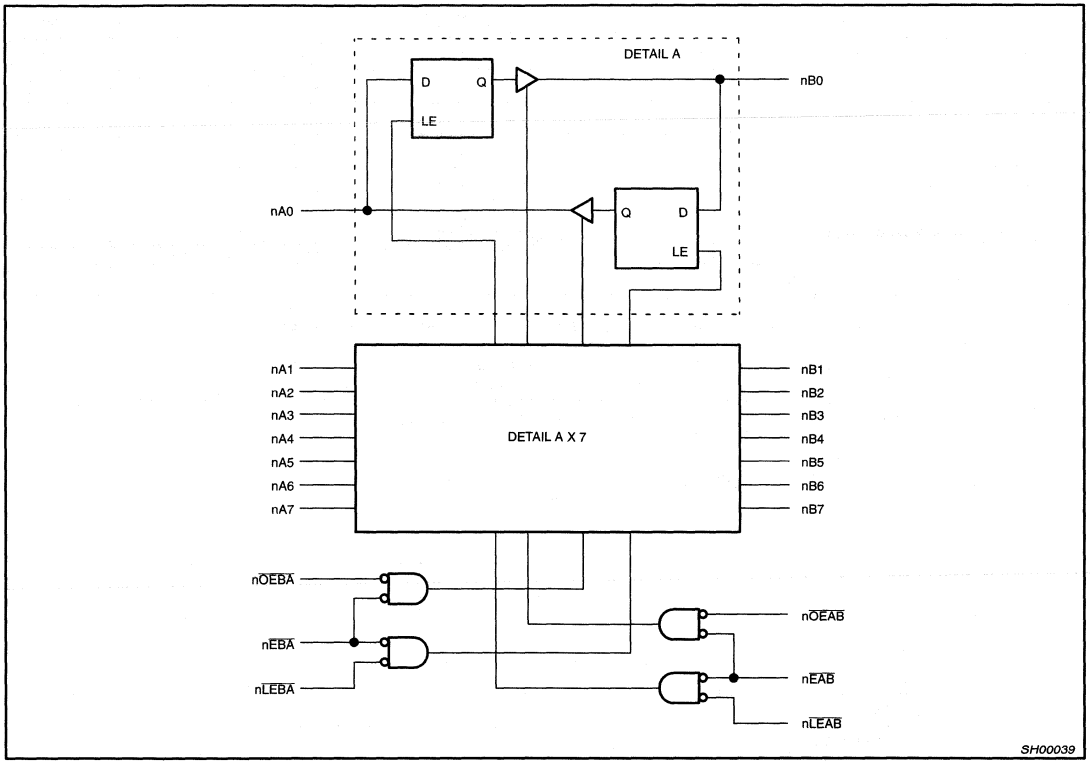
LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	A Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	B Data inputs/outputs
1, 56 28, 29	$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	$1\overline{EAB}$, $1\overline{EBA}$, $2\overline{EAB}$, $2\overline{EBA}$	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	$1\overline{LEAB}$, $1\overline{LEBA}$, $2\overline{LEAB}$, $2\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
nOEXX	nEXX	nLEXX	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of nLEXX or nEXX (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of nLEXX or nEXX (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of nLEXX or nEXX (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.54		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.36		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.2	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.35	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		0.5	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			1.0	–5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1.0	±100	µA
I_{HOLD}	Bus Hold current A or B outputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			45	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			35	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.5	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and .
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.0 1.0	2.2 2.2	3.7 3.7	4.4 4.4	ns
t_{PLH} t_{PHL}	Propagation delay n$\overline{LEBA}$ to nAx, n$\overline{LEAB}$ to nBx	1 2	1.5 1.5	2.7 2.7	4.8 4.8	6.2 6.2	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	1.5 1.5	2.8 2.6	4.6 5.0	6.1 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	2.0 2.0	3.1 3.2	5.2 4.6	5.7 4.7	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	1.5 1.5	2.9 2.6	4.8 5.1	6.1 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	2.0 2.0	3.1 3.2	5.1 4.3	5.7 4.5	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

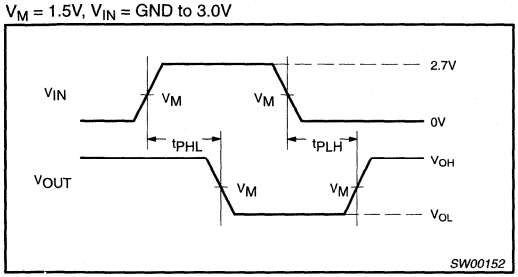
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

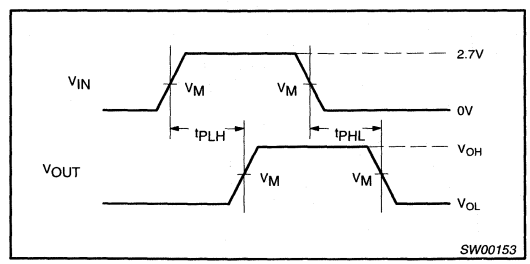
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	0.8 1.0	0.4 0.1	0.5 1.5	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	1.0 1.2	0.2 0.4	0.5 1.3	ns
t_s(H) t_s(L)	Setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	0.7 1.3	0.1 0.1	0.4 1.5	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	1.2 1.3	0.2 0.4	0.8 1.4	ns
t_W(L)	Latch enable pulse width, Low	3	1.8	1.0	1.8	ns

AC WAVEFORMS

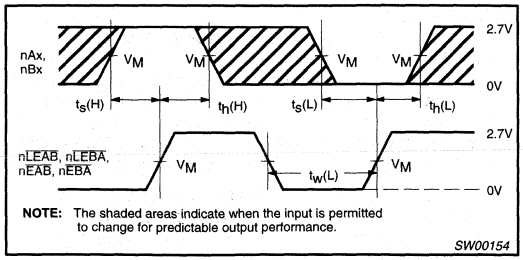
V_M = 1.5V, V_{IN} = GND to 3.0V



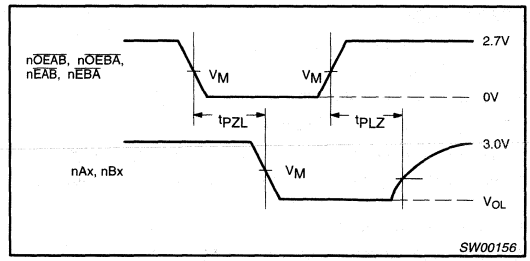
Waveform 1. Propagation Delay For Inverting Output



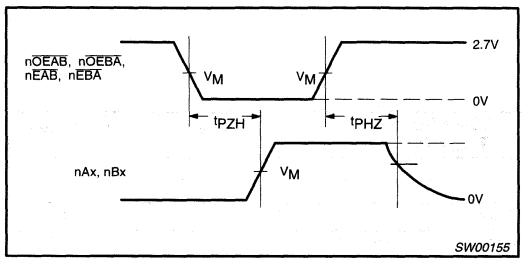
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width

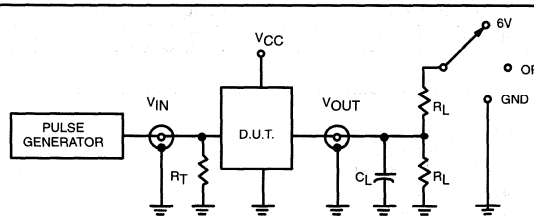


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

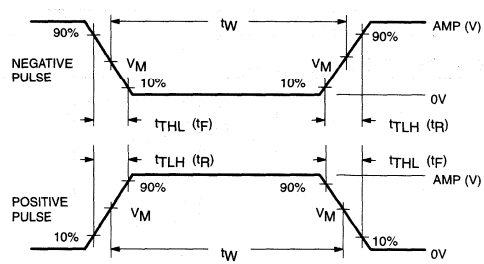


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit bus transceiver (3-State) 74LVT16646A

FEATURES

- 16-bit universal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16646A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

Data on the A or B bus is clocked into the registers on the Low to High transition of the appropriate clock (CPAB or CPBA). The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode data).

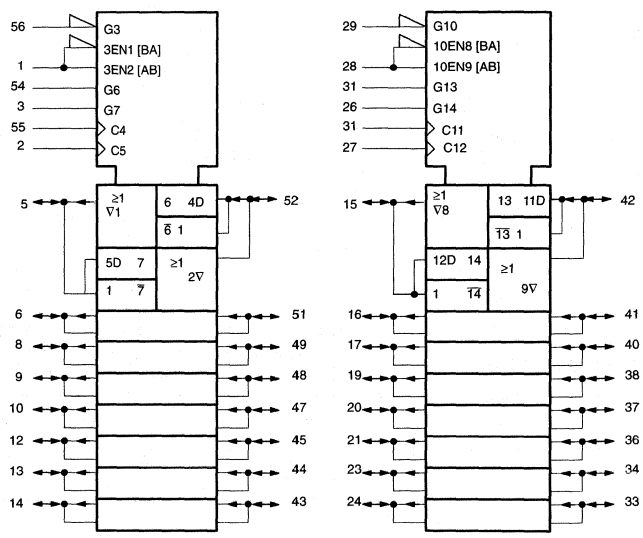
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

ORDERING INFORMATION

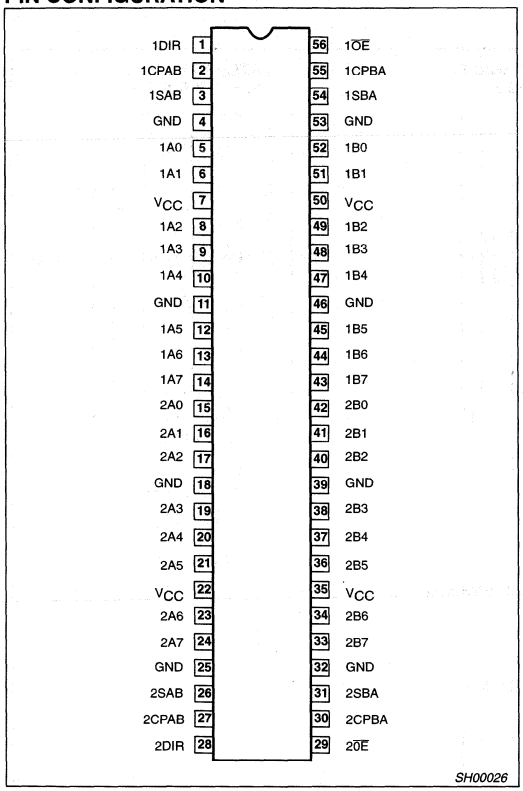
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT166646A DL	VT16646A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16646A DGG	VT16646A DGG	SOT364-1

LOGIC SYMBOL (IEEE/IEC)

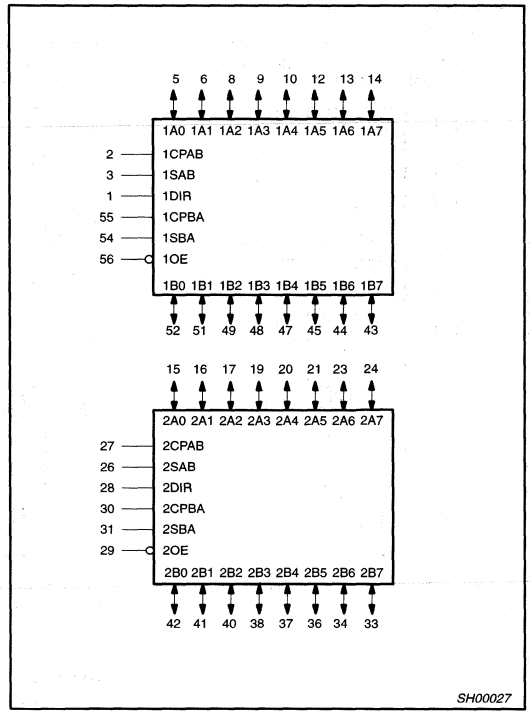


3.3V 16-bit bus transceiver (3-State) 74LVT16646A

PIN CONFIGURATION



LOGIC SYMBOL

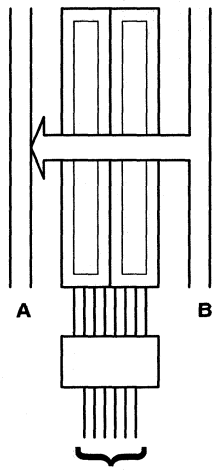


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
1, 28	1DIR, 2DIR	Direction control inputs
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 - 1A7, 2A0 - 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 - 1B7, 2B0 - 2B7	Data inputs/outputs (B side)
56, 29	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

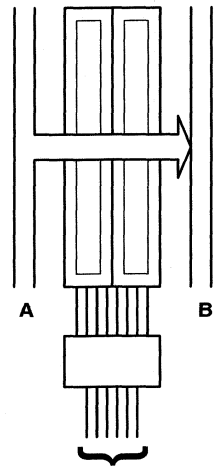
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74LVT16646A.

REAL TIME BUS TRANSFER BUS B TO BUS A



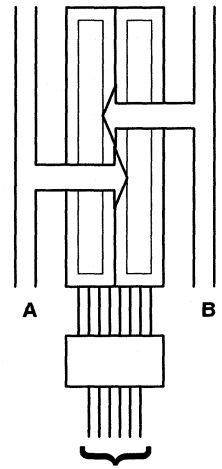
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



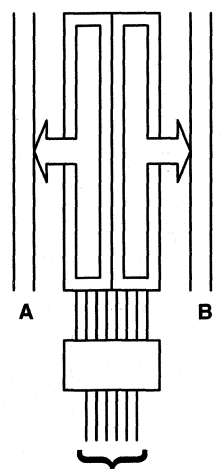
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	↑	X	X	X
L	L	X	↑	X	X
H	X	↑	↑	X	X

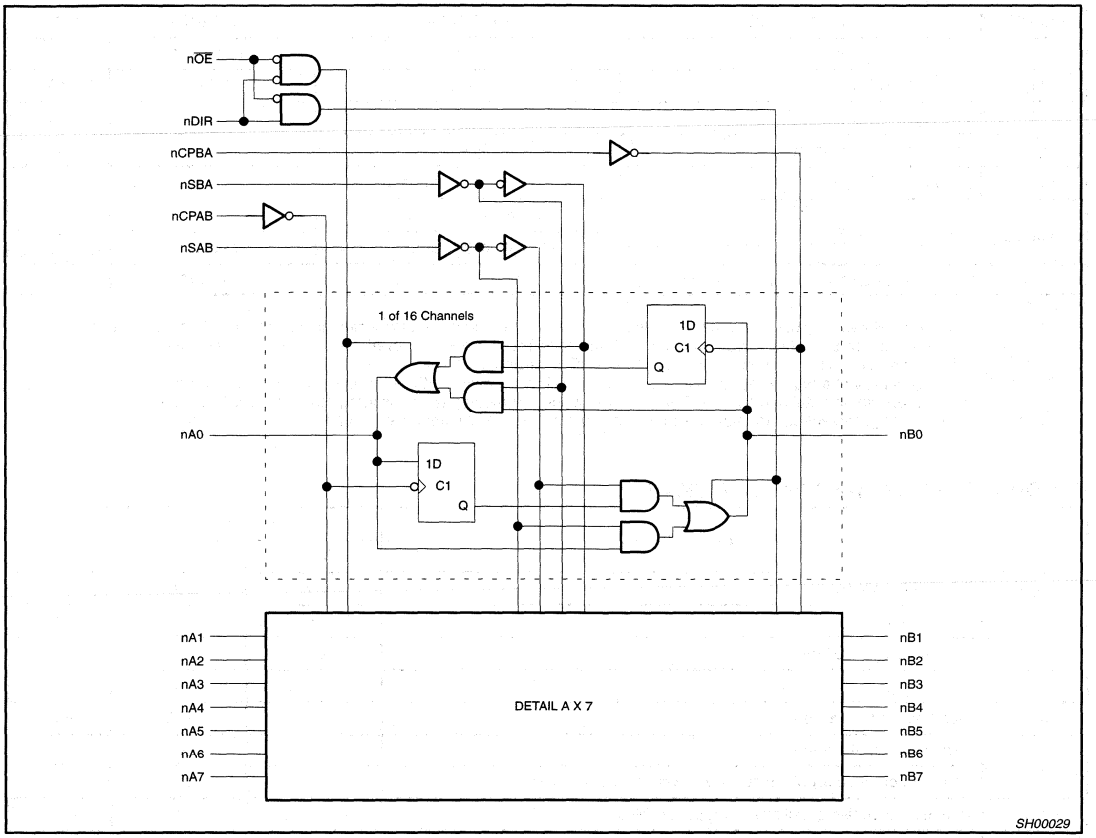
TRANSFER STORED DATA TO A OR B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	H|L	X	H
L	H	H|L	X	H	X

SH00028

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOE	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOE input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			.03	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B outputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			35	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.9	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a. transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2 3	0.5 0.5	1.9 1.9	3.7 3.7	4.3 4.4	ns
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.5 1.5	2.7 2.4	4.5 4.5	5.3 5.2	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	2	1.0 1.0	2.5 2.8	4.9 4.9	5.7 5.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.0 1.0	2.7 2.5	4.3 4.4	5.1 5.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	3.2 2.9	5.2 4.6	5.5 4.7	ns
t_{PZH} t_{PZL}	Output Enable time nDIR to nAx or nBx	5 6	1.0 1.0	2.9 2.8	4.5 4.6	5.3 5.3	ns
t_{PHZ} t_{PLZ}	Output Disable time nDIR to nAx or nBx	5 6	1.0 1.0	3.1 2.9	5.7 5.2	6.6 5.7	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

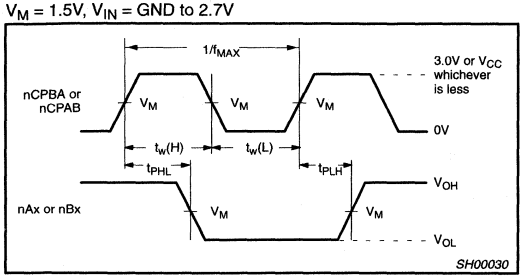
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

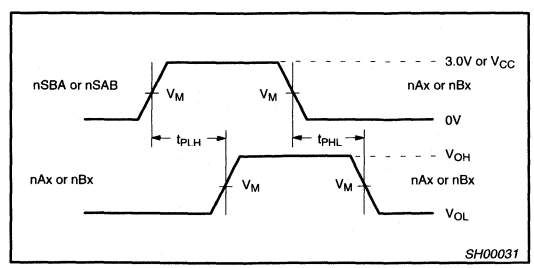
SYMBOL	PARAMETER	WAVEFORM				UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
ts(H) ts(L)	Setup time, High or Low nAx to nCPAB or nBx to nCPBA	4	1.0 1.9	0.6 0.4	1.1 2.4	ns
th(H) th(L)	Hold time, High or Low nAx to nCPAB or nBx to nCPBA	4	1.0 1.0	0.4 0.5	1.0 1.0	ns
tw(H) tw(L)	Pulse width, High or Low nCPAB or nCPBA	1	2.6 2.8	2.2 2.4	2.6 2.8	ns

AC WAVEFORMS

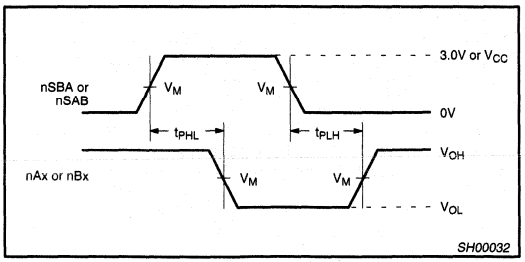
V_M = 1.5V, V_{IN} = GND to 2.7V



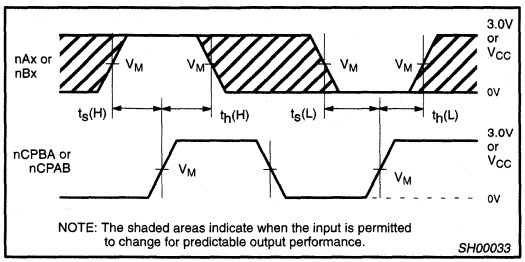
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



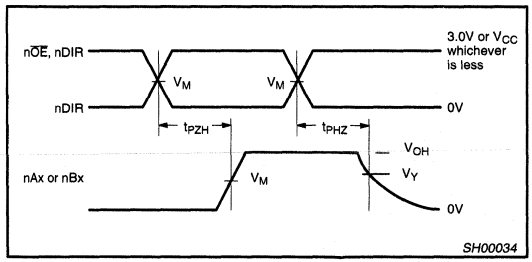
Waveform 2. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx



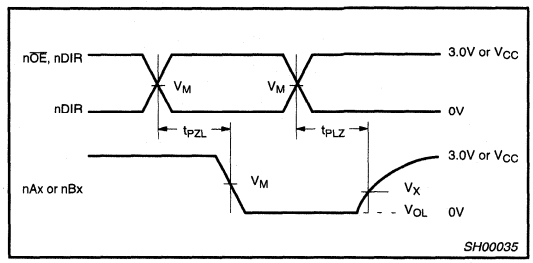
Waveform 3. Propagation Delay, nSBA to nAx or nSAB to nBx



Waveform 4. Data Setup and Hold Times

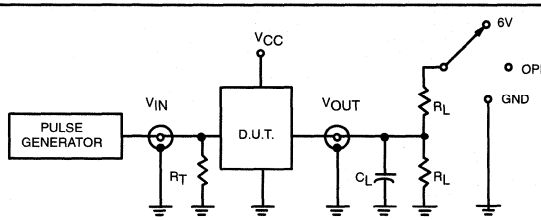


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

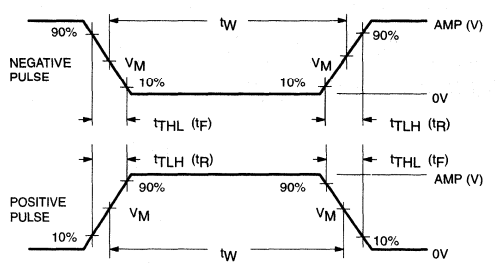


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

3.3V 16-bit bus transceiver/register (3-State) 74LVT16652A

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16652A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complimentary output-enable (OEAB and $\overline{OE}$BA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A Low-input level selects real-time data, and a High input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

Data on the A or B bus, or both, can be stored in the internal flip-flops by Low-to-High transitions at the appropriate clock (CPAB or CPBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OE}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

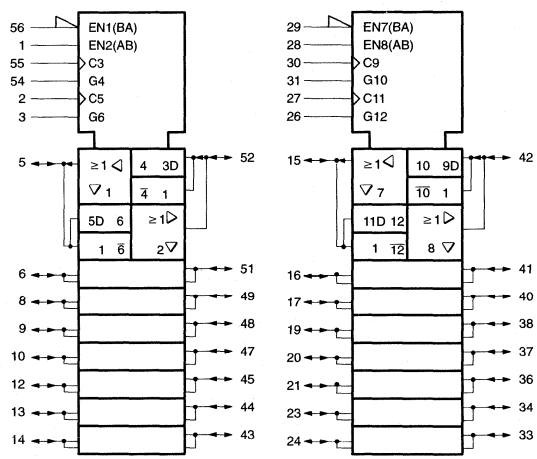
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance Control pins	V_I = 0V or 3.0V	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; V_I = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16652A DL	VT16652A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16652A DGG	VT16652A DGG	SOT364-1

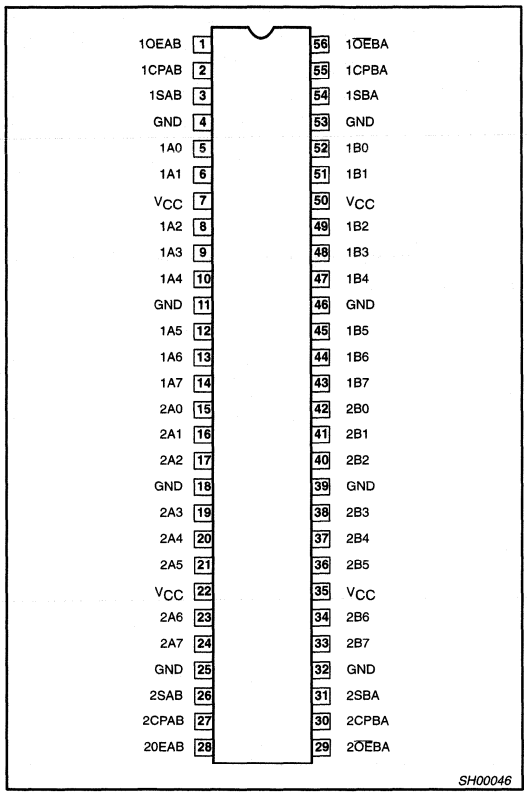
LOGIC SYMBOL (IEEE/IEC)



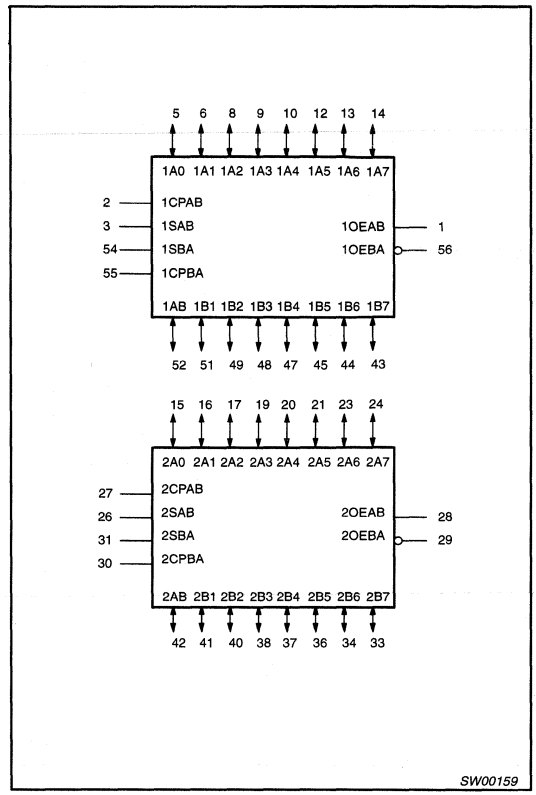
SW00158

3.3V 16-bit bus transceiver/register (3-State) 74LVT16652A

PIN CONFIGURATION



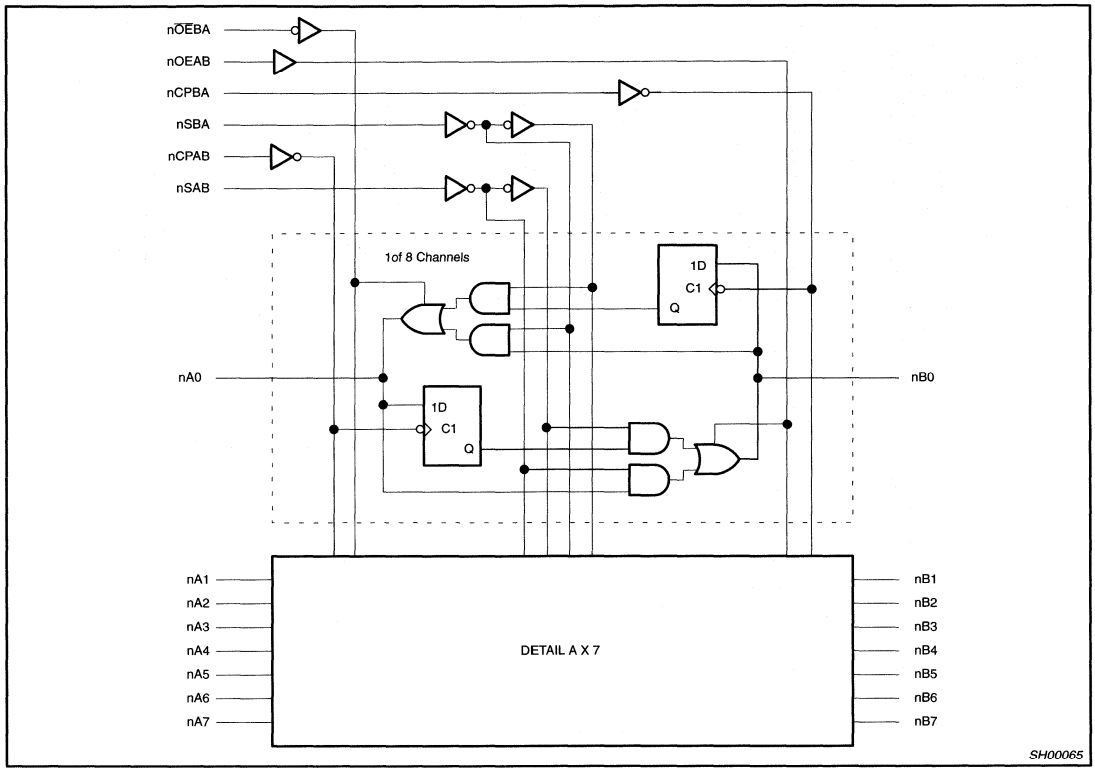
LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
1, 56, 28, 29	1OEAB, 1$\overline{OE}$BA, 2OEAB, 2$\overline{OE}$BA	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



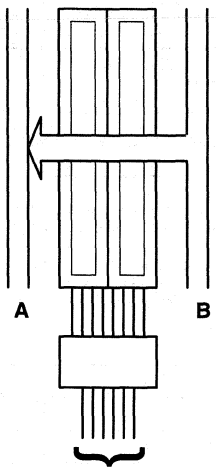
FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOEBA and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (nSAB and nSBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

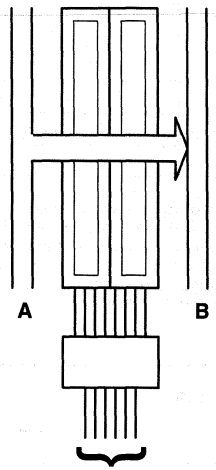
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74LVT16652A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

REAL TIME BUS TRANSFER BUS B TO BUS A



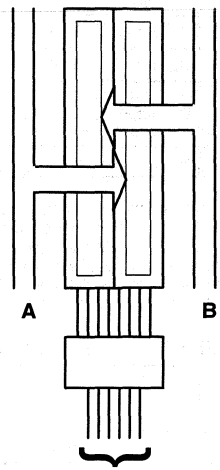
nOEAB	nŌEBA	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



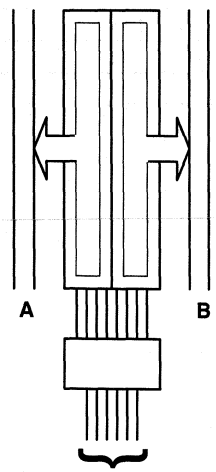
nOEAB	nŌEBA	nCPAB	nCPBA	nSAB	nSBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



nOEAB	nŌEBA	nCPAB	nCPBA	nSAB	nSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



nOEAB	nŌEBA	nCPAB	nCPBA	nSAB	nSBA
H	L	H|L	H|L	H	H

SH00066

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.11	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B outputs[6]	V_{CC} = 3V; V_I = 0.8V		75	135		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			45	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			35	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.9	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	180			MHz
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	0.5 0.5	1.9 1.9	3.7 3.7	4.0 4.0	ns
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.5 1.5	2.7 2.4	4.5 4.5	4.9 4.9	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	3	1.0 1.0	2.3 2.8	4.8 4.8	5.4 5.4	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{OE}$BA to nAx	5 6	1.0 1.0	2.7 2.5	4.6 4.6	5.0 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{OE}$BA to nAx	5 6	1.5 1.5	3.9 2.9	4.9 4.9	4.8 4.6	ns
t_{PZH} t_{PZL}	Output enable time nOEAB to nBx	5 6	1.0 1.0	2.9 2.7	4.6 4.6	5.0 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time nOEAB to nBx	5 6	1.5 1.5	3.1 2.8	4.9 4.9	5.2 4.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS

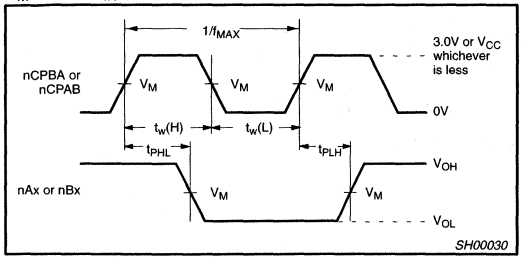
GND = 0V, t_R = 2.5ns, t_F = 2.5ns, C_L = 50pF, R_L = 500Ω, T_{amb} = –40 °C to +85 °C

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time 1 nAx to nCPAB, nBx to nCPBA	4	1.0 1.9	0.6 0.5	1.1 2.4	ns
t_h(H) t_h(L)	Hold time 1 nAx to nCPAB, nBx to nCPBA	4	1.0 1.0	0.4 0.5	1.0 1.0	ns
t_w(H) t_w(L)	Pulse width, High or Low nCPAB or nCPBA	1	2.6 2.8	2.2 2.4	2.6 2.8	ns

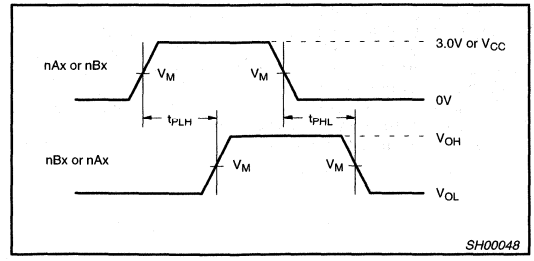
NOTE:
1. This data sheet limit may vary among suppliers.

AC WAVEFORMS

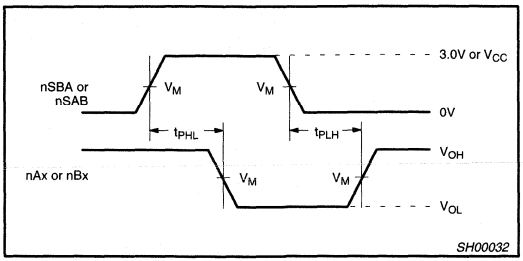
V_M = 1.5V, V_{IN} = GND to 3.0V



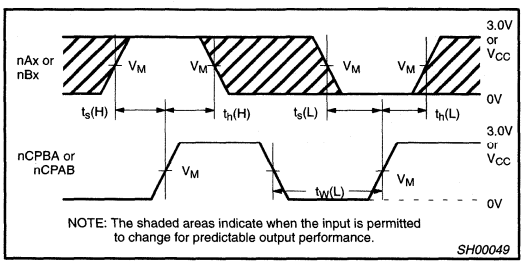
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



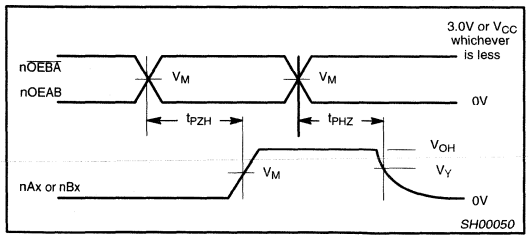
Waveform 2. Propagation Delay, nAx to nBx or nBx to nAx



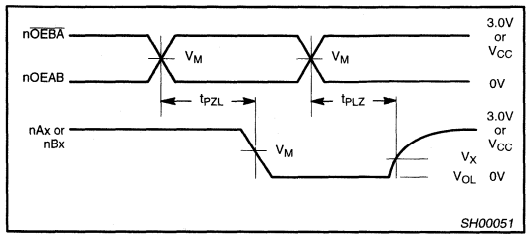
Waveform 3. Propagation Delay, SBA to nAx or SAB to nBx



Waveform 4. Data Setup and Hold Times

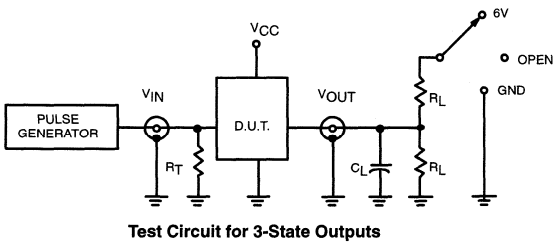


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

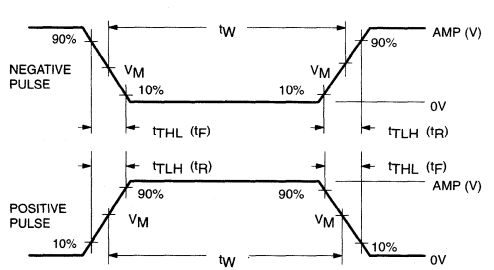


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

Section 4
2.5V/3.3V Devices
ALVT

BiCMOS Bus Interface Logic

CONTENTS

2.5V/3.3V 16-bit inverting buffer/driver (3-State) 74ALVT16240

FEATURES

- 16-bit bus interface
- 5V I/O compatibile
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16240 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

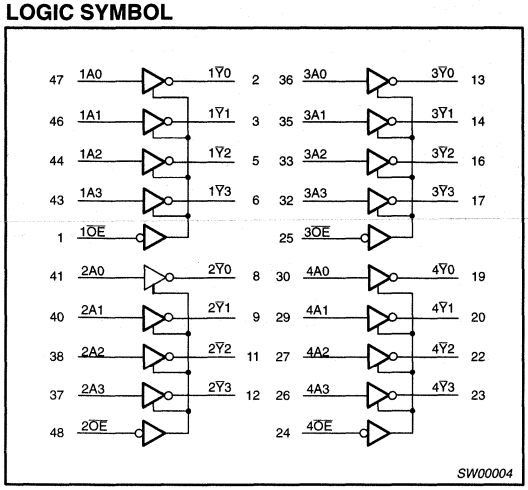
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL 2.5V	TYPICAL 3.3V	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF	2.5 1.9	1.7 1.7	ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_O	Output pin capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	60	µA

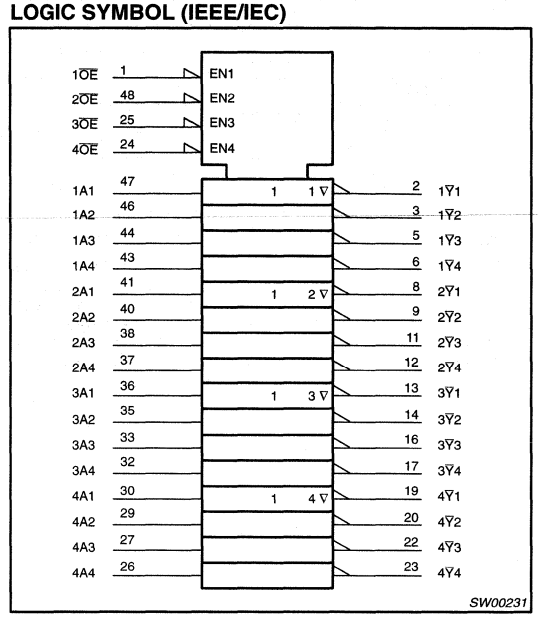
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16240 DL	AV16240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16240 DGG	AV16240 DGG	SOT362-1

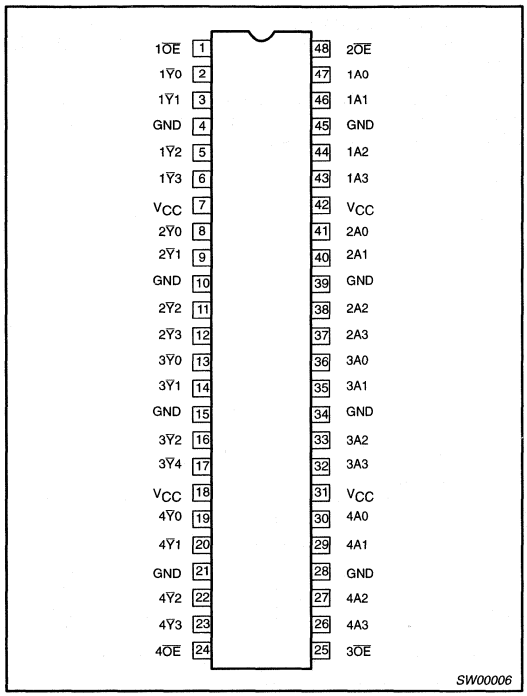
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0-1$\overline{Y}$3 2$\overline{Y}$0-2$\overline{Y}$3 3$\overline{Y}$0-3$\overline{Y}$3 4$\overline{Y}$0-4$\overline{Y}$3	Data outputs
1, 48, 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Outputs
n$\overline{OE}$	nAx	n$\overline{Y}$x
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.9	5.5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	0.5 0.5	1.7 1.7	3.0 2.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	1.9 1.9	3.0 3.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	2.8 2.3	4.1 3.4	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.5		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.7	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

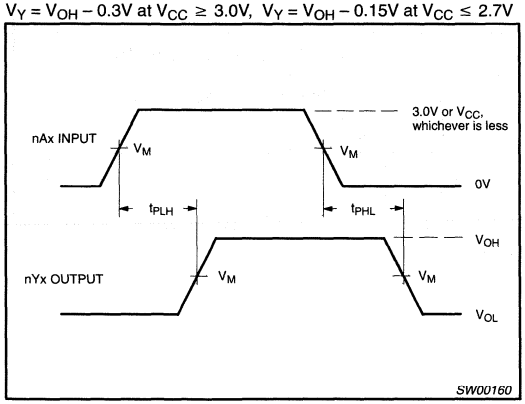
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nȲx	1	1.0 1.0	2.5 1.9	3.7 2.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.3 2.6	5.3 4.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.0 1.0	2.5 1.8	4.0 3.0	ns

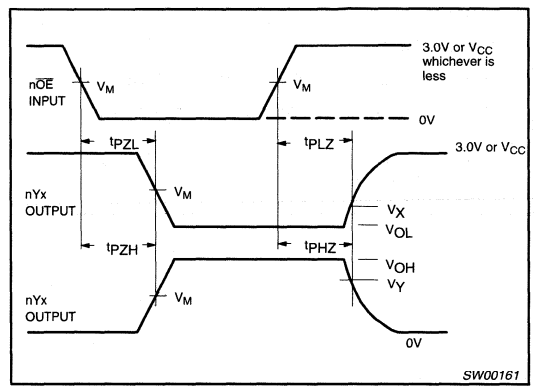
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 3.0V, $V_M = V_{CC}/2$ at $V_{CC} \leq$ 2.7V
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 3.0V, $V_X = V_{OL}$ + 0.15V at $V_{CC} \leq$ 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 3.0V, $V_Y = V_{OH}$ – 0.15V at $V_{CC} \leq$ 2.7V

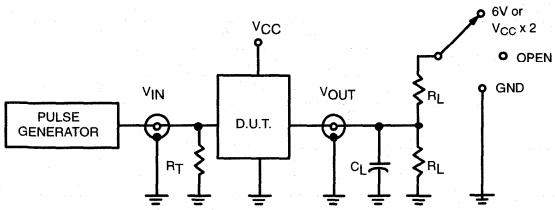


Waveform 1. Input (nAx) to Output (nȲx) Propagation Delays

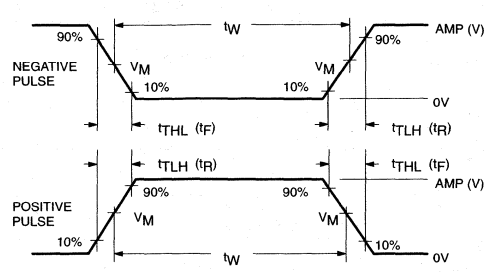


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 16-bit inverting buffer/driver with 30Ω termination resistors (3-State)

74ALVT162240

FEATURES

- 16-bit bus interface
- 5V I/O compatibile
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT162240 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

The 74ALVT162240 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

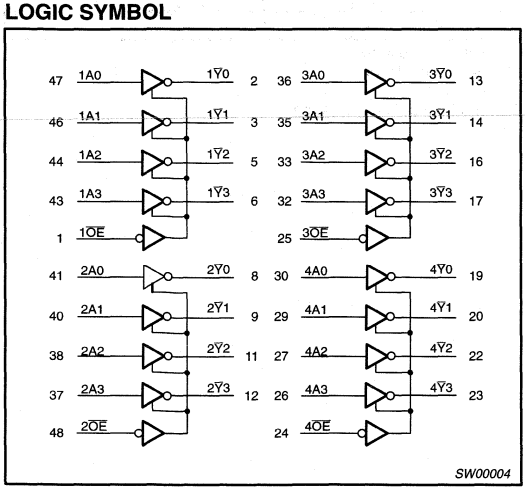
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF	3.7 2.3	2.6 2.2	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	100	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162240 DL	AV162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162240 DGG	AV162240 DGG	SOT362-1

LOGIC SYMBOL



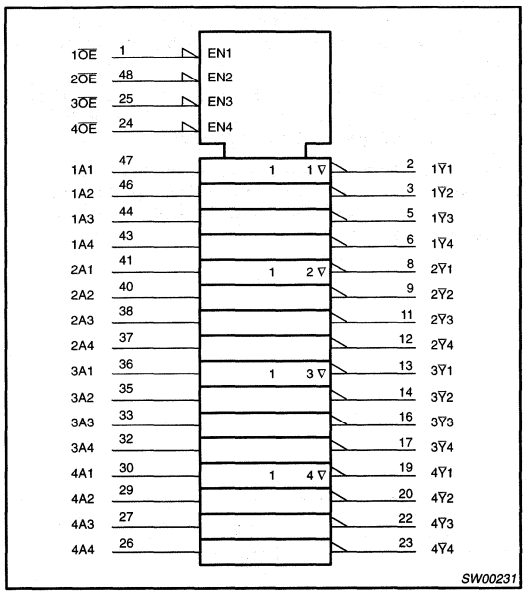
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0 - 1A3 2A0 - 2A3 3A0 - 3A3 4A0 - 4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0 - 1$\overline{Y}$3 2$\overline{Y}$0 - 2$\overline{Y}$3 3$\overline{Y}$0 - 3$\overline{Y}$3 4$\overline{Y}$0 - 4$\overline{Y}$3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

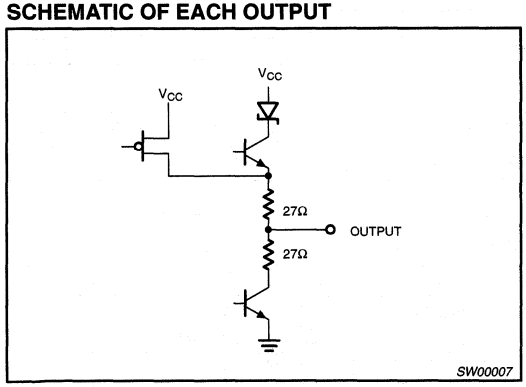
2.5V/3.3V 16-bit inverting buffer/driver with 30Ω termination resistors (3-State)

74ALVT162240

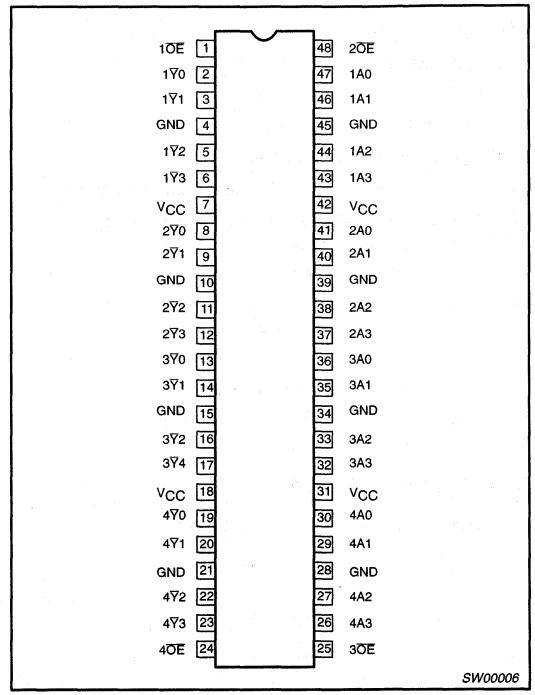
LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



PIN CONFIGURATION



FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	$n\overline{Y}x$
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = −18mA			−0.85	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = −12mA		2.0	2.5	2.5	V
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA			0.5	0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3.0V; V_I = 0.8V		75	130		µA
		V_{CC} = 3.0V; V_I = 2.0V		−75	−140		
		V_I = 0V to 3.6V; V_{CC}= 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	−5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.6	5.5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.1	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.0 1.0	2.6 2.2	4.3 3.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	3.3 2.5	5.2 3.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.0 2.4	4.4 3.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3V; I_{OH} = –8mA		1.7			V
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 12mA			0.5	0.7	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.5V; V_I = 0.7V			90		µA
		V_{CC} = 2.5V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.6	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.1	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

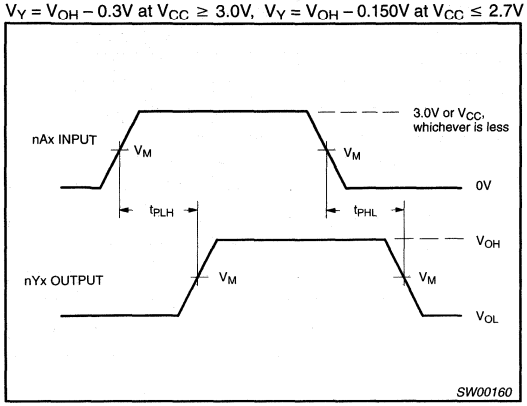
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 2.5V ±0.2V MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay nAx to nBx or nBx to nAx	1	1.0	3.7	5.4	ns
t_{PHL}			1.0	2.3	3.5	
t_{PZH}	Output enable time to High and Low level	2	1.5	4.5	6.8	ns
t_{PZL}			1.5	3.1	4.9	
t_{PHZ}	Output disable time from High and Low Level	2	1.5	2.8	4.4	ns
t_{PLZ}			1.0	2.0	3.3	

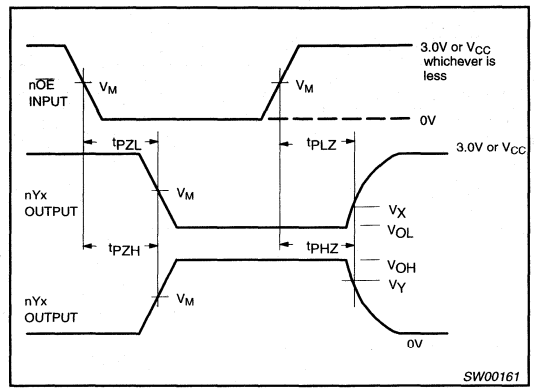
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 3.0V, $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V, $V_X = V_{OL}$ + 0.150V at V_{CC} ≤ 2.7V
$V_Y = V_{OH}$ − 0.3V at V_{CC} ≥ 3.0V, $V_Y = V_{OH}$ − 0.150V at V_{CC} ≤ 2.7V

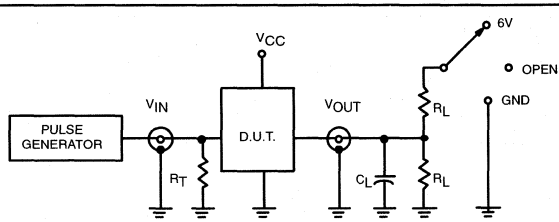


Waveform 1. Input (nAx) to Output (n$\overline{Y}$x) Propagation Delays

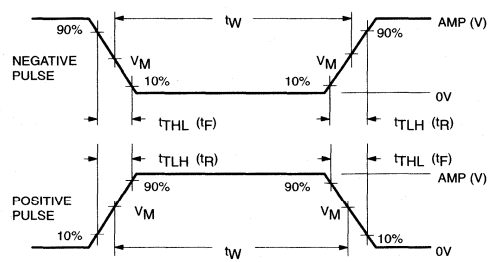


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00232

2.5V/3.3V 16-bit buffer/driver (3-State) 74ALVT16241

FEATURES

- 16-bit bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16241 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, 2OE, 3OE, $4\overline{OE}$), each controlling four of the 3-State outputs.

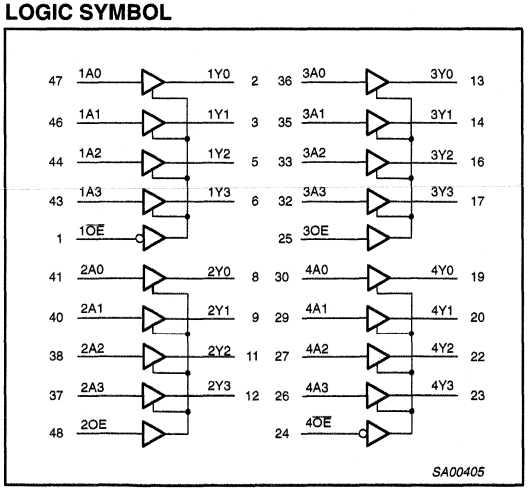
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF	1.6 1.6	1.2 1.3	ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output pin capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

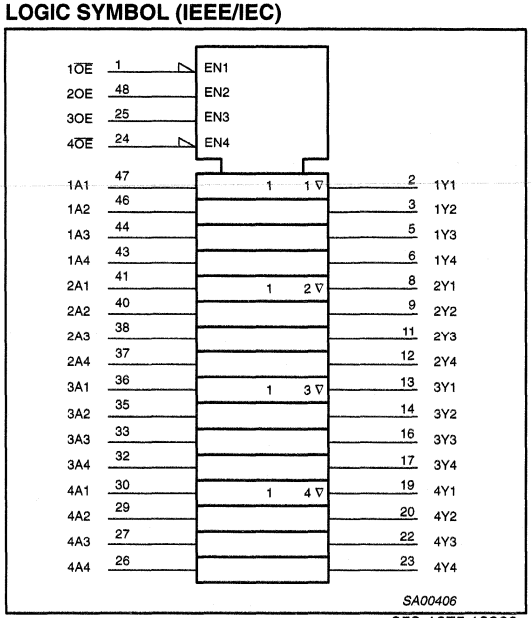
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16241 DL	AV16241 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16241 DGG	AV16241 DGG	SOT362-1

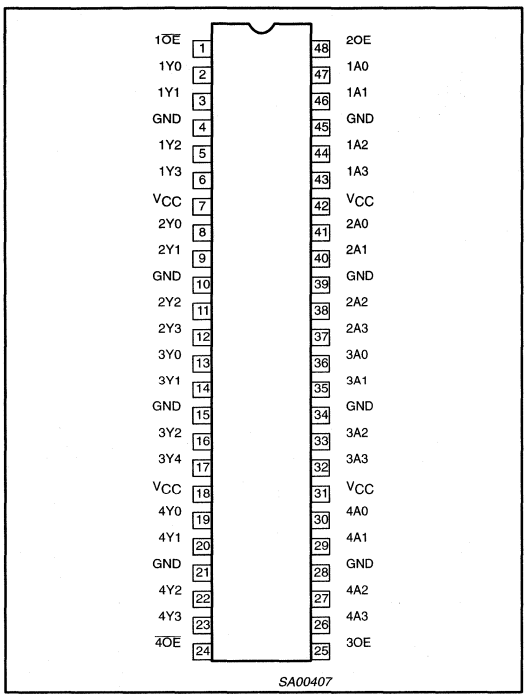
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0-1$\overline{Y}$3 2$\overline{Y}$0-2$\overline{Y}$3 3$\overline{Y}$0-3$\overline{Y}$3 4$\overline{Y}$0-4$\overline{Y}$3	Data outputs
1, 48, 25, 24	1$\overline{OE}$, 2OE, 3OE, 4$\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Outputs
1$\overline{OE}$, 4$\overline{OE}$	1Ax, 4Ax	1Yx, 4Yx
L	H	H
L	L	L
H	X	Z

Inputs		Outputs
2OE, 3OE	2Ax, 3Ax	2Yx, 3Yx
H	H	H
H	L	L
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	µA
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	0.5 0.5	1.2 1.3	1.9 2.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 0.5	2.2 1.6	3.9 2.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.0	2.9 2.5	5.4 4.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.5V; V_I = 0.7V			90		µA
		V_{CC} = 2.5V; V_I = 1.7V			–70		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

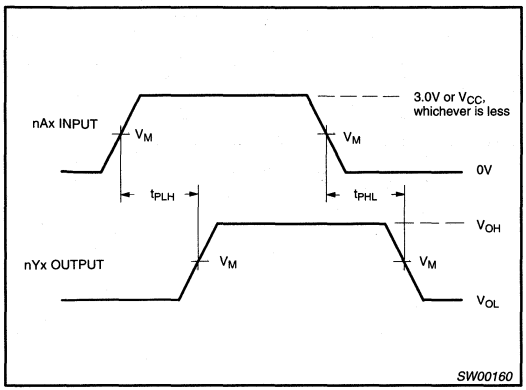
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 2.5V ±0.2V MIN	TYP[1]	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	0.5 0.5	1.6 1.6	2.6 2.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.0	3.1 2.2	5.1 4.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.0 0.5	2.9 2.3	5.7 5.0	ns

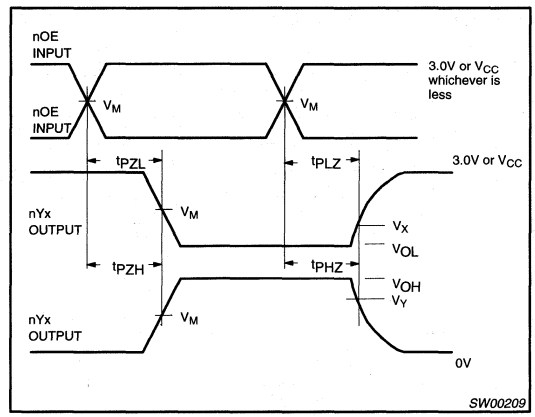
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 3.0V; V_M = V_{CC}/2 at V_{CC} ≤ 2.7V
V_X = V_{OL} + 0.3V at V_{CC} ≥ 3.0V; V_X = V_{OL} + 0.15V at V_{CC} ≤ 2.7V
V_Y = V_{OH} – 0.3V at V_{CC} ≥ 3.0V; V_Y = V_{OH} – 0.15V at V_{CC} ≤ 2.7V

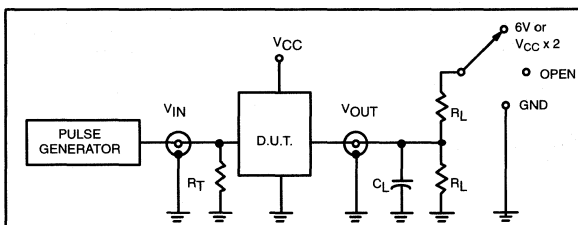


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

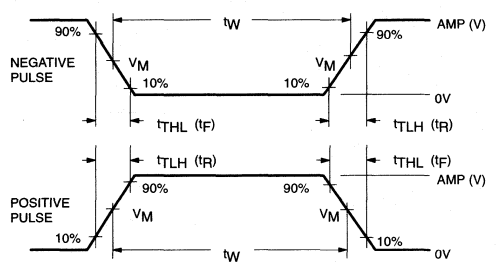


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 16-bit buffer/driver with 30Ω termination resistors (3-State)

74ALVT162241

FEATURES

- 16-bit bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT162241 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1$\overline{OE}$, 2OE, 3OE, 4$\overline{OE}$), each controlling four of the 3-State outputs.

The 74ALVT162241 is designed with 30Ω series resistance in both High and Low output stages. This design reduces the line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters. The series termination resistors reduce overshoot and undershoot and are ideal for driving memory arrays.

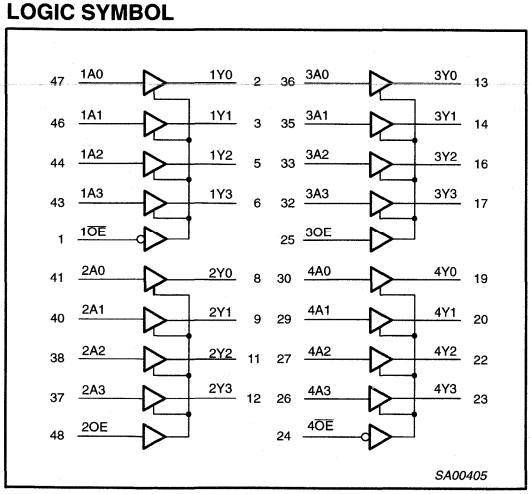
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF	3.1 2.3	2.2 2.0	ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output pin capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

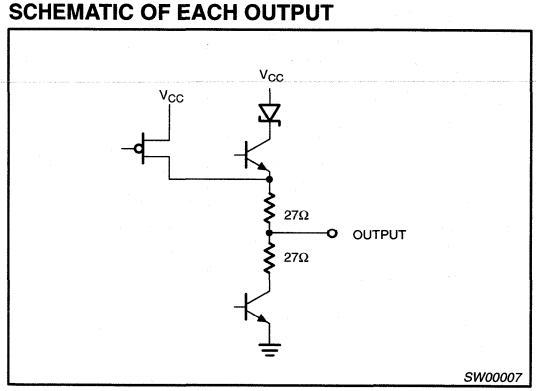
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162241 DL	AV162241 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162241 DGG	AV162241 DGG	SOT362-1

LOGIC SYMBOL



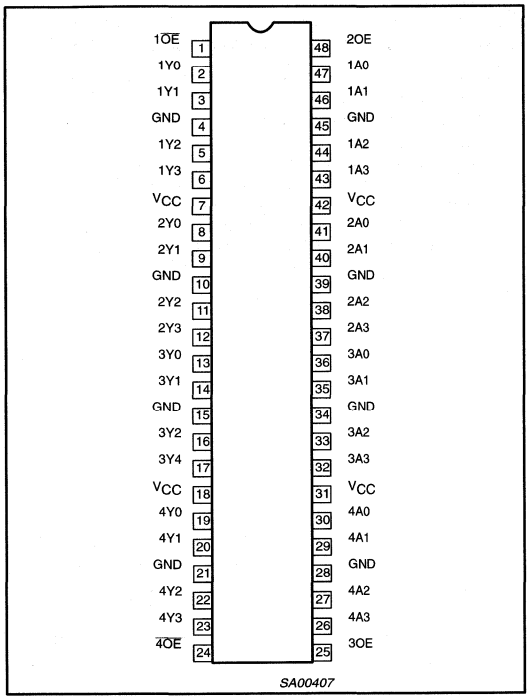
SCHEMATIC OF EACH OUTPUT



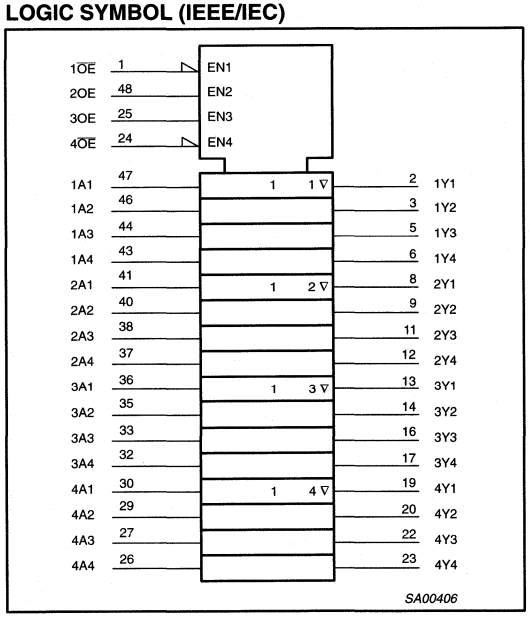
2.5V/3.3V 16-bit buffer/driver with 30Ω termination resistors (3-State)

74ALVT162241

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	$1\overline{Y}0$-$1\overline{Y}3$ $2\overline{Y}0$-$2\overline{Y}3$ $3\overline{Y}0$-$3\overline{Y}3$ $4\overline{Y}0$-$4\overline{Y}3$	Data outputs
1, 48, 25, 24	$1\overline{OE}$, 2OE, 3OE, $4\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive suppiy voltage

FUNCTION TABLE

Inputs		Outputs
$1\overline{OE}$, $4\overline{OE}$	1Ax, 4Ax	1Yx, 4Yx
L	H	H
L	L	L
H	X	Z

Inputs		Outputs
2OE, 3OE	2Ax, 3Ax	2Yx, 3Yx
H	H	H
H	L	L
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0	2.3		V
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA			0.5	0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	µA
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3.0V; V_I = 0.8V		75	130		µA
		V_{CC} = 3.0V; V_I = 2.0V		–75	200		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay nAx to n$\overline{Y}$x	1	0.5	2.2	3.6	ns
t_{PHL}			0.5	2.0	3.0	
t_{PZH}	Output enable time to High and Low level	2	1.0	3.9	5.8	ns
t_{PZL}			0.5	2.6	4.0	
t_{PHZ}	Output disable time from High and Low Level	2	1.5	4.1	6.6	ns
t_{PLZ}			1.0	2.9	5.3	

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3V; I_{OH} = –8mA		1.7	2.1		V
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 12mA			0.5	0.7	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}[6]	Bus Hold current	V_{CC} = 2.5V; V_I = 0.7V			90		µA
	Data inputs	V_{CC} = 2.5V; V_I = 1.7V			–70		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

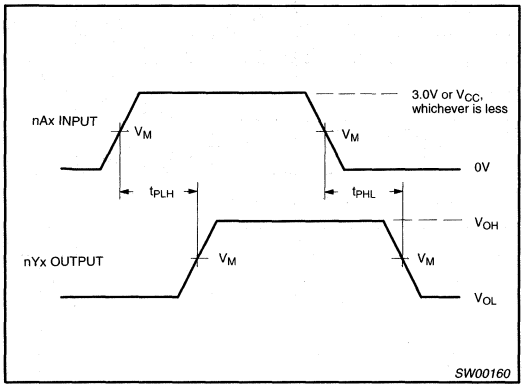
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 2.5V ±0.2V MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay nAx to n$\overline{Y}$x	1	0.5	3.1	4.6	ns
t_{PHL}			0.5	2.3	3.6	
t_{PZH}	Output enable time to High and Low level	2	1.5	4.8	7.5	ns
t_{PZL}			1.0	3.4	6.0	
t_{PHZ}	Output disable time from High and Low Level	2	1.0	4.5	8.3	ns
t_{PLZ}			0.5	3.0	6.3	

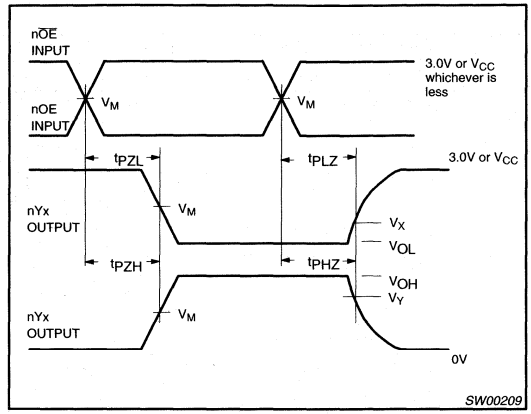
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 3.0V; $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V; $V_X = V_{OL}$ + 0.15V at V_{CC} ≤ 2.7V
$V_Y = V_{OH}$ − 0.3V at V_{CC} ≥ 3.0V; $V_Y = V_{OH}$ − 0.15V at V_{CC} ≤ 2.7V

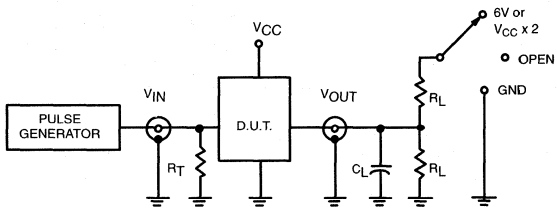


Waveform 1. Input (nAx) to Output (nȲx) Propagation Delays

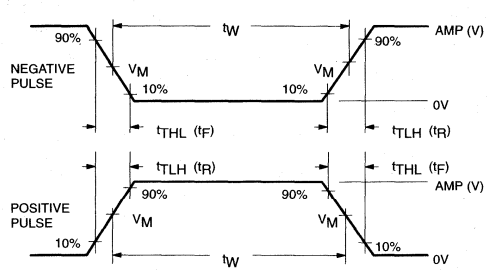


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 16-bit buffer/driver (3-State) 74ALVT16244

FEATURES

- 16-bit bus interface
- 5V I/O compatibile
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16244 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-State bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

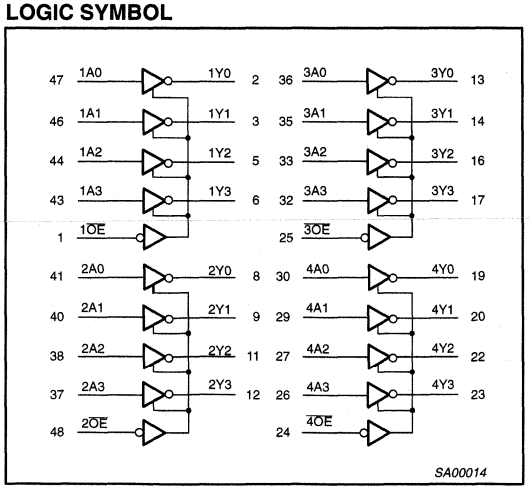
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF	1.8 1.9	1.5 1.5	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

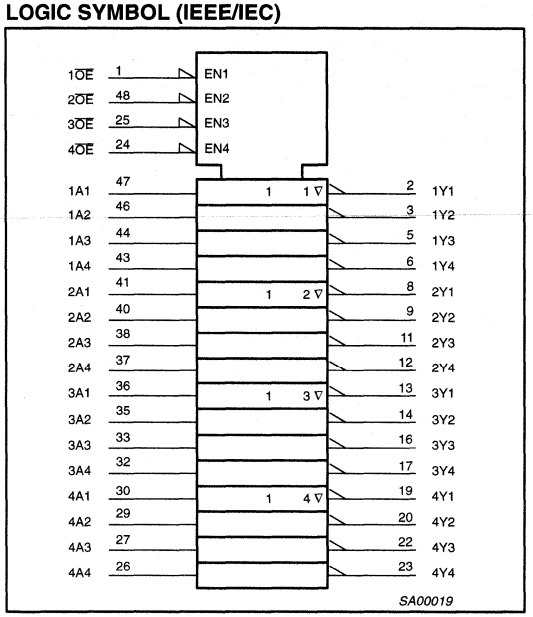
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16244 DL	AV16244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16244 DGG	AV16244 DGG	SOT362-1

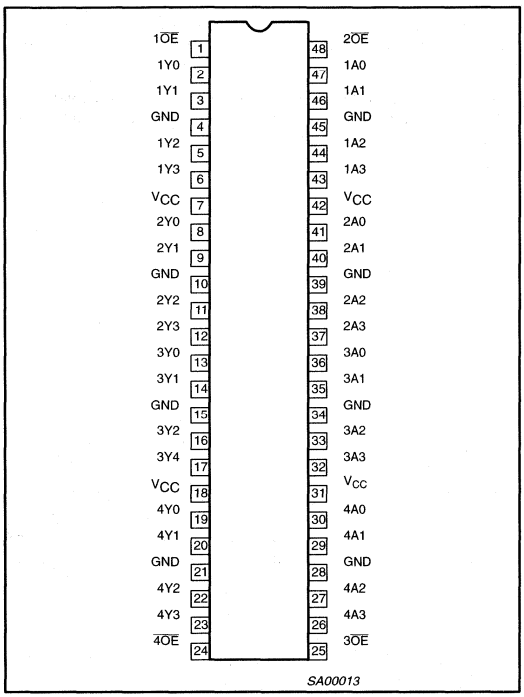
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



SA00013

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 - 1A3, 2A0 - 2A3, 3A0 - 3A3, 4A0 - 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 - 1Y3, 2Y0 - 2Y3, 3Y0 - 3Y3, 4Y0 - 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			01.	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.6	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.8 0.8	1.5 1.5	2.4 2.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 0.5	2.3 1.8	3.8 2.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	2.7 2.3	4.2 3.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 2.7V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.5		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			115		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.5	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

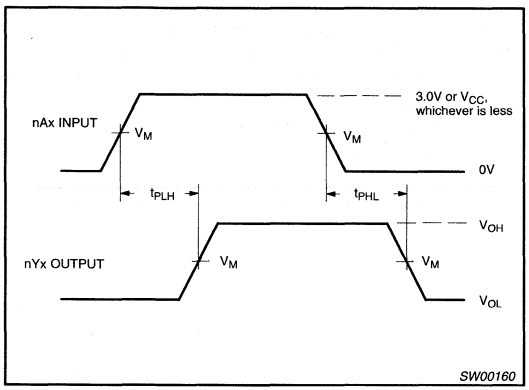
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	1.8 1.9	3.0 3.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	2.0 1.5	3.1 2.5	5.9 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.0	2.7 2.0	4.4 3.4	ns

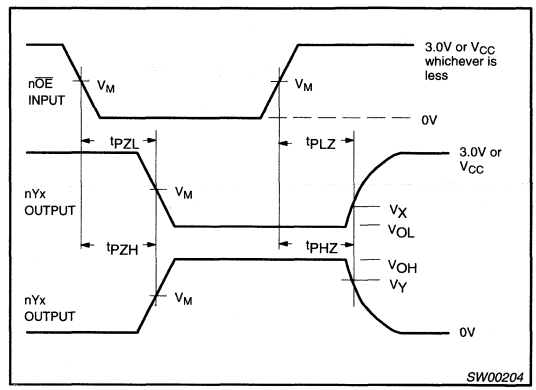
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 3.0V; $V_M = V_{CC}/2$ at $V_{CC} \leq$ 2.7V
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 3.0V; $V_X = V_{OL}$ + 0.15V at $V_{CC} \leq$ 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 3.0V; $V_Y = V_{OH}$ – 0.15V at $V_{CC} \leq$ 2.7V

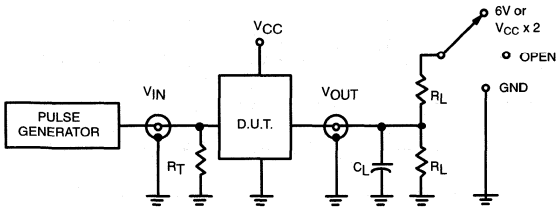


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

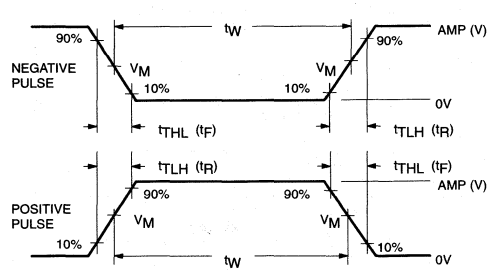


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 16-bit buffer/driver with 30Ω termination resistors (3-State)

74ALVT162244

FEATURES

- 16-bit bus interface
- 3-State buffers
- 5V I/O compatibile
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external terminating resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT162244 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

The 74ALVT162244 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

This device is a 16-bit buffer and line driver featuring non-inverting 3-State bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

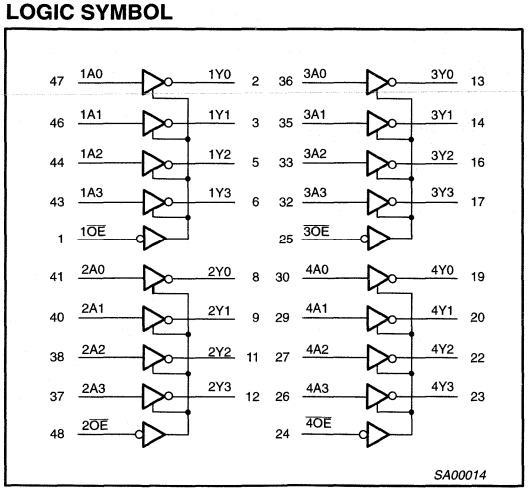
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF	2.7 2.3	2.2 2.2	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162244 DL	AV162244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162244 DGG	AV162244 DGG	SOT362-1

LOGIC SYMBOL



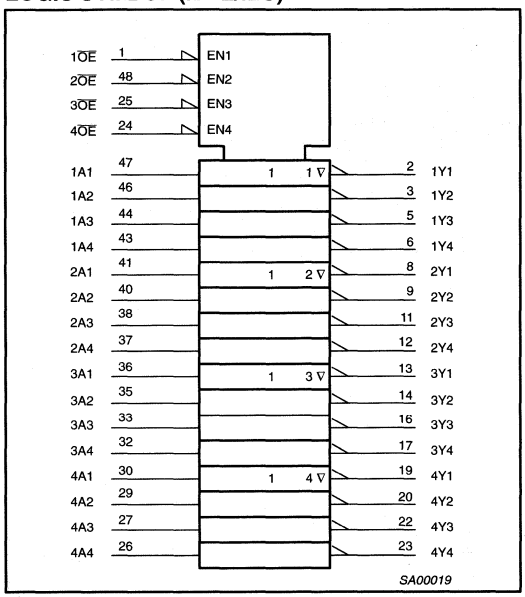
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 - 1A3, 2A0 - 2A3, 3A0 - 3A3, 4A0 - 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 - 1Y3, 2Y0 - 2Y3, 3Y0 - 3Y3, 4Y0 - 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

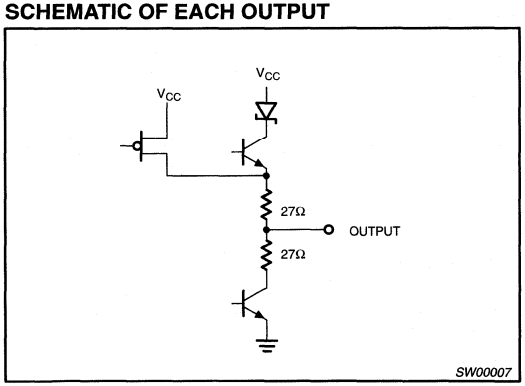
2.5V/3.3V 16-bit buffer/driver with 30Ω termination resistors (3-State)

74ALVT162244

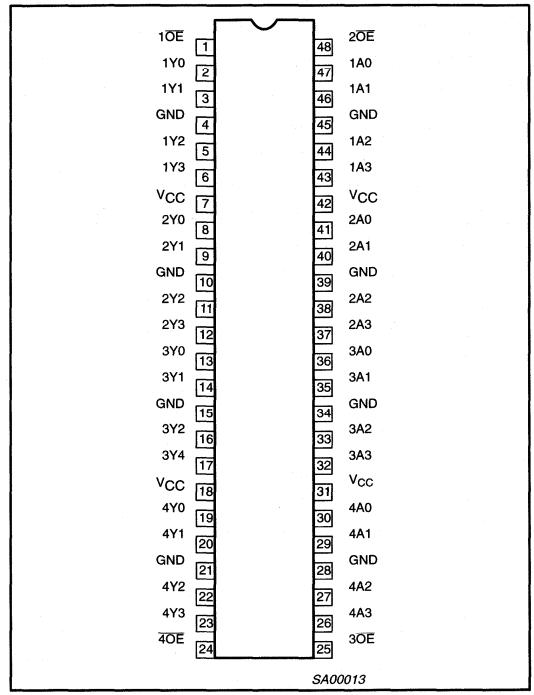
LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



PIN CONFIGURATION



FUNCTION TABLE

INPUTS		OUTPUTS
nOE	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0	2.5		V
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA			0.5	0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			01.	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.7	5.0	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.05	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.0 1.0	2.2 2.2	3.3 3.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	3.2 2.4	4.9 3.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.1 2.5	4.7 4.1	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3V; I_{OH} = –8mA		1.7			V
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 12mA			0.6	0.7	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	µA
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	µA
		V_{CC} = 2.7V; V_I = 0			0.1	-5	µA
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			115		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.5	4.5	mA
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

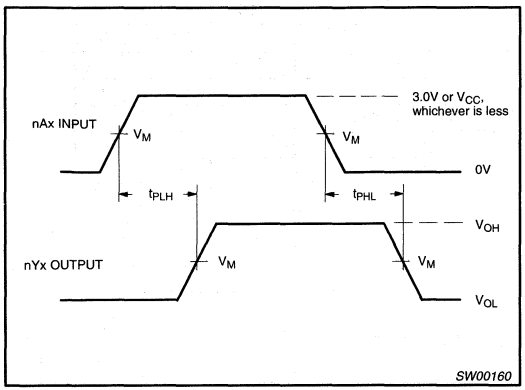
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 2.5V ±0.2V MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay nAx to nBx or nBx to nAx	1	1.5	2.7	4.2	ns
t_{PHL}			1.5	2.3	3.7	ns
t_{PZH}	Output enable time to High and Low level	2	2.0	4.4	6.8	ns
t_{PZL}			2.0	3.0	5.1	ns
t_{PHZ}	Output disable time from High and Low Level	2	1.0	2.8	4.6	ns
t_{PLZ}			1.0	2.0	3.3	ns

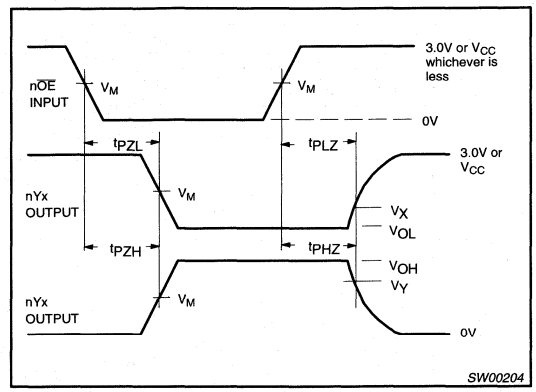
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 3.0V; $V_M = V_{CC}/2$ at $V_{CC} \leq$ 2.7V
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 3.0V; $V_X = V_{OL}$ + 0.15V at $V_{CC} \leq$ 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 3.0V; $V_Y = V_{OH}$ – 0.15V at $V_{CC} \leq$ 2.7V

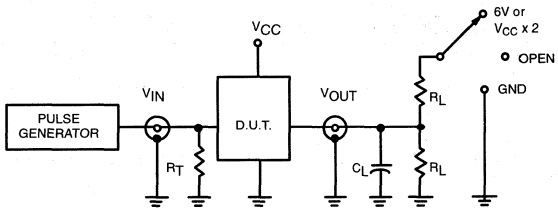


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

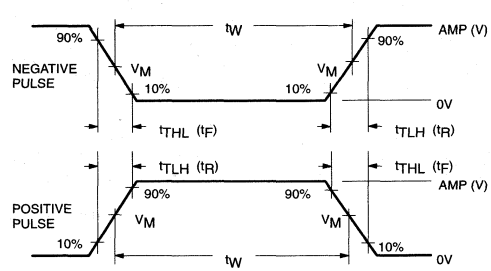


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 16-bit transceiver (3-State) 74ALVT16245

FEATURES

- 16-bit bidirectional bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 400V per Machine Model

DESCRIPTION

The 74ALVT16245 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

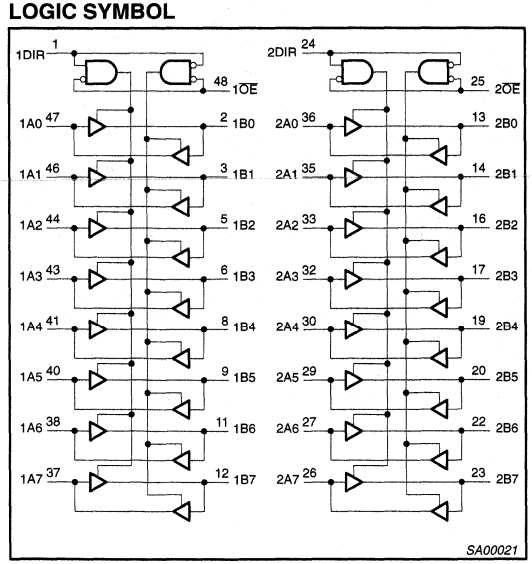
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF	1.7 1.9	1.5 1.5	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

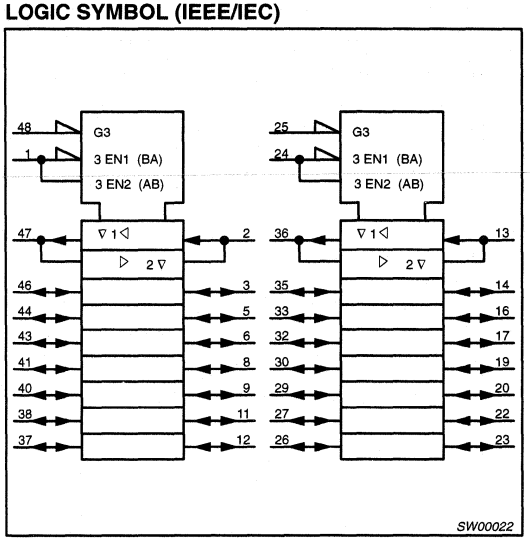
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16245 DL	AV16245 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16245 DGG	AV16245 DGG	SOT362-1

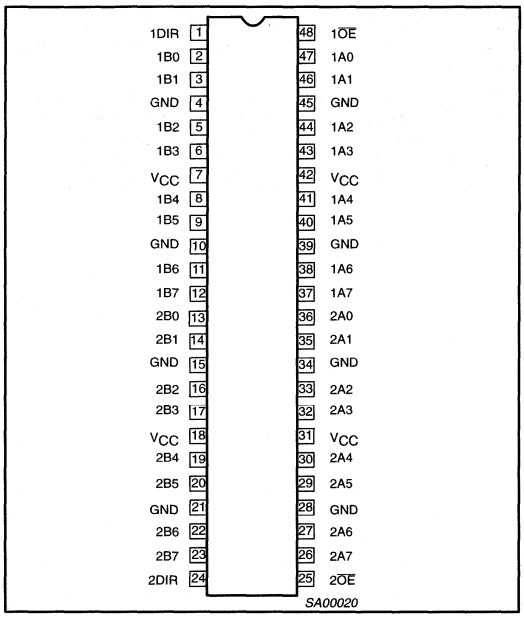
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	$n\overline{OE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B ports[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq 1.2V$; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.2	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.2	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	0.5 0.5	1.5 1.5	2.4 2.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.1 1.7	3.5 2.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.4 2.8	4.5 3.7	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

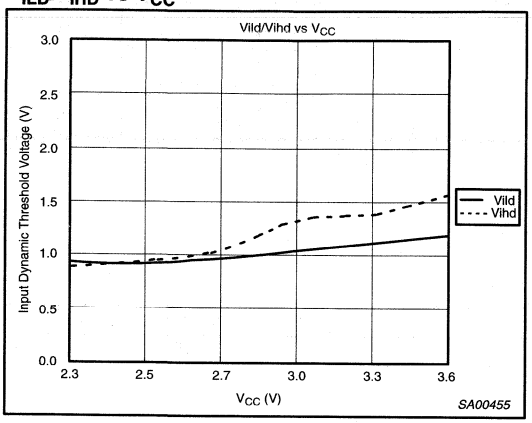
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	45	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.1	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

DYNAMIC SWITCHING THRESHOLD

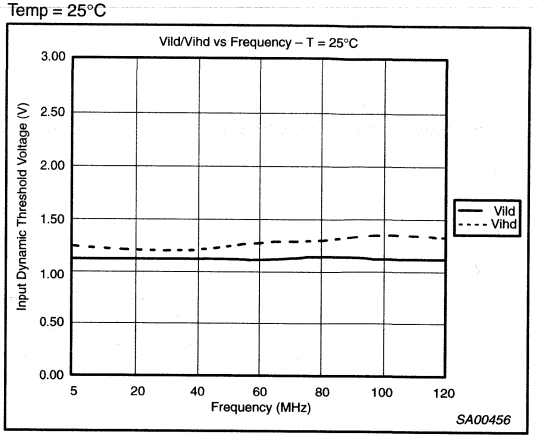
Dynamic switching threshold is the change in V_{IH} and V_{IL} when the device is operated in various switching and output loading conditions. The cause of this variation is due to extra load placed on internal circuit structures. V_{IHD} and V_{ILD} are measures of the dynamic switching threshold. V_{IHD} is the input high switching level when the device is heavily loaded. V_{ILD} is the input low switching level when the device is heavily loaded.

V_{ILD}/V_{IHD} vs V_{CC}



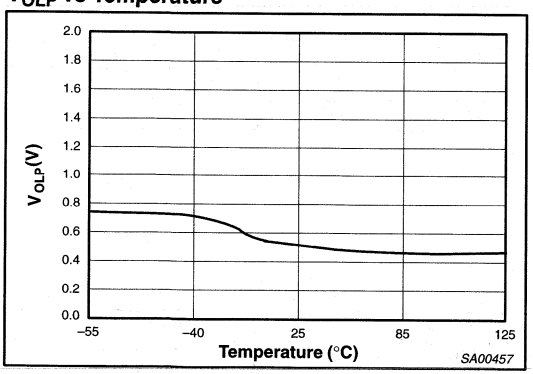
V_{ILD}/V_{IHD} vs Frequency

Temp = 25°C

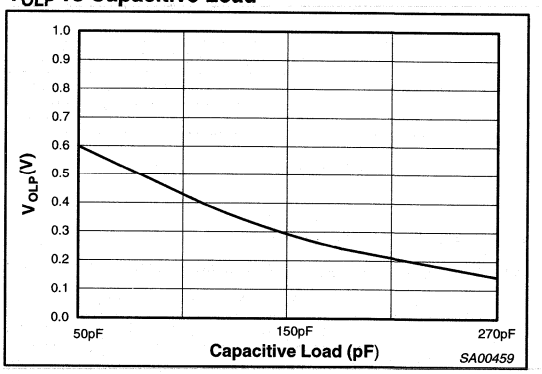


GROUND/V_{CC} BOUNCE

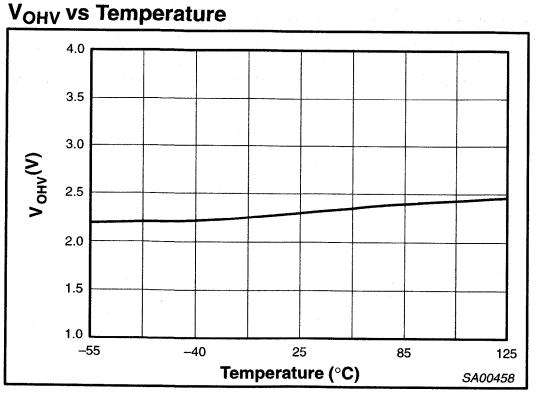
V_{OLP} vs Temperature



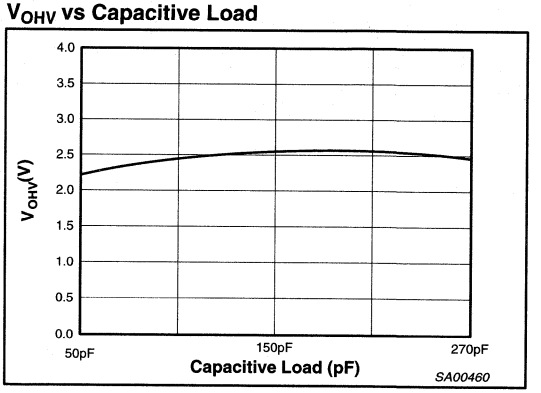
V_{OLP} vs Capacitive Load



V_{OHV} vs Temperature



V_{OHV} vs Capacitive Load



AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	0.5 0.5	1.7 1.9	2.8 2.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.0	3.0 2.3	4.5 3.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.0	3.0 2.3	4.6 3.5	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

SKEW DATA

t_{ps} (Pin Skew or Transition Skew)

$t_{PS} = | t_{PHL} - t_{PLH} |$

	V_{CC} = 2.3	V_{CC} = 2.5	V_{CC} = 2.7	V_{CC} = 3.0	V_{CC} = 3.3	V_{CC} = 3.6	UNITS
$t_{PS\ Max}$	429	469	430	426	267	336	ps

$t_{OST} = | t_{P\Phi m} - t_{P\Phi n} |$

Where Φ is any edge transition (high-to-low or low-to-high) measured between any two outputs (m or n) within any given device.

	V_{CC} = 2.3	V_{CC} = 2.5	V_{CC} = 2.7	V_{CC} = 3.0	V_{CC} = 3.3	V_{CC} = 3.6	UNITS
t_{OST} nAn-nBn	546	625	586	546	427	397	ps
nBn-nAn	508	547	586	506	427	417	

NOTE:
One output switching, Temp = 25°C.

t_{OSHL}, t_{OSLH}, (Common Edge Skew)

$t_{OSHL} = | t_{PHL\ max} - t_{PHL\ min} |$ (Output Skew for Low-to-High Transitions)

$t_{OSLH} = | t_{PLH\ max} - t_{PLH\ min} |$ (Output Skew for High-to-Low Transitions)

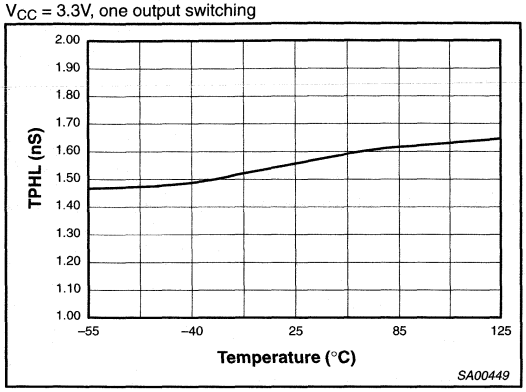
	V_{CC} = 2.3	V_{CC} = 2.5	V_{CC} = 2.7	V_{CC} = 3.0	V_{CC} = 3.3	V_{CC} = 3.6	UNITS
t_{OSLH} nAn-nBn	312	312	313	276	267	257	ps
t_{OSHL} nAn-nBn	312	352	352	297	289	267	
t_{OSLH} nBn-nAn	235	273	312	274	296	326	
t_{OSHL} nBn-nAn	234	235	274	248	287	267	

NOTE:
One output switching, Temp = 25°C.

EXTENDED DATA

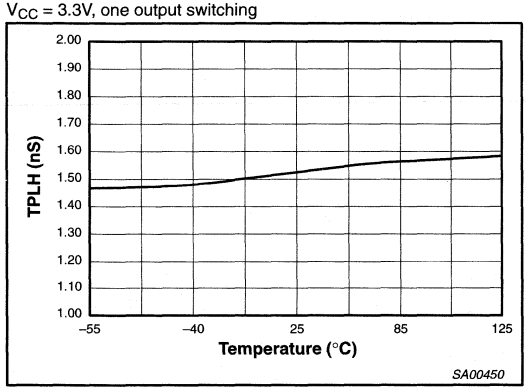
TPHL vs TEMP

V_{CC} = 3.3V, one output switching



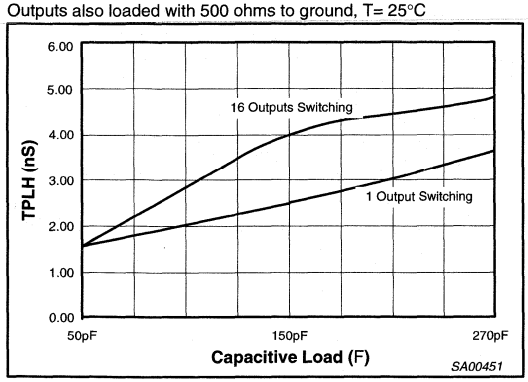
TPLH vs TEMP

V_{CC} = 3.3V, one output switching



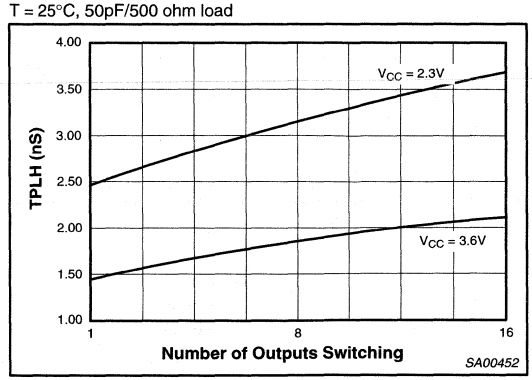
TPLH vs OUTPUT LOAD

Outputs also loaded with 500 ohms to ground, T= 25°C



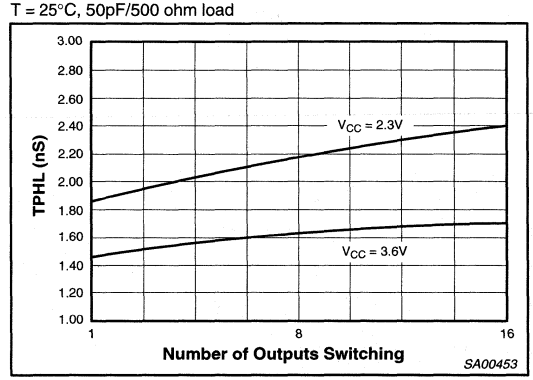
TPLH vs NUMBER of OUTPUTS SWITCHING

T = 25°C, 50pF/500 ohm load



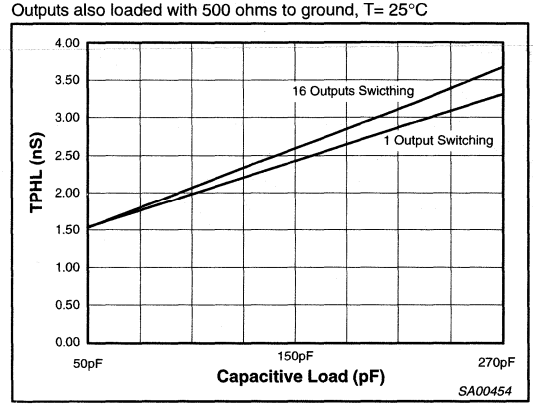
TPHL vs NUMBER of OUTPUTS SWITCHING

T = 25°C, 50pF/500 ohm load



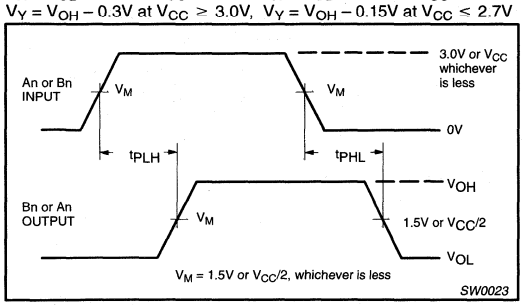
TPHL vs OUTPUT LOAD

Outputs also loaded with 500 ohms to ground, T= 25°C

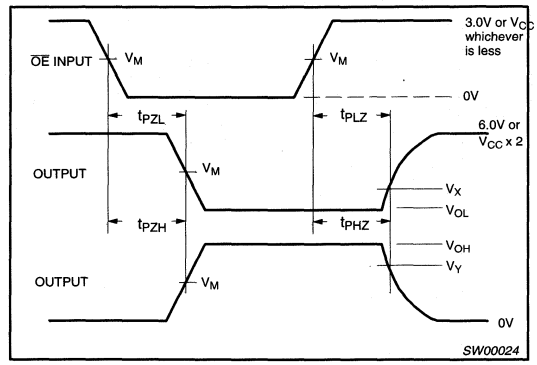


AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 3.0V, $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V, $V_X = V_{OL}$ + 0.15V at V_{CC} ≤ 2.7V
$V_Y = V_{OH}$ – 0.3V at V_{CC} ≥ 3.0V, $V_Y = V_{OH}$ – 0.15V at V_{CC} ≤ 2.7V

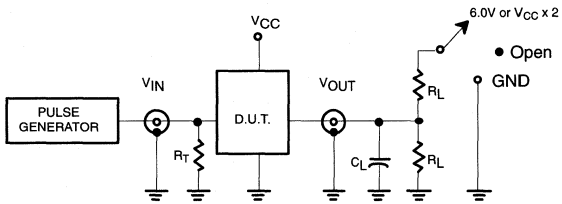


Waveform 1. Input to Output Propagation Delays

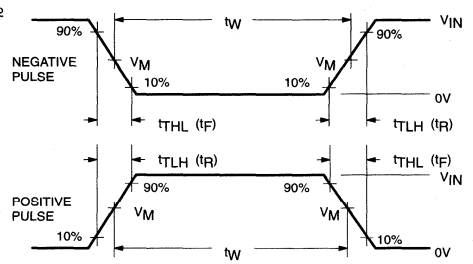


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

2.5V/3.3V 16-bit transceiver with 30Ω termination resistors (3-State)

74ALVT162245

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- 5V I/O compatibile
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT162245 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($n\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

The 74ALVT162245 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF	2.9 2.4	2.3 2.0	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

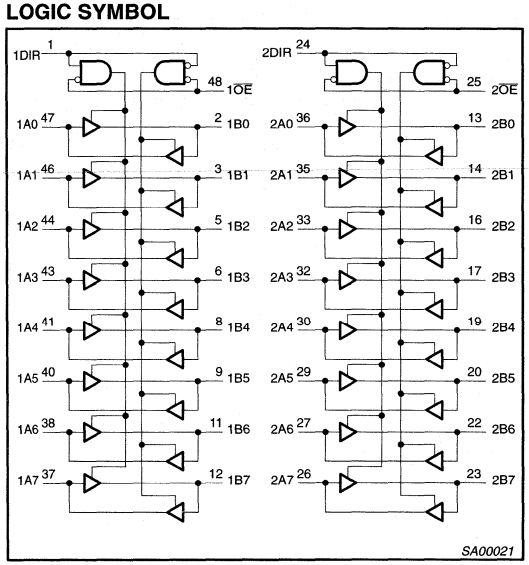
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162245 DL	AV162245 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162245 DGG	AV162245 DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	$n\overline{OE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

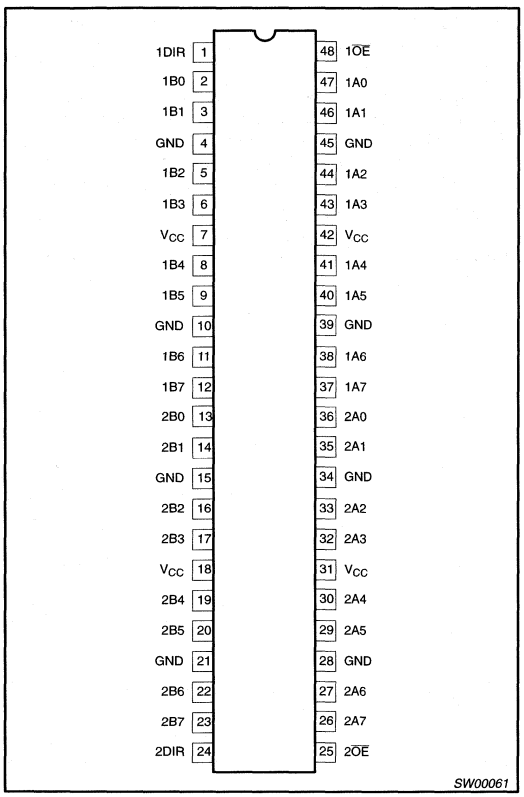
LOGIC SYMBOL



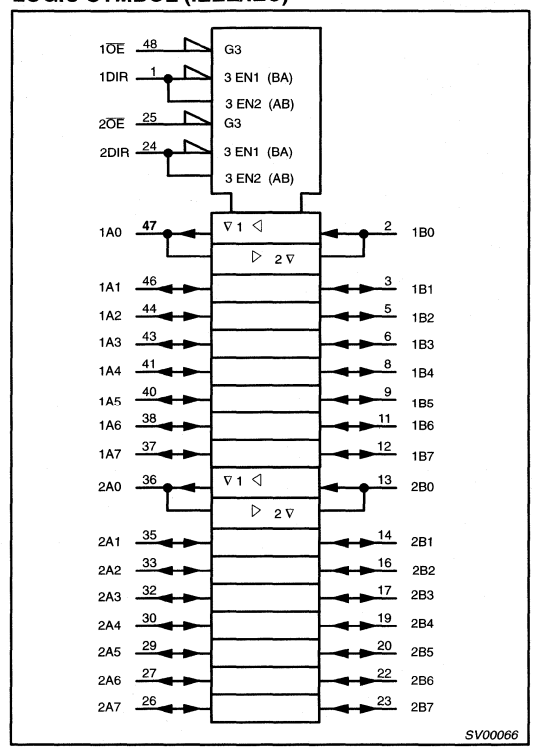
2.5V/3.3V 16-bit transceiver with 30Ω termination resistors (3-State)

74ALVT162245

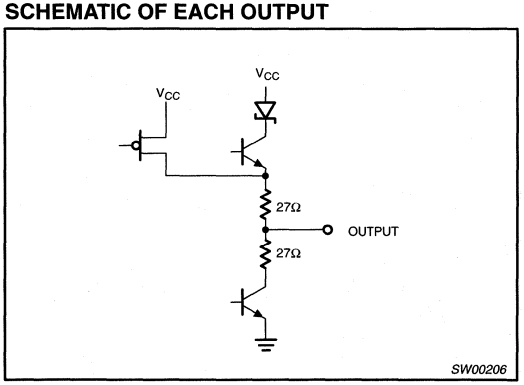
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
nOE	**nDIR**	**nAx**	**nBx**
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0	2.3		V
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA			0.6	0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			01.	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	0.5 0.5	2.3 2.0	3.6 3.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.0 2.6	5.0 3.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.0 1.0	3.6 3.0	5.2 4.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3V; I_{OH} = –8mA		1.7			V
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 12mA			0.6	0.7	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–75		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			20	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			40	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.5	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.05	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

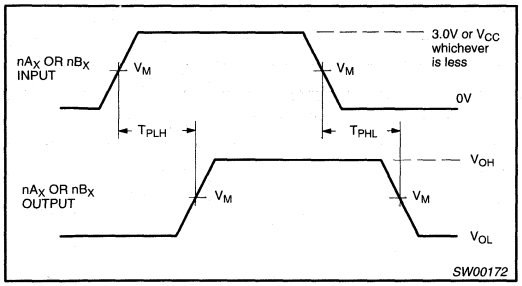
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.5 1.5	2.9 2.4	5.3 4.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	4.3 3.1	6.3 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.2 3.3	6.2 5.1	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

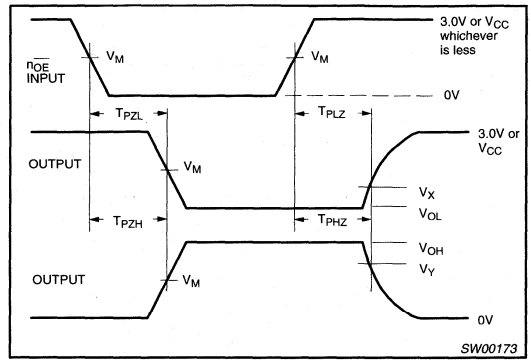
AC WAVEFORMS

NOTES:

1. $V_M = 1.5V$ at $V_{CC} \geq 3.0V$, $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7V$
2. $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 3.0V$, $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} \leq 2.7V$
3. $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 3.0V$, $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} \leq 2.7V$

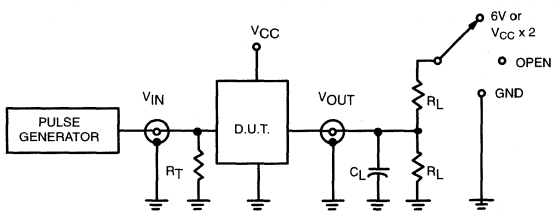


Waveform 1. Input to Output Propagation Delays

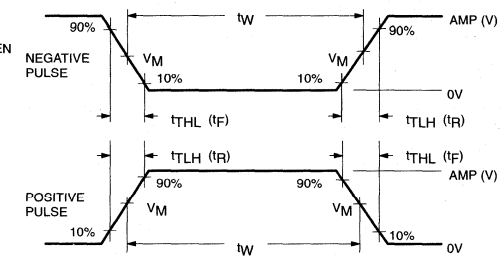


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 12-bit to 24-bit multiplexed D-type latches (3-State)

74ALVT16260

FEATURES

- ESD protection exceeds 2000V per Mil-Std-883C, Method 3015; exceeds 200V using machine model
- Latch-up protection exceeds 500mA per JEDEC Standard JESD-17.
- Distributed V_{CC} and GND pin configuration minimizes high-speed switching noise.
- Output capability (–32mA I_{OH}, 64mA I_{OL}).
- Bus hold inputs eliminate the need for external pull-up resistors.
- 5V I/O compatible
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset

DESCRIPTION

The 74ALVT16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is alto useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch enable input is high, the latch is transparent. When the latch enable input goes low, the data present at the inputs is latched and remains latched until the latch enable input is returned high.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The 74ALVT16260 is available in a 56-pin Shrink Small Outline Package (SSOP) and 56-pin Thin Shrink Small Outline Package (TSSOP).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx nBx to nAx	C_L = 50 pF	3.5 3.3	2.8 2.6	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	4	pF
C_{OUT}	Output capacitance	$V_{I/O}$ = 0 V or 5.0 V	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	100	80	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16260 DL	AV16260 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16260 DGG	AV16260 DGG	SOT364-1

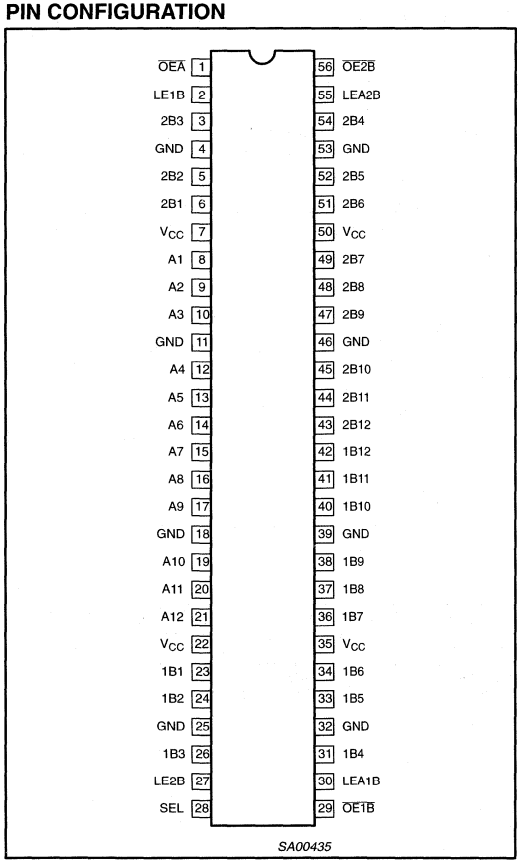
2.5V/3.3V 12-bit to 24-bit multiplexed D-type latches (3-State)

74ALVT16260

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21	An	Data inputs/outputs (A)
23, 24, 26, 31, 33, 34, 36, 37, 38, 40, 41, 42	1Bn	Data inputs/outputs (B1)
6, 5, 3, 54, 52, 51, 49, 48, 47, 45, 44, 43	2Bn	Data inputs/outputs (B2)
1, 29, 56	$\overline{OEA}$, $\overline{OE1B}$, $\overline{OE2B}$	Output enable input (active low)
2, 27, 30, 55	LE1B, LE2B, LEA1B, LEA2B	Latch enable inputs
28	SEL	B1/B2 input select input
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION



SA00435

FUNCTION TABLES

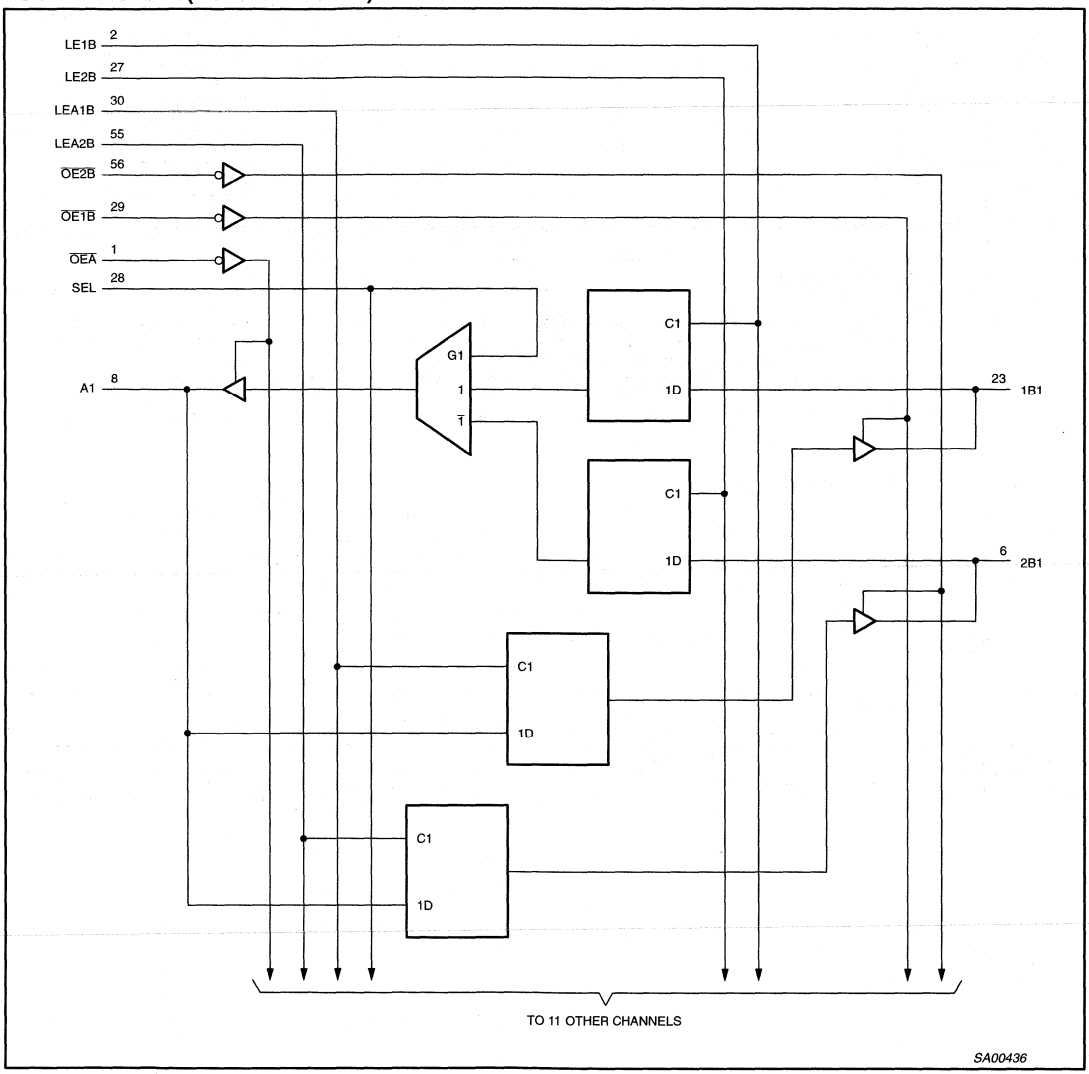
B to A ($\overline{OEB}$ = H)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A0
X	X	X	X	X	H	Z

A to B ($\overline{OEA}$ = H)

INPUTS					OUTPUT	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B0
L	H	L	L	L	L	2B0
H	L	H	L	L	1B0	H
L	L	H	L	L	1B0	L
X	L	L	L	L	1B0	2B0
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage[3]		−0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		−8		−32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = −18mA			−0.85	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = −100µA		V_{CC}−0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = −32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		−75	−140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	−5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.7	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}−0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER		T_{amb} = −40°C to +85°C V_{CC} = +3.3V ± 0.3V			UNIT
	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	
t_{PLH}	A or B	B or A	1	2.8	4.8	ns
t_{PHL}			1	2.6	4.6	ns
t_{PLH}	$\overline{LE}$	A or B	1.1	2.9	4.6	ns
t_{PHL}			1.1	3.1	4.7	ns
t_{PLH}	SEL (B1)	A	1.3	2.3	3.4	ns
	SEL (B2)	A	1.1	2.4	3.8	ns
t_{PHL}	SEL (B1)	A	1.5	2.4	3.6	ns
	SEL (B2)	A	1.6	2.4	3.6	ns
t_{PZH}	$\overline{OE}$	A or B	1	2.3	4.2	ns
t_{PZL}			1.6	2.3	4.0	ns
t_{PHZ}	$\overline{OE}$	A or B	2.2	4.4	6.0	ns
t_{PLZ}			1.3	3.1	5.0	ns

AC SETUP CHARACTERISTICS (3.3V ± 0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	T_{amb} = −40°C to +85°C V_{CC} = +3.3V ± 0.3V		UNIT
		MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	± 100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			1	100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.7	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER		T_{amb} = −40°C to +85°C V_{CC} = +2.5V ± 0.2V			UNIT
	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	
t_{PLH}	A or B	B or A	1	3.5	5.3	ns
t_{PHL}			1	3.3	5.4	ns
t_{PLH}	$\overline{LE}$	A or B	1.1	3.9	6.0	ns
t_{PHL}			1.1	4.2	6.2	ns
t_{PLH}	SEL (B1)	A	1.3	2.9	4.5	ns
	SEL (B2)	A	1.1	3.3	4.8	ns
t_{PHL}	SEL (B1)	A	1.5	3.0	4.5	ns
	SEL (B2)	A	1.6	3.2	4.6	ns
t_{PZH}	$\overline{OE}$	A or B	1	3.1	5.0	ns
t_{PZL}			1.6	2.0	3.0	ns
t_{PHZ}	$\overline{OE}$	A or B	2.2	4.0	6.6	ns
t_{PLZ}			1.3	2.0	3.4	ns

AC SETUP CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	T_{amb} = −40°C to +85°C V_{CC} = +2.5V ± 0.2V		UNIT
		MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		ns

AC WAVEFORMS

V_M = 1.5V for all waveforms

The outputs are measured one at a time with one transition per measurement.

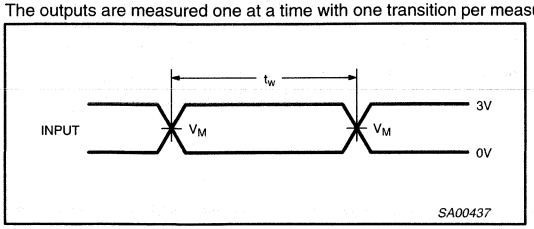


Figure 1. Pulse duration

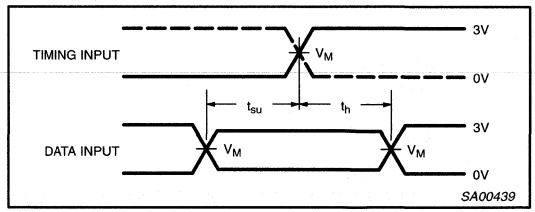
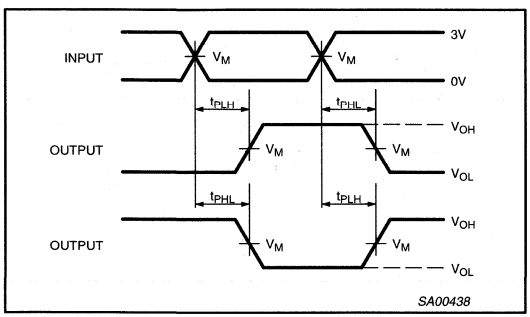
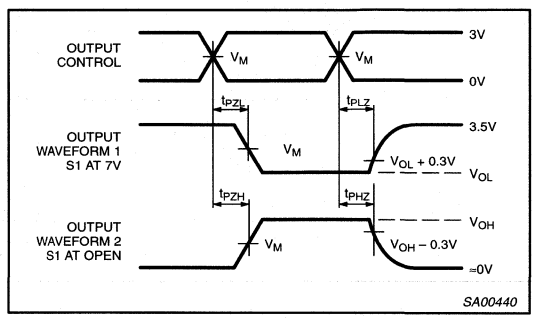


Figure 3. Setup and hold times



All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r ≤ 2.5ns, t_f ≤ 2.5ns.

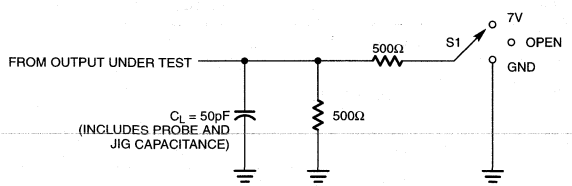
Figure 2. Propagation delay times; inverting and non-inverting outputs



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 4. Enable and disable times; low- and high-level enabling

TEST LOAD CIRCUIT



Load Circuit for Outputs

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7V
t_{PHZ}/t_{PZH}	Open

SA00441

Figure 5. Test load circuit

2.5V/3.3V 1-to-4 address driver (3-State) 74ALVT16344

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- 5V I/O Compatible
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ALVT16344 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT16344 is a 1-to-4 address driver used in applications where four separate memory locations must be addressed by a single address.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF	2.3	1.8	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

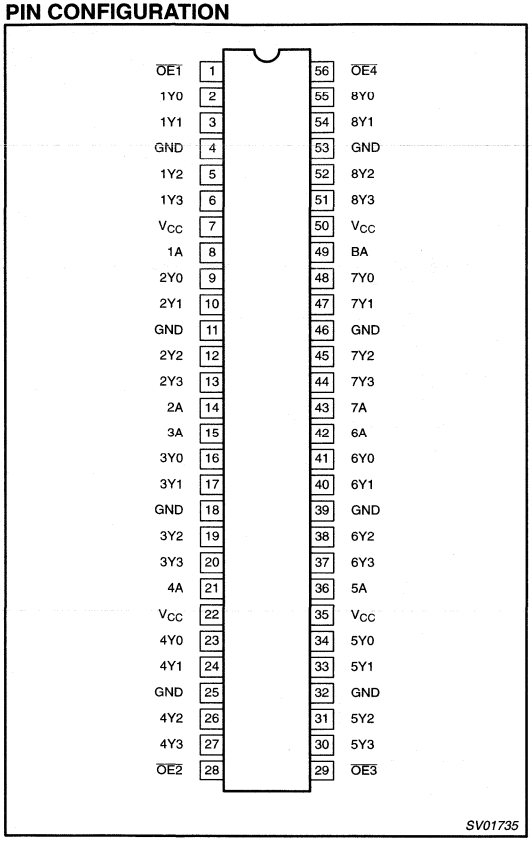
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16344 DL	AV16344 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16344 DGG	AV16344 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 14, 15, 21, 36, 42, 43, 49	nA	Data inputs
2, 3, 5, 6, 9, 10, 12, 13, 16, 17, 19, 20, 23, 24, 26, 27, 30,31, 33, 34, 37, 38, 40, 44, 45, 47, 48, 51, 52, 54, 55,	nY_X	Data outputs
1, 28, 29, 56	$\overline{OE}$	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION

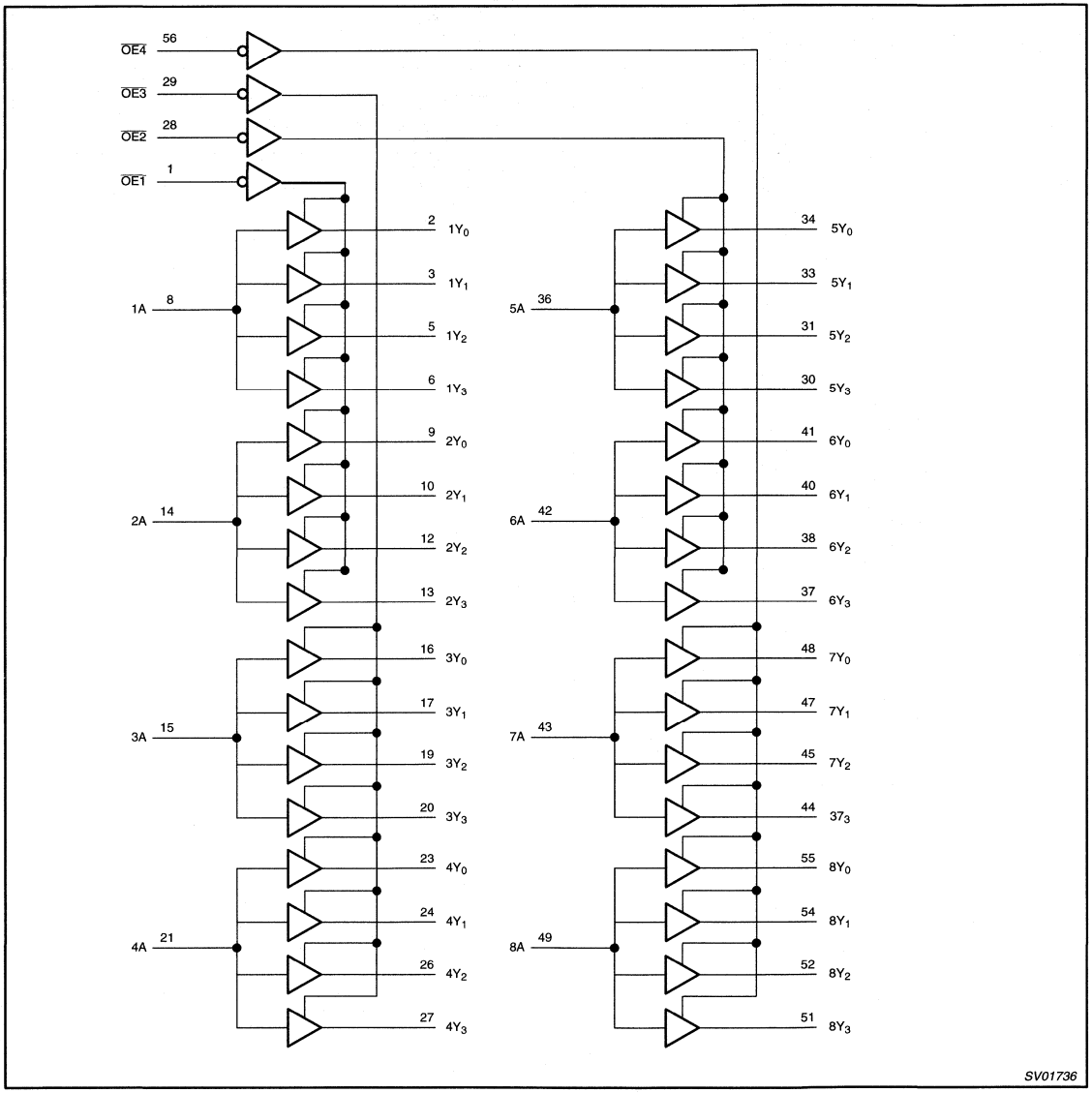


FUNCTION TABLE

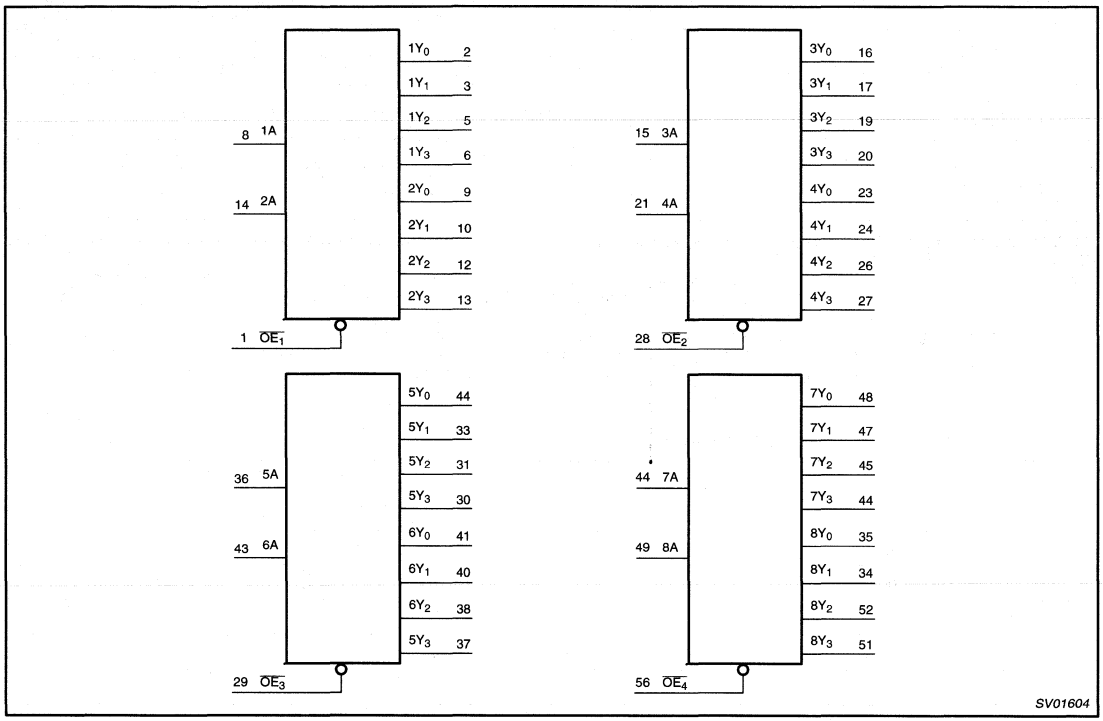
INPUTS		OUTPUTS	OPERATING MODE
$\overline{OE}$	nA	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = High voltage level
L = Low voltage level

LOGIC DIAGRAM



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A inputs	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.2	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = -40 to +85°C, V_{CC} = +3.3V ±0.3V MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	1.8 1.8	2.8 2.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 0.5	2.2 1.6	3.8 2.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.0 1.0	3.2 2.5	4.8 3.8	ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 2.7V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.7	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}[6]	Bus Hold current A inputs	V_{CC} = 2.5V; V_I = 0.8V			115		µA
		V_{CC} = 2.5V; V_I = 2.0V			10		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.6	5.0	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

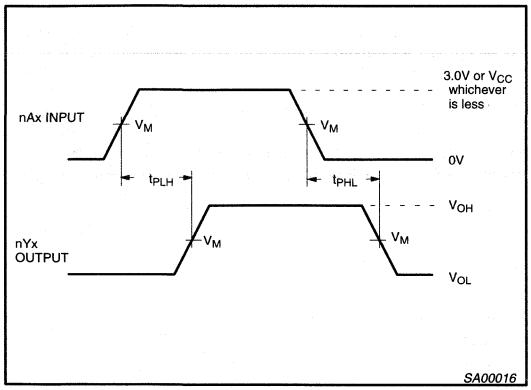
AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

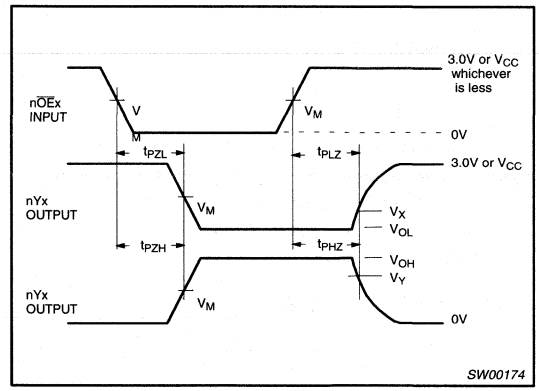
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	2.2 2.3	3.3 3.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.1 2.1	5.5 4.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.0 1.0	3.1 2.3	5.1 3.9	ns

AC WAVEFORMS

V_M = 1.5V for $V_{CC} \geq$ 3.0V; $V_M = V_{CC}/2$ for $V_{CC} \leq$ 2.7V
$V_X = V_{OL}$ + 0.3V for $V_{CC} \geq$ 3.0V; $V_X = V_{OL}$ + 0.15V for $V_{CC} \leq$ 2.7V
$V_Y = V_{OH} - 0.3V$ for $V_{CC} \geq$ 3.0V; $V_Y = V_{OH} - 0.15V$ for $V_{CC} \leq$ 2.7V

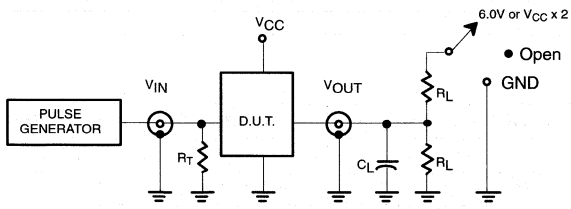


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

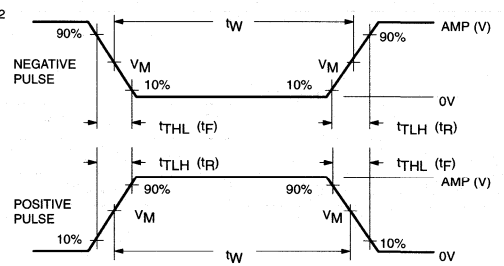


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC *CHARACTERISTICS for value.*

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00205

2.5V/3.3V 1-to-4 address driver with 30Ω termination resistors (3-State)

74ALVT162344

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- 5V I/O Compatible
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Outputs include series resistance of 30Ω making external termination resistors unnecessary

DESCRIPTION

The 74ALVT162344 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT162344 is a 1-to-4 address driver used in applications where four separate memory locations must be addressed by a single address.

The 74ALVT162344 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF	2.3	1.8	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162344 DL	AV162344 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162344 DGG	AV162344 DGG	SOT364-1

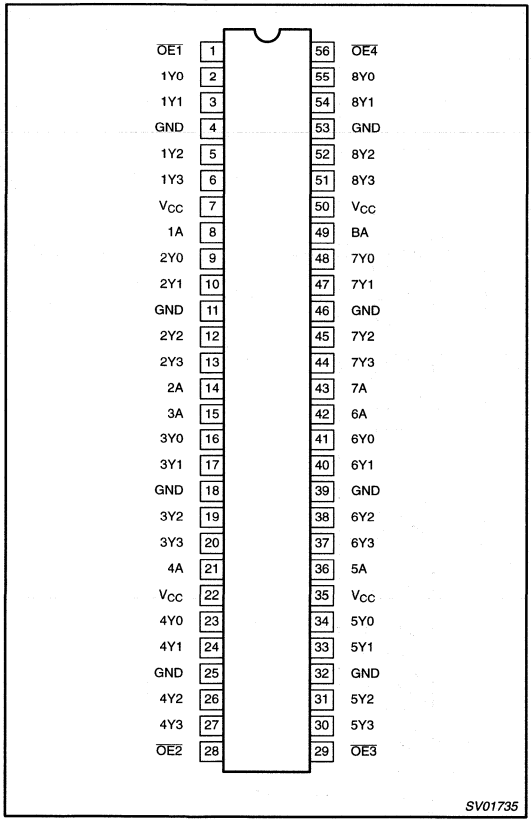
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 14, 15, 21, 36, 42, 43, 49	nA	Data inputs
2, 3, 5, 6, 9, 10, 12, 13, 16, 17, 19, 20, 23, 24, 26, 27, 30,31, 33, 34, 37, 38, 40, 44, 45, 47, 48, 51, 52, 54, 55,	nY_X	Data outputs
1, 28, 29, 56	$\overline{OE}$	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

2.5V/3.3V 1-to-4 address driver with 30Ω termination resistors (3-State)

74ALVT162344

PIN CONFIGURATION

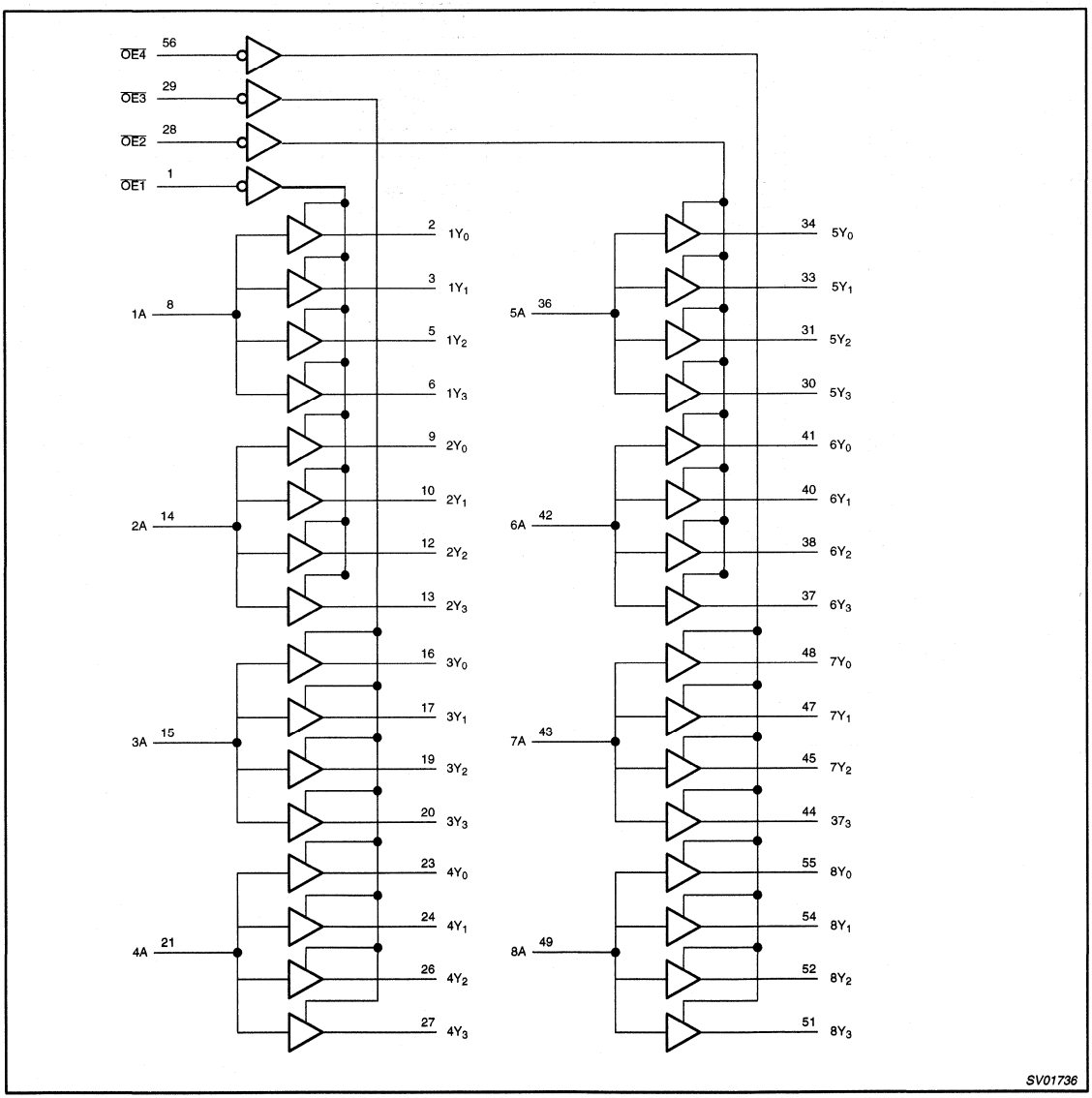


FUNCTION TABLE

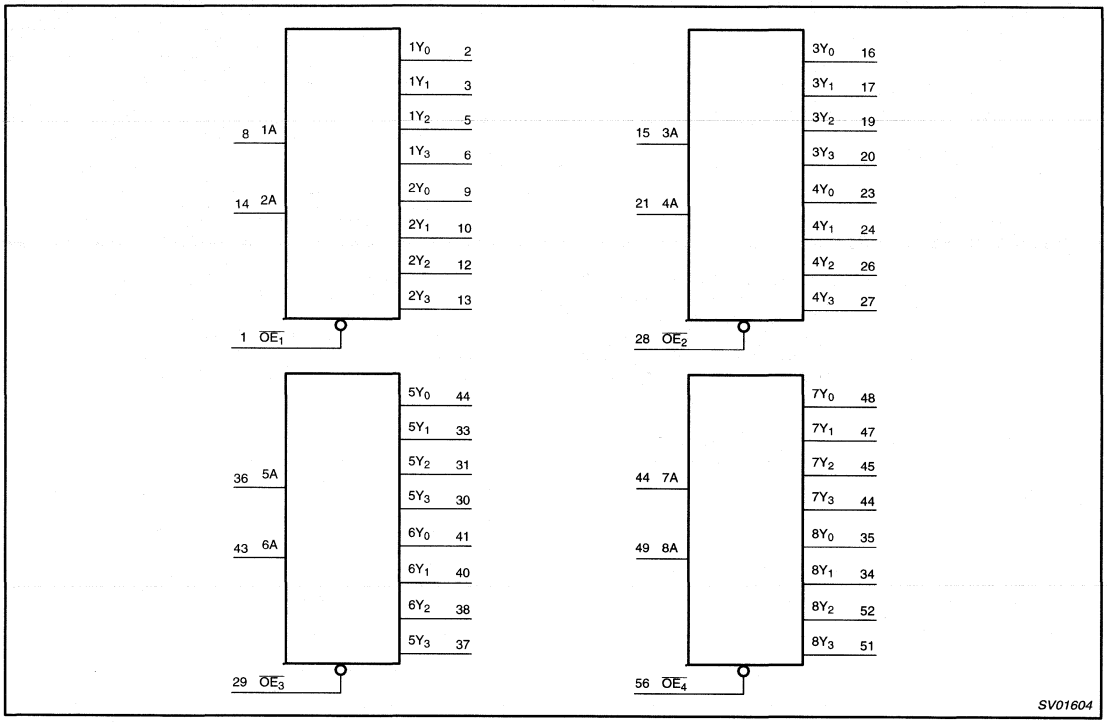
INPUTS		OUTPUTS	OPERATING MODE
$\overline{OE}$	nA	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = High voltage level
L = Low voltage level

LOGIC DIAGRAM



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A inputs	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.2	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = -40 to +85°C V_{CC} = +3.3V ±0.3V MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	1.8 1.8	2.8 2.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 0.5	2.2 1.6	3.8 2.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.0 1.0	3.2 2.5	4.8 3.8	ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 2.7V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.7	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 2.5V; V_I = 0.7V			90		µA
		V_{CC} = 5.5V; V_I = 1.7V			10		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.6	5.0	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

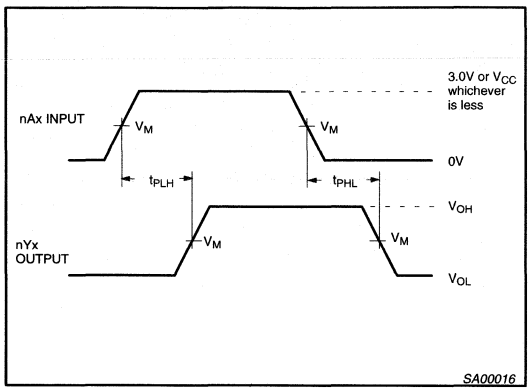
AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

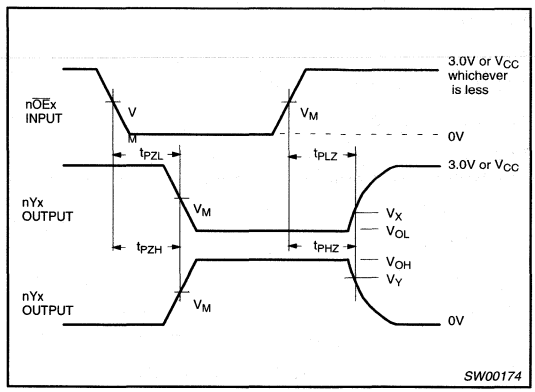
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	2.2 2.3	3.3 3.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.1 2.1	5.5 4.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.0 1.0	3.1 2.3	5.1 3.9	ns

AC WAVEFORMS

V_M = 1.5V for $V_{CC} \geq$ 3.0V; $V_M = V_{CC}/2$ for $V_{CC} \leq$ 2.7V
$V_X = V_{OL}$ + 0.3V for $V_{CC} \geq$ 3.0V; $V_X = V_{OL}$ + 0.15V for $V_{CC} \leq$ 2.7V
$V_Y = V_{OH}$ – 0.3V for $V_{CC} \geq$ 3.0V; $V_Y = V_{OH}$ – 0.15V for $V_{CC} \leq$ 2.7V

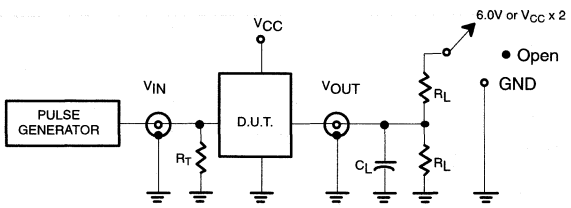


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

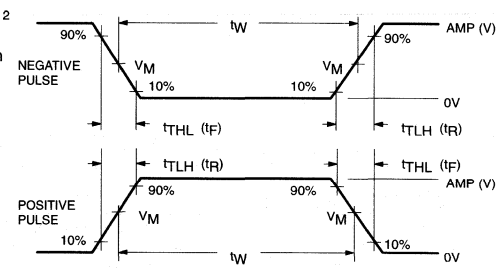


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC *CHARACTERISTICS for value.*

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00205

2.5V/3.3V 16-bit transparent D-type latch (3-State) 74ALVT16373

FEATURES

- 16-bit transparent latch
- 5V I/O compatibile
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16373 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When latch enable (LE) input is High, the Q outputs follow the data (D) inputs. When latch enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

QUICK REFERENCE DATA

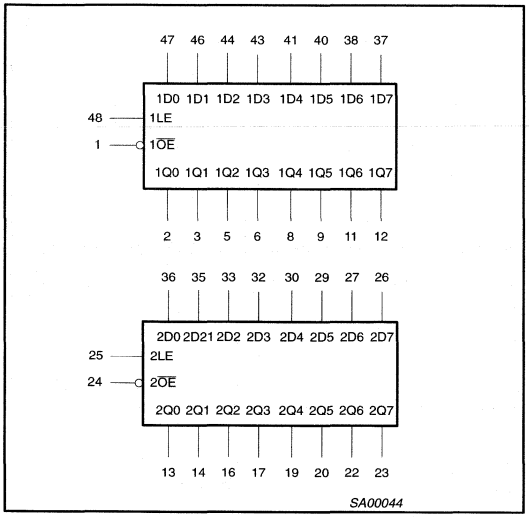
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF	2.0 2.4	1.6 1.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

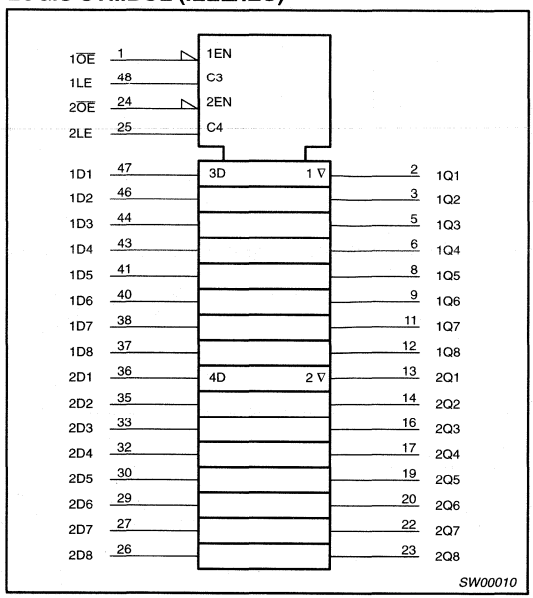
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16373 DL	AV16373 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16373 DGG	AV16373 DGG	SOT362-1

2.5V/3.3V 16-bit transparent D-type latch (3-State) 74ALVT16373

LOGIC SYMBOL



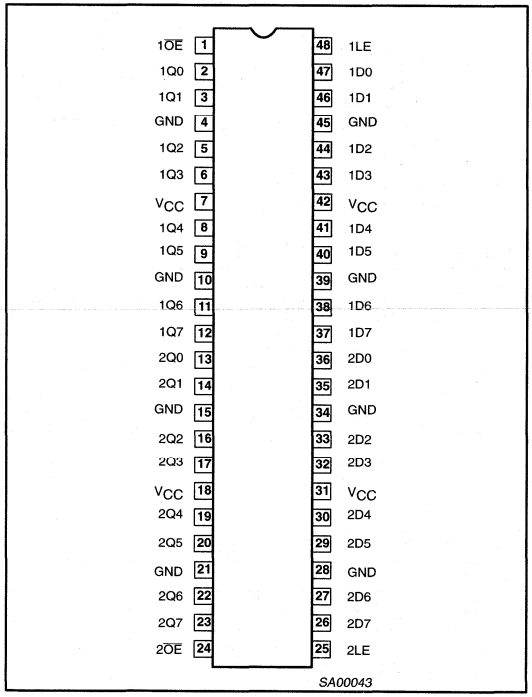
LOGIC SYMBOL (IEEE/IEC)



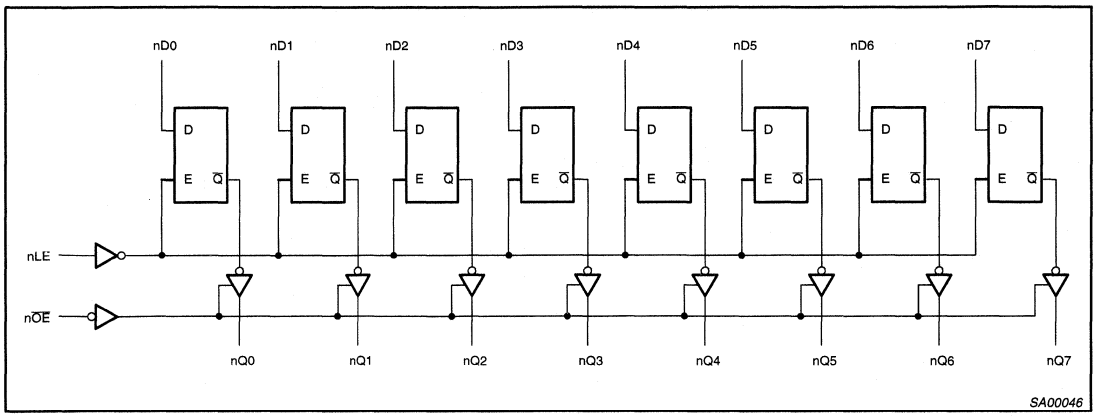
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1LE, 2LE	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nE	nDx	REGISTER	nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq 1.2V$; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}/OE$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.05	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	0.5 0.5	1.6 1.8	2.5 2.9	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.0 1.0	2.0 2.3	3.1 3.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.5 1.0	2.3 1.9	4.0 3.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5	1.5 1.5	2.9 2.3	4.5 3.7	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8			
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.0 1.0	2.0 2.4	3.2 4.2	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.5 1.5	2.6 2.8	4.2 4.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	2.0 1.5	3.5 2.6	5.5 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5	1.5 1.0	2.7 2.0	4.5 3.5	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

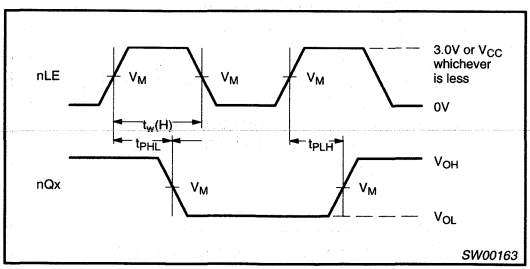
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

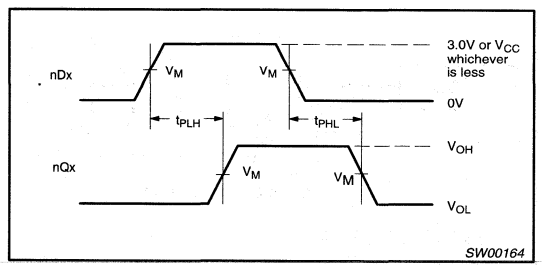
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		
			MIN	TYP	MIN	TYP	
t_S(H) t_S(L)	Setup time nDx to nE	3	0 1.5	–0.7 0.2	0.5 0.8	–0.2 0.2	ns
t_h(H) t_h(L)	Hold time nDx to nE	3	0.5 1.5	–0.2 0.7	0.8 1.0	0 0.2	ns
t_W(H)	nE pulse width High	1	1.5 1.5		1.5 1.5		ns

AC WAVEFORMS

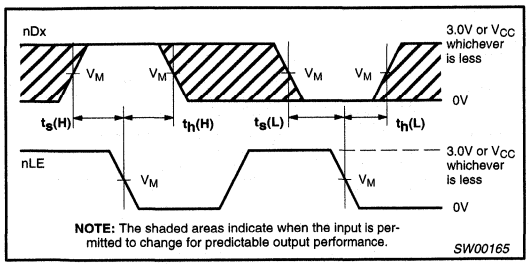
For all waveforms
V_M = 1.5V for $V_{CC} \geq$ 3.0V; $V_M = V_{CC}/2$ for $V_{CC} \leq$ 2.7V
V_M = 1.5V for $V_{CC} \geq$ 3.0V; $V_M = V_{CC}/2$ for $V_{CC} \leq$ 2.7V
$V_X = V_{OL}$ + 0.3V for $V_{CC} \geq$ 3.0V; $V_X = V_{OL}$ + 0.15V for $V_{CC} \leq$ 2.7V
$V_Y = V_{OH}$ – 0.3V for $V_{CC} \geq$ 3.0V; $V_Y = V_{OH}$ – 0.15V for $V_{CC} \leq$ 2.7V



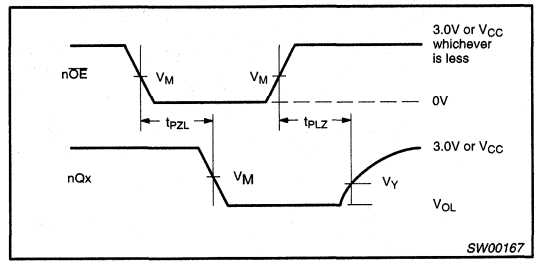
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



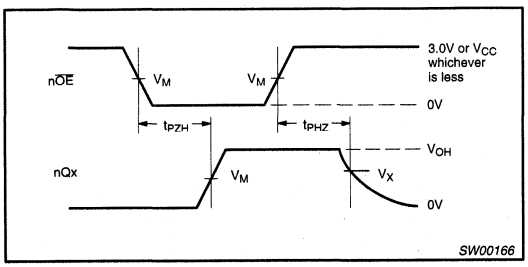
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

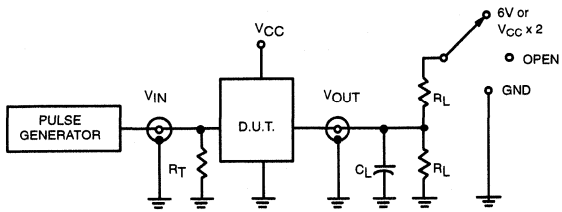


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

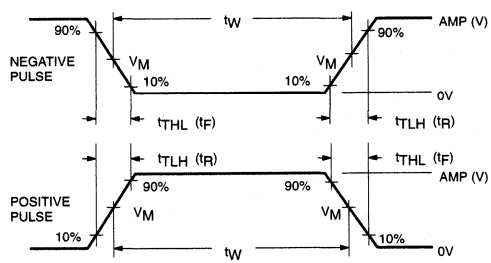


Waveform 4. 3-State Output Enable time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74ALVT16374

FEATURES

- 16-bit edge-triggered flip-flop
- 5V I/O compatibile
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16374 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit edge-triggered D-type flip-flop featuring non-inverting 3-State outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

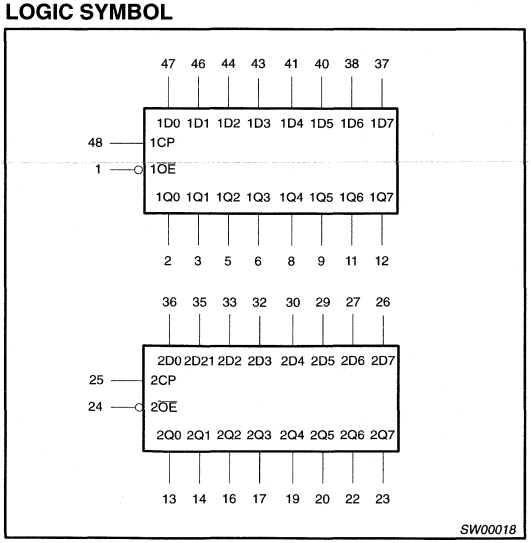
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF	2.6 2.8	2.1 2.3	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	40	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16374 DL	AV16374 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16374 DGG	AV16374 DGG	SOT362-1

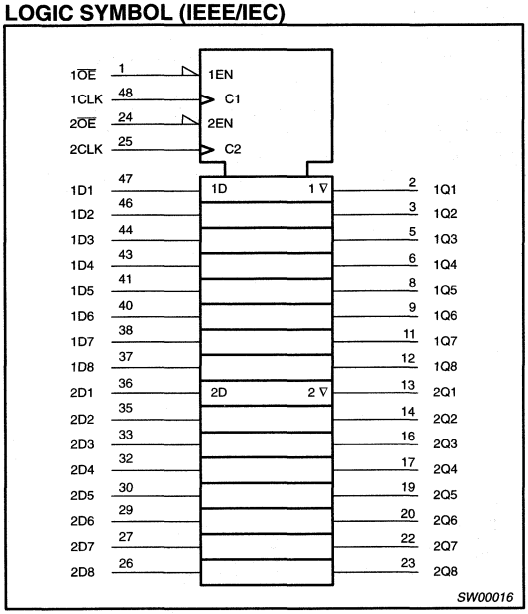
LOGIC SYMBOL



2.5V/3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74ALVT16374

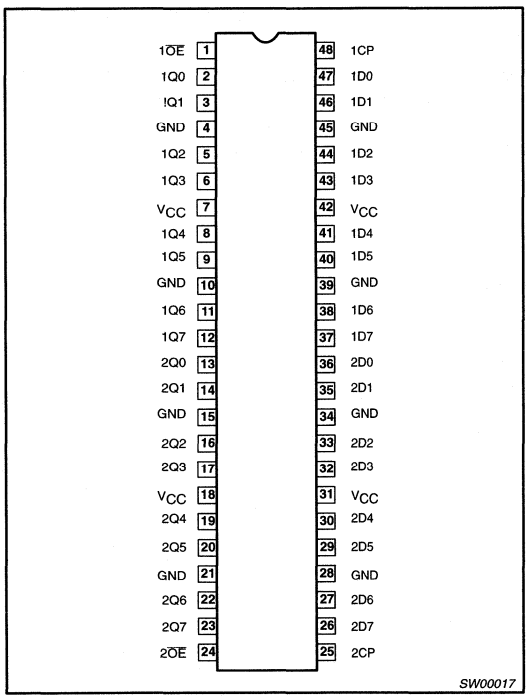
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	1D0 - 1D7 2D0 - 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12 13, 14, 16, 17, 19, 20, 22, 23	1Q0 - 1Q7 2Q0 - 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

PIN CONFIGURATION



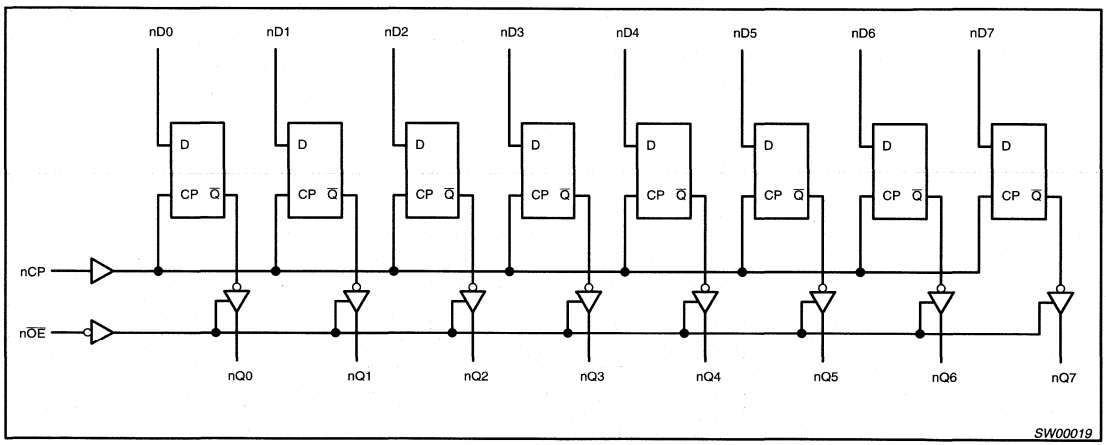
2.5V/3.3V 16-bit edge-triggered D-type flip-flop (3-State) 74ALVT16374

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx	REGISTER	nQ0 - nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↑	X	NC	NC	Hold
H H	↑ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↑ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.7	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
f_{max}	Maximum clock frequency	1	250			MHz
t_{PLH} t_{PHL}	Propagation delay nCp to nQx	1	1.0 1.0	2.1 2.3	3.2 3.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.0 1.0	2.3 2.0	3.8 3.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	3 4	1.0 1.0	2.7 2.3	4.2 3.4	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.7	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 2.5V ±0.2V			UNIT
			MIN	TYP[1]	MAX	
f_{max}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay nCp to nQx	1	1.5 1.5	2.6 2.8	4.2 4.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.0 1.0	3.4 2.6	5.6 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	3 4	2.0 1.0	2.7 2.0	4.4 3.3	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

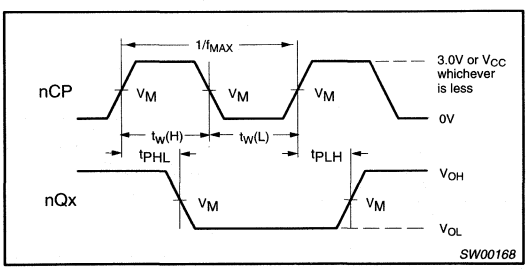
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

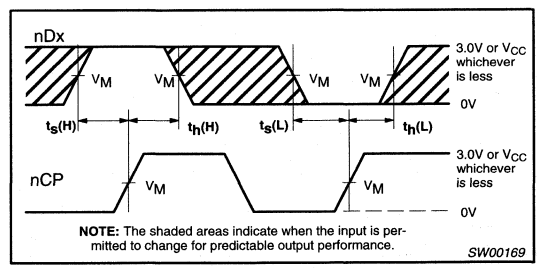
SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 2.5V ±0.2V		LIMITS V_{CC} = 3.3V ±0.3V		UNIT
			MIN	TYP	MIN	TYP	
t_S(H) t_S(L)	Setup time nDx to nCP	3	1.0 1.5	0 0.4	1.0 1.5	0 0	ns
t_h(H) t_h(L)	Hold time nDx to nCP	3	0.5 0.5	0 0	0.5 0.5	0 0	ns
t_W(H) t_w(L)	nCP pulse width High or Low	1	1.5 1.5		1.5 1.5		ns

AC WAVEFORMS

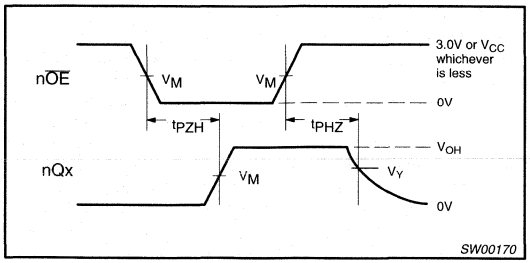
V_M = 1.5V for $V_{CC} \geq$ 3.0V; $V_M = V_{CC}/2$ for $V_{CC} \leq$ 2.7V
$V_X = V_{OL}$ + 0.3V for $V_{CC} \geq$ 3.0V; $V_X = V_{OL}$ + 0.15V for $V_{CC} \leq$ 2.7V
$V_Y = V_{OH}$ – 0.3V for $V_{CC} \geq$ 3.0V; $V_Y = V_{OH}$ – 0.15V for $V_{CC} \leq$ 2.7V



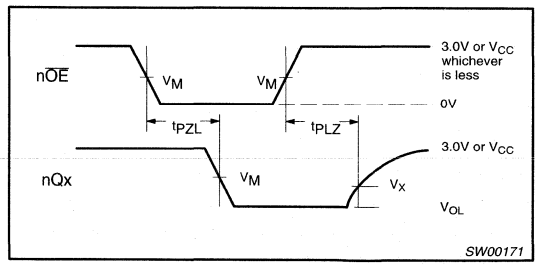
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

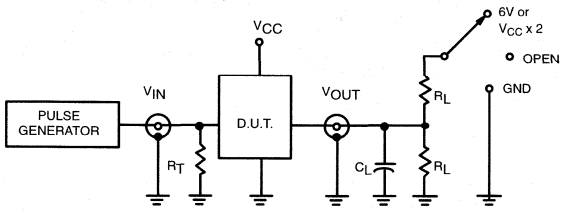


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

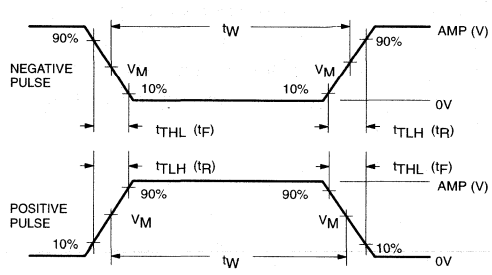


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 18-bit universal bus transceiver (3-State) 74ALVT16500

FEATURES

- 18-bit bidirectional bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Negative edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16500 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V and 3.3V with I/O compatibility up to 5V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock ($\overline{CPAB}$ and $\overline{CPBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if $\overline{CPAB}$ is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of $\overline{CPAB}$. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and $\overline{CPBA}$. The output enables are complimentary (OEAB is active High, and $\overline{OEBA}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF	1.9 2.4	1.5 1.8	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or V_{CC}	8	8	pF
I_{CCZ}	Total supply current	Outputs disabled	40	60	µA

ORDERING INFORMATION

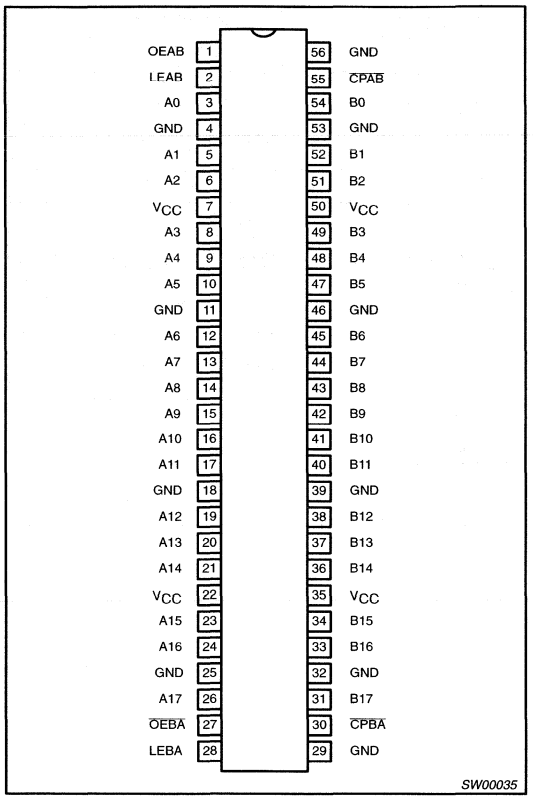
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16500 DL	AV16500 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16500 DGG	AV16500 DGG	SOT364-1

PIN DESCRIPTION

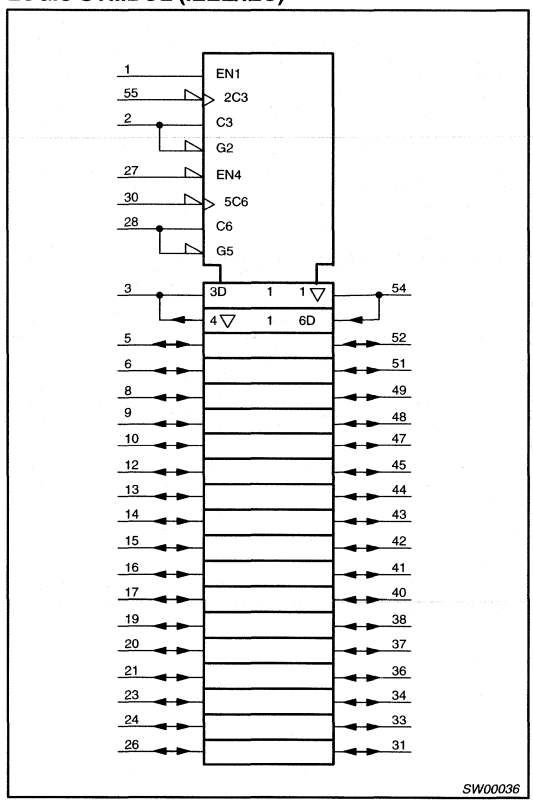
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	$\overline{CPAB}$/$\overline{CPBA}$	A-to-B/B-to-A Clock input (active falling edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

2.5V/3.3V 18-bit universal bus transceiver (3-State) 74ALVT16500

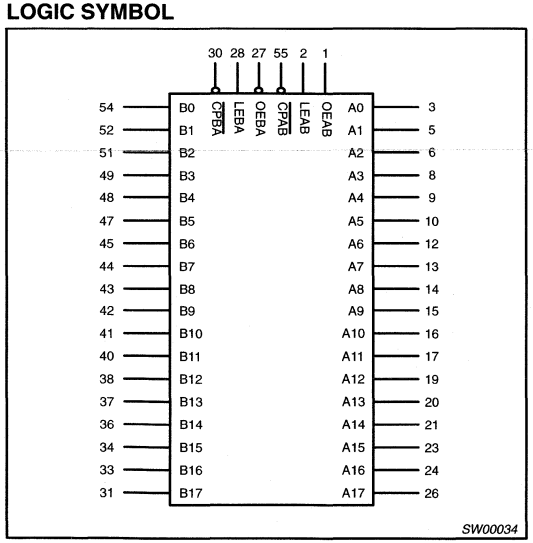
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



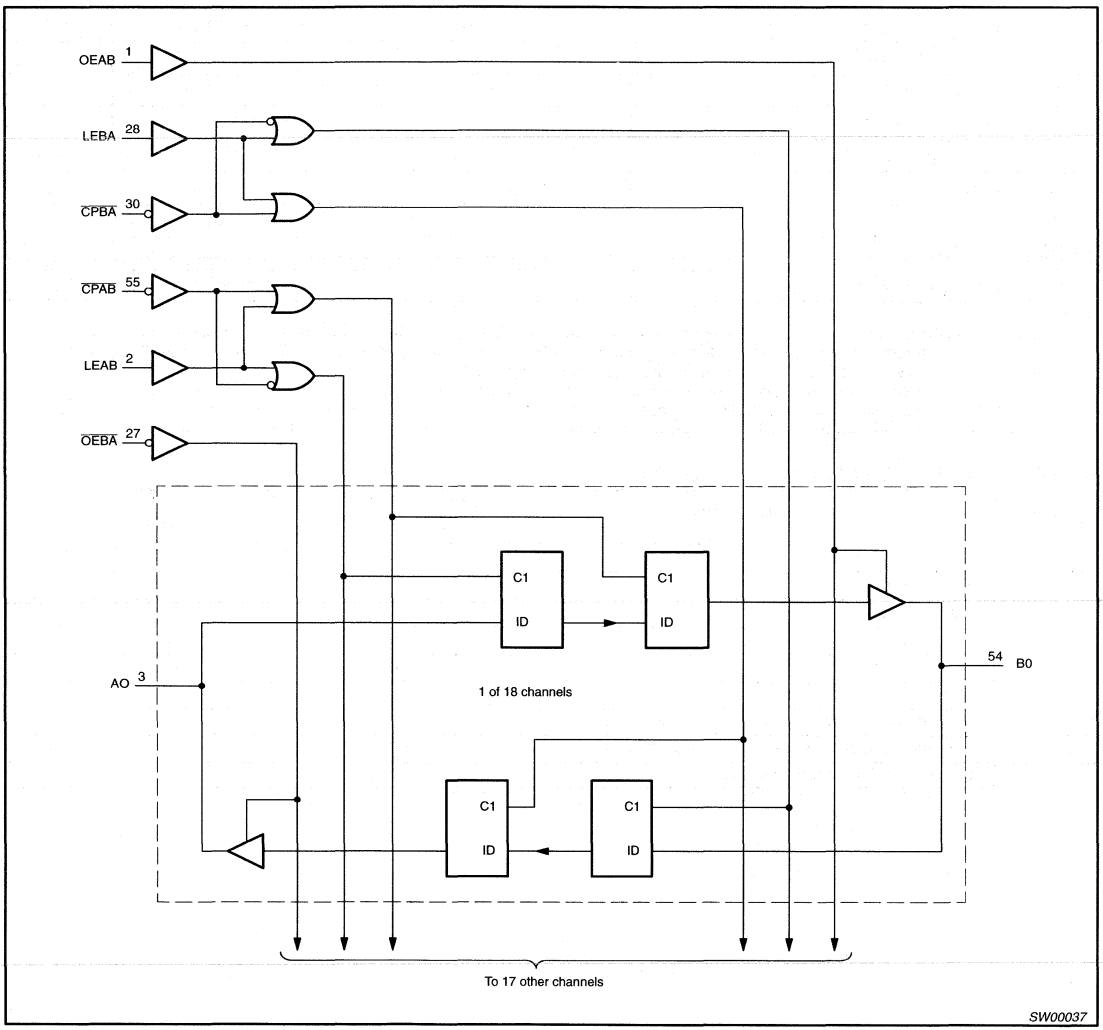
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	$\overline{CPAB}$	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↓	h	H	Z	Disabled, Clock data
L	L	↓	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↓	h	H	H	Clock data & display
H	L	↓	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CPBA}$.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			1	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.06	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.5 1.8	2.3 2.7	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	1.5 1.5	2.3 3.3	3.6 4.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An	1	1.5 1.5	2.5 3.1	4.0 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.5 1.5	2.3 1.4	3.3 2.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	2.8 2.3	4.3 3.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	1.9 2.0	1.0 1.0	ns
th(H) th(L)	Hold time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	0 0	–0.9 –0.9	ns
ts(H) ts(L)	Setup time, High or Low An to LEAB or Bn to LEBA	4	0.0 0.3	–1.0 –0.3	ns
th(H) th(L)	Hold time, High or Low An to LEAB or Bn to LEBA	4	1.2 1.2	0.4 0.4	ns
tw(H) tw(L)	Pulse width, High or Low $\overline{CPAB}$ or $\overline{CPBA}$	1	1.0 1.0		ns
tw(H)	LEAB or LEBA pulse width, High	3	1.0		ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8			
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.9 2.4	3.1 3.5	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	1.5 2.0	2.9 4.3	4.6 6.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An	1	2.0 2.0	3.4 4.2	5.3 6.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.5 1.0	2.6 1.6	4.1 2.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.0	2.7 2.1	4.1 3.2	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

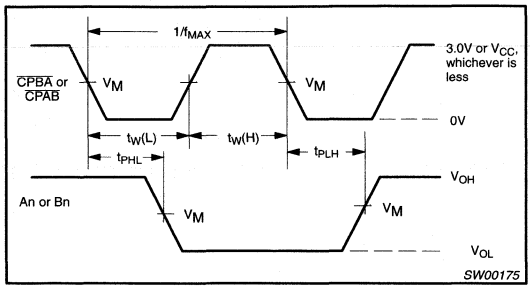
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	2.3 3.4	0.8 1.4	ns
th(H) th(L)	Hold time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	0 0	–1.2 –0.9	ns
ts(H) ts(L)	Setup time, High or Low An to LEAB or Bn to LEBA	4	0 1.0	–0.7 0	ns
th(H) th(L)	Hold time, High or Low An to LEAB or Bn to LEBA	4	1.0 1.4	0.1 0.7	ns
tw(H) tw(L)	Pulse width, High or Low $\overline{CPAB}$ or $\overline{CPBA}$	1	1.5 1.5		ns
tw(H)	LEAB or LEBA pulse width, High	3	1.5		ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

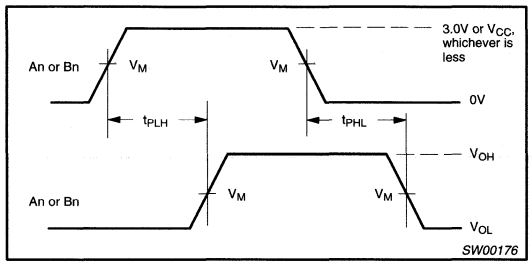
AC WAVEFORMS

NOTES:

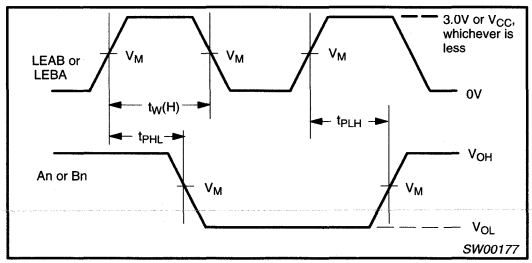
1. $V_M = 1.5V$ at $V_{CC} \geq 3.0V$, $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7V$
2. $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 3.0V$, $V_X = V_{OL} + 0.15V$ at $V_{CC} \leq 2.7V$
3. $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 3.0V$, $V_Y = V_{OH} - 0.15V$ at $V_{CC} \leq 2.7V$



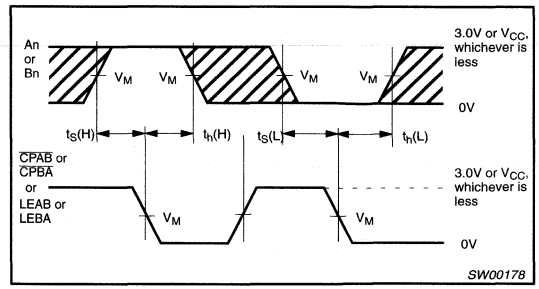
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



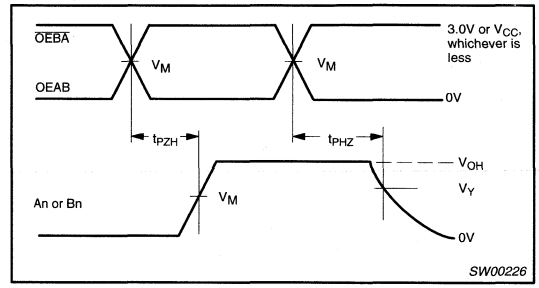
Waveform 2. Propagation Delay, Transparent Mode



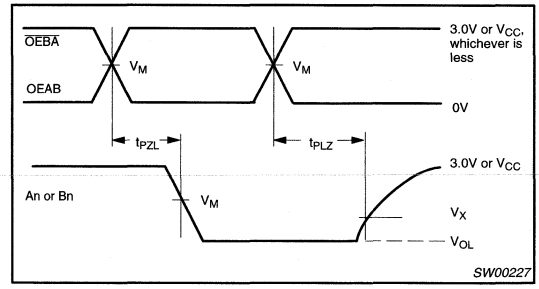
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 4. Data Setup and Hold Times

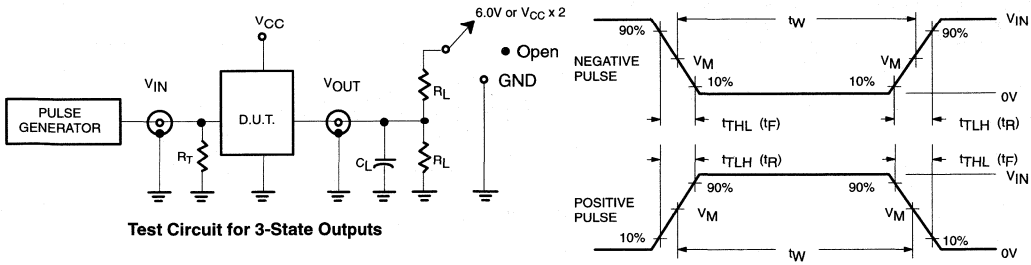


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00025

2.5V/3.3V 18-bit universal bus transceiver (3-State) 74ALVT16501

FEATURES

- 18-bit bidirectional bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL and LVTTL input and output switching levels
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Positive edge triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 400V per Machine Model

DESCRIPTION

The 74ALVT16501 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V and 3.3V with I/O compatibility up to 5V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and CPBA. The output enables are complimentary (OEAB is active High, and $\overline{OEBA}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF	1.9 2.5	1.4 1.8	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or V_{CC}	4	4	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or V_{CC}	8	8	pF
I_{CCZ}	Total supply current	Outputs disabled	40	60	µA

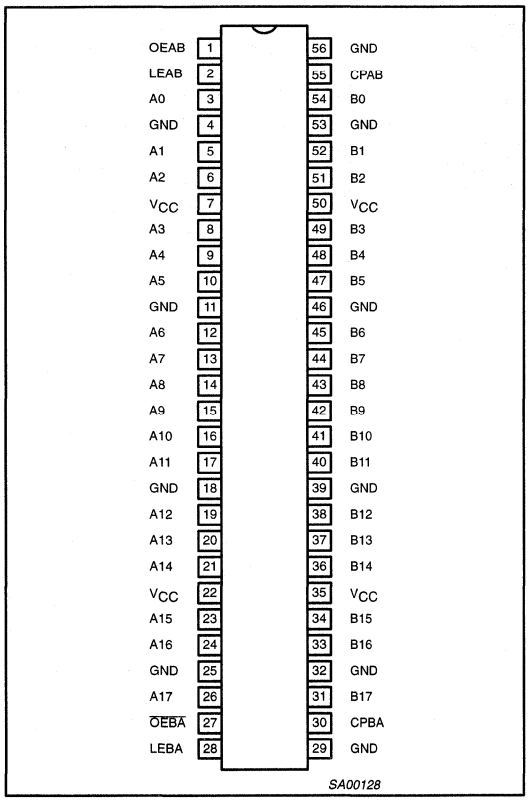
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16501 DL	AV16501 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16501 DGG	AV16501 DGG	SOT364-1

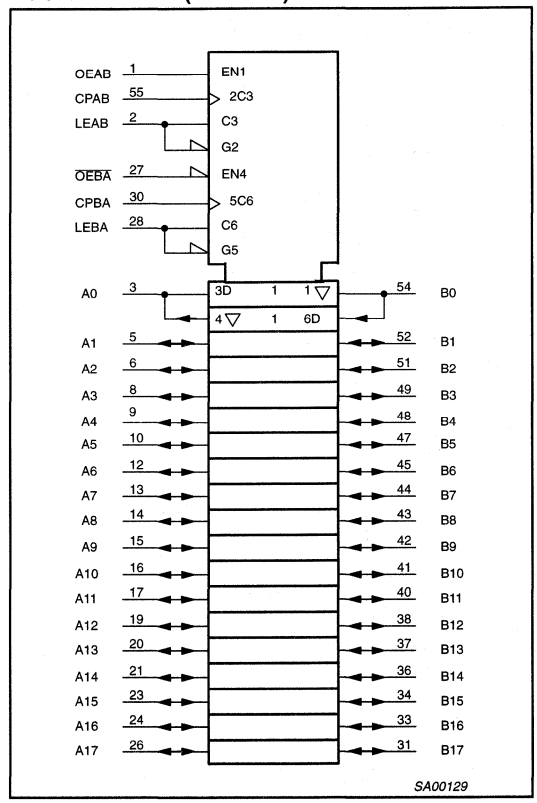
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53, 29, 56	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

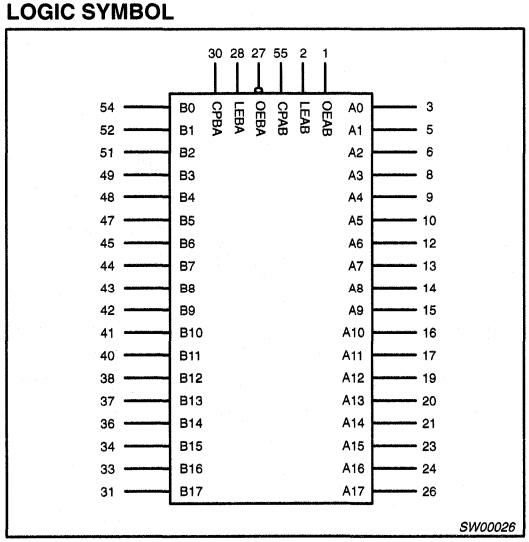
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



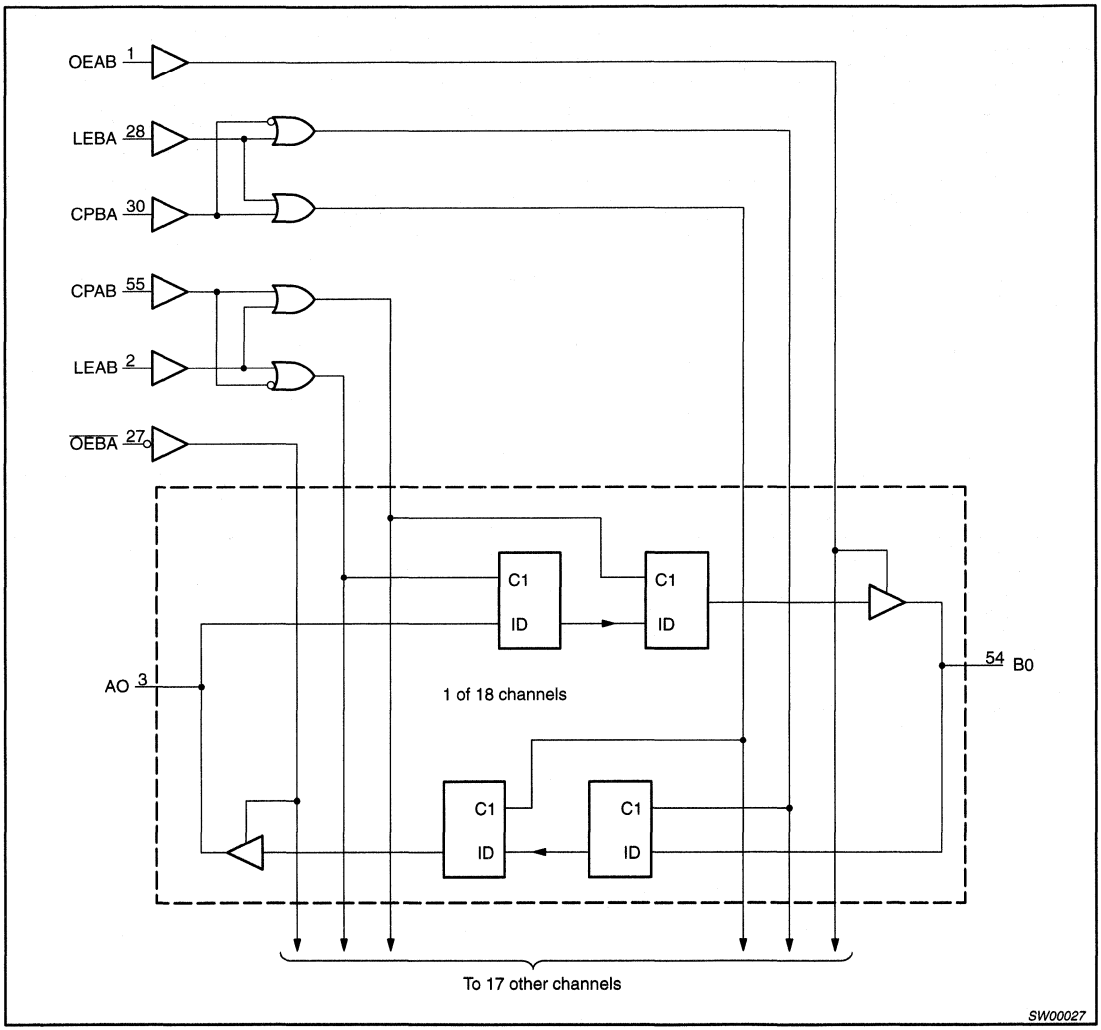
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↑	h	H	Z	Disabled, Clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↑	h	H	H	Clock data & display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CPBA.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedence "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS [1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = −18mA			−0.85	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = −100µA		V_{CC}−0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = −32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		−75	−140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1.0	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.06	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}−0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.4 1.8	3.4 3.8	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	1.5 1.5	2.1 2.7	3.4 4.0	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.0 1.0	1.9 2.7	3.2 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.0 1.0	2.0 1.4	3.1 3.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	2.0 2.0	2.7 2.5	4.2 4.0	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP	
$t_S(H)$ $t_S(L)$	Setup time, High or Low An to CPAB or Bn to CPBA	4	2.0 2.0	0.5 0.7	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low An to CPAB or Bn to CPBA	4	1.0 1.0	–0.6 –0.3	ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low An to LEAB or Bn to LEBA	4	1.0 1.0	–0.6 –0.1	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low An to LEAB or Bn to LEBA	4	1.0 1.5	0.1 0.6	ns
$t_W(H)$ $t_W(L)$	Pulse width, High or Low CPAB or CPBA	1	2.0 2.0		ns
$t_W(H)$	LEAB or LEBA pulse width, High	3	1.5		ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8			
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–75		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			5	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			4	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.5	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O =0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.9 2.5	3.0 3.8	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	2.0 2.0	3.0 3.5	4.5 5.4	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.0 1.0	2.9 3.7	4.9 5.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.5 1.5	3.1 2.1	4.5 2.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	3.0 2.4	4.2 3.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

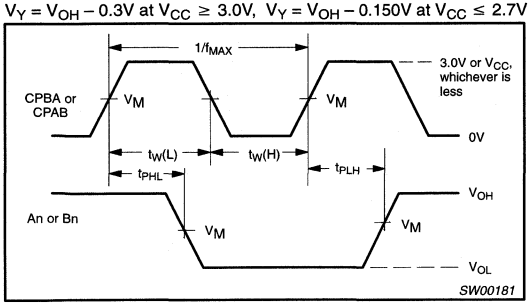
AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

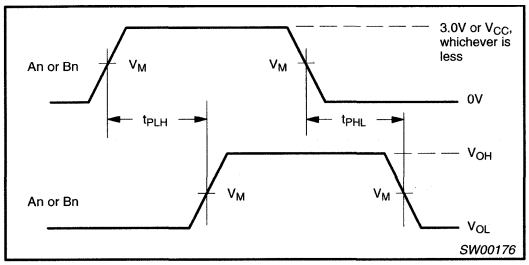
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP	
$t_S(H)$ $t_S(L)$	Setup time, High or Low An to CPAB or Bn to CPBA	4	1.9 2.5	0.4 1.2	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low An to CPAB or Bn to CPBA	4	0 1.0	–1.2 –0.4	ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low An to LEAB or Bn to LEBA	4	0 1.0	–1.0 –0.5	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low An to LEAB or Bn to LEBA	4	1.0 2.0	–0.5 1.0	ns
$t_W(H)$ $t_W(L)$	Pulse width, High or Low CPAB or CPBA	1	3.0 3.0		ns
$t_W(H)$	LEAB or LEBA pulse width, High	3	1.5		ns

AC WAVEFORMS

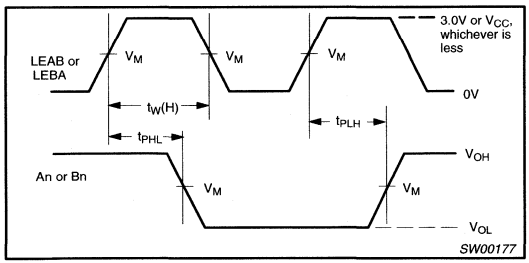
V_M = 1.5V at V_{CC} ≥ 3.0V, $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V, $V_X = V_{OL}$ + 0.150V at V_{CC} ≤ 2.7V
$V_Y = V_{OH}$ – 0.3V at V_{CC} ≥ 3.0V, $V_Y = V_{OH}$ – 0.150V at V_{CC} ≤ 2.7V



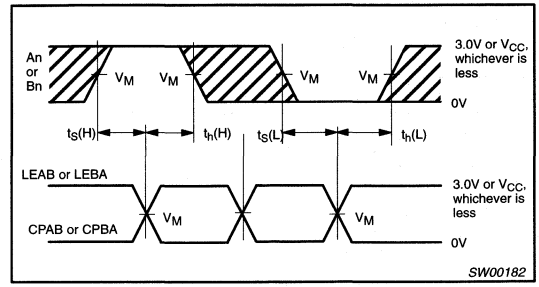
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



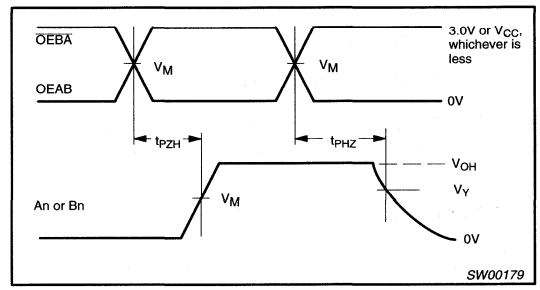
Waveform 2. Propagation Delay, Transparent Mode



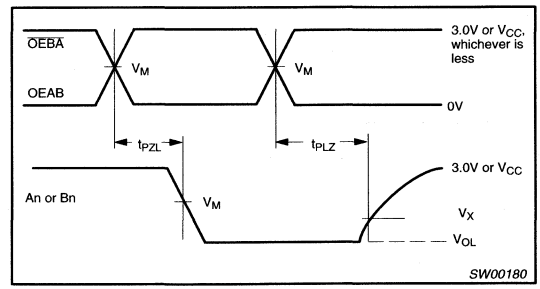
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 4. Data Setup and Hold Times

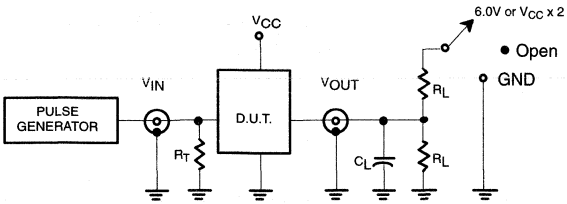


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

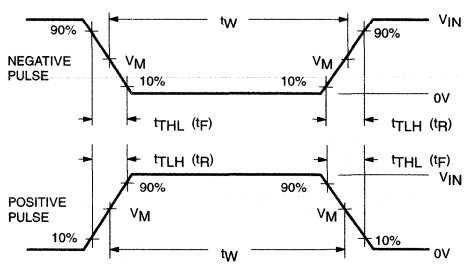


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00220

2.5V/3.3V 16-bit buffer/driver (3-State) 74ALVT16541

FEATURES

- 16-bit universal bus interface
- 5V I/O compatibile
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16541 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device can be used as two octal buffers or one 16-bit buffer. The device is ideal for driving bus lines.

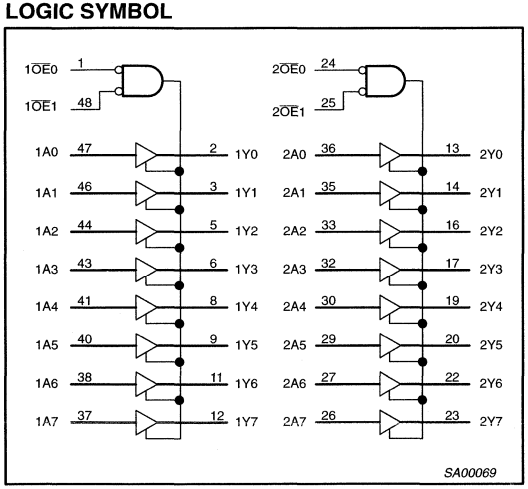
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF	1.8 1.7	1.4 1.4	ns
C_{IN}	Input capacitance n$\overline{OE}$x	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output pin capacitance	Outputs disabled; V_O = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16541 DL	AV16541 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16541 DGG	AV16541 DGG	SOT362-1

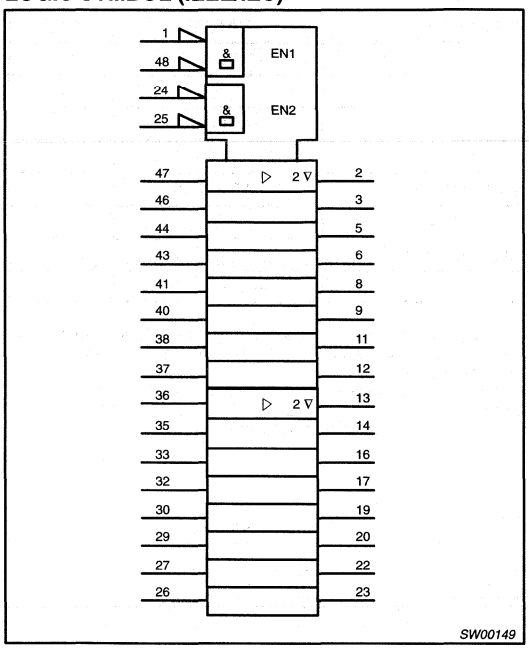
LOGIC SYMBOL



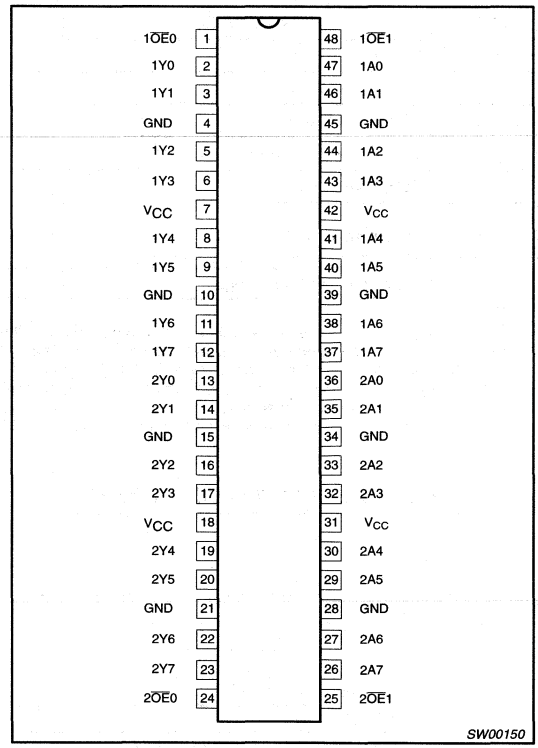
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0–1A7 2A0–2A7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12,13, 14, 16, 17, 19, 20, 22, 23	1Y0–1Y7 2Y0–2Y7	Data outputs
1, 48 24, 25	1$\overline{OE}$0, 1$\overline{OE}$1, 2$\overline{OE}$0, 2$\overline{OE}$1	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



FUNCTION TABLE

INPUTS			OUTPUTS
$n\overline{OE}0$	$n\overline{OE}1$	nAx	nYx
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.2	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	1.4 1.4	2.3 2.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.0 2.3	4.8 3.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.3 2.8	4.7 3.9	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 8mA			0.3	0.4	
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

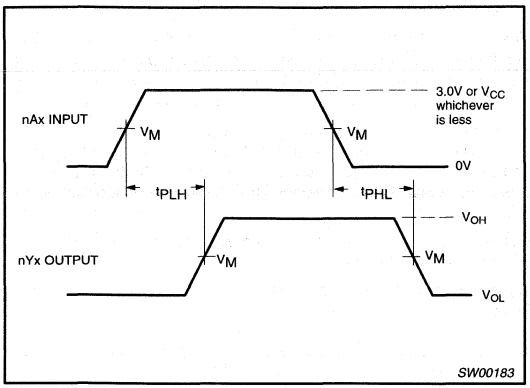
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	0.5 0.5	1.8 1.7	2.9 2.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	4.4 3.3	6.5 5.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.0	3.2 2.5	4.9 3.9	ns

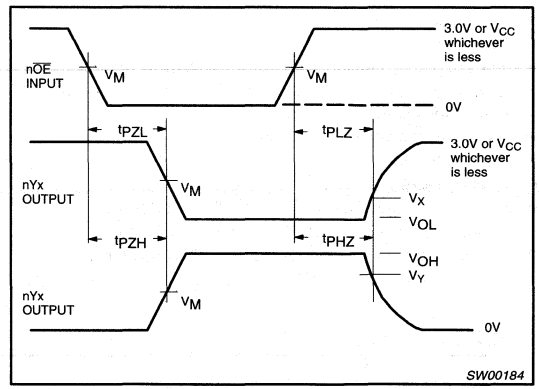
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 3.0V; $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V; $V_X = V_{OL}$ + 0.15V at V_{CC} ≤ 2.7V
$V_Y = V_{OH}$ − 0.3V at V_{CC} ≥ 3.0V; $V_Y = V_{OH}$ − 0.15V at V_{CC} ≤ 2.7V

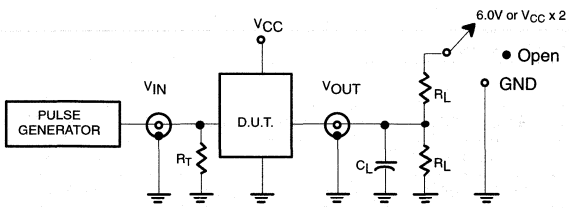


Waveform 1. Input to Output Propagation Delays

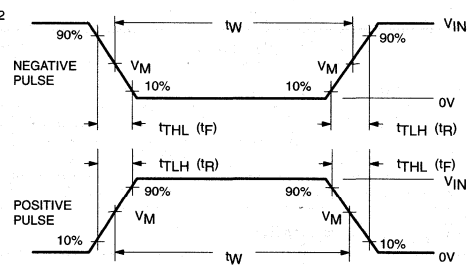


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

2.5V/3.3V 16-bit registered transceiver (3-State) 74ALVT16543

FEATURES

- 16-bit universal bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16543 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74ALVT16543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are Low, the A-to-B path is transparent.

A subsequent Low-to-High transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $n\overline{EAB}$ and $n\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

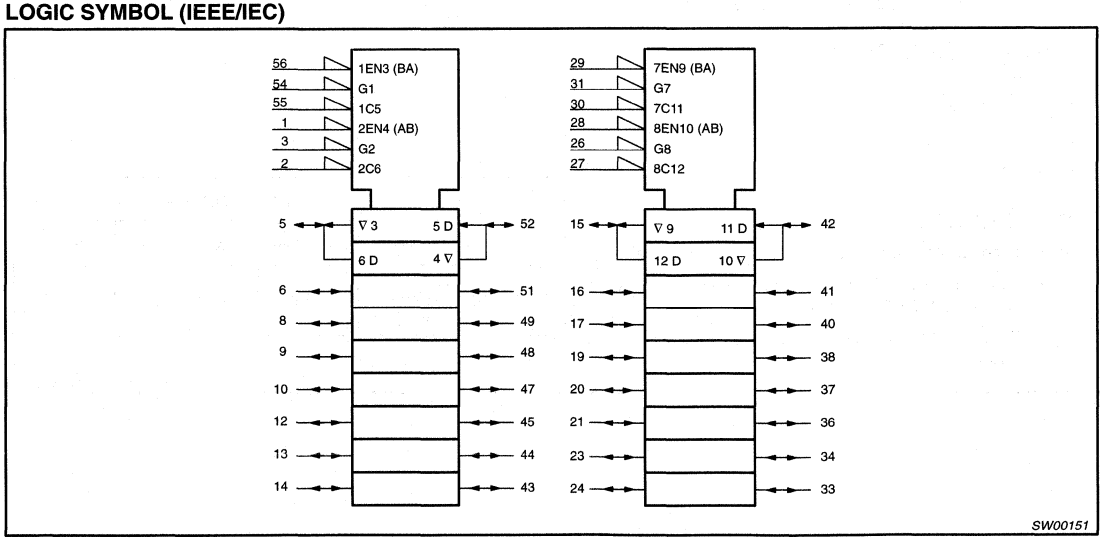
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF	1.8 2.7	1.6 1.8	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

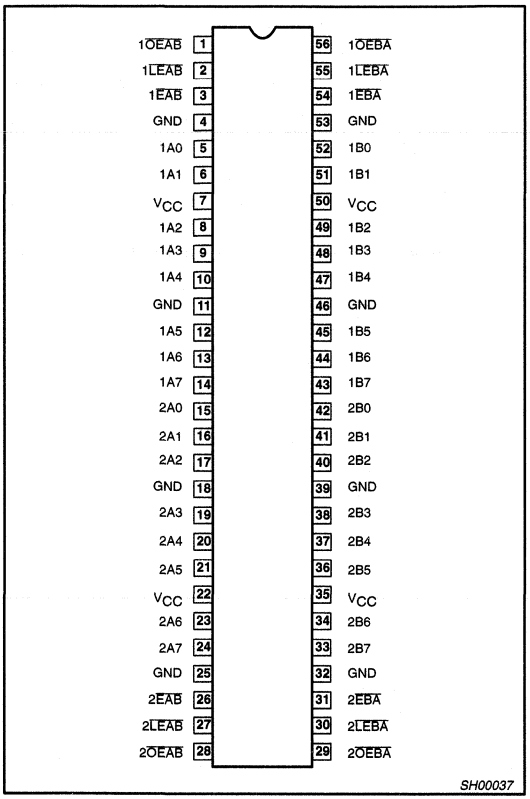
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16543 DL	AV16543 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16543 DGG	AV16543 DGG	SOT364-1

LOGIC SYMBOL (IEEE/IEC)

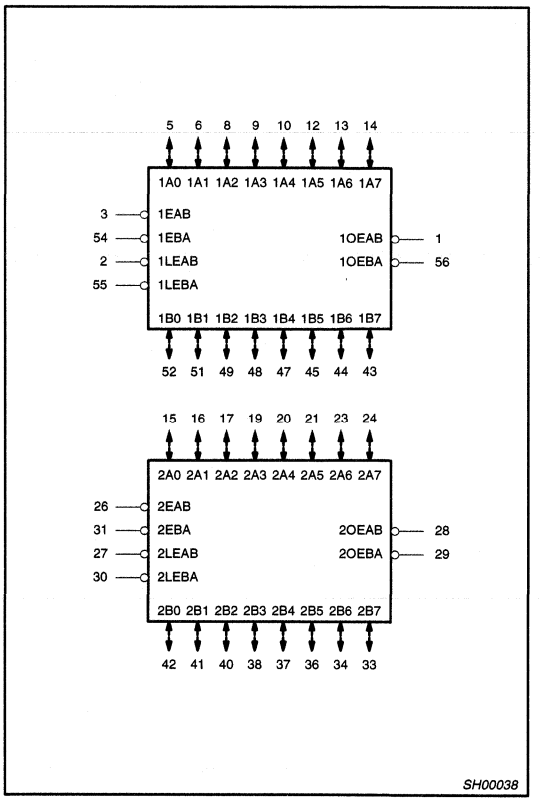


PIN CONFIGURATION



SH00037

LOGIC SYMBOL

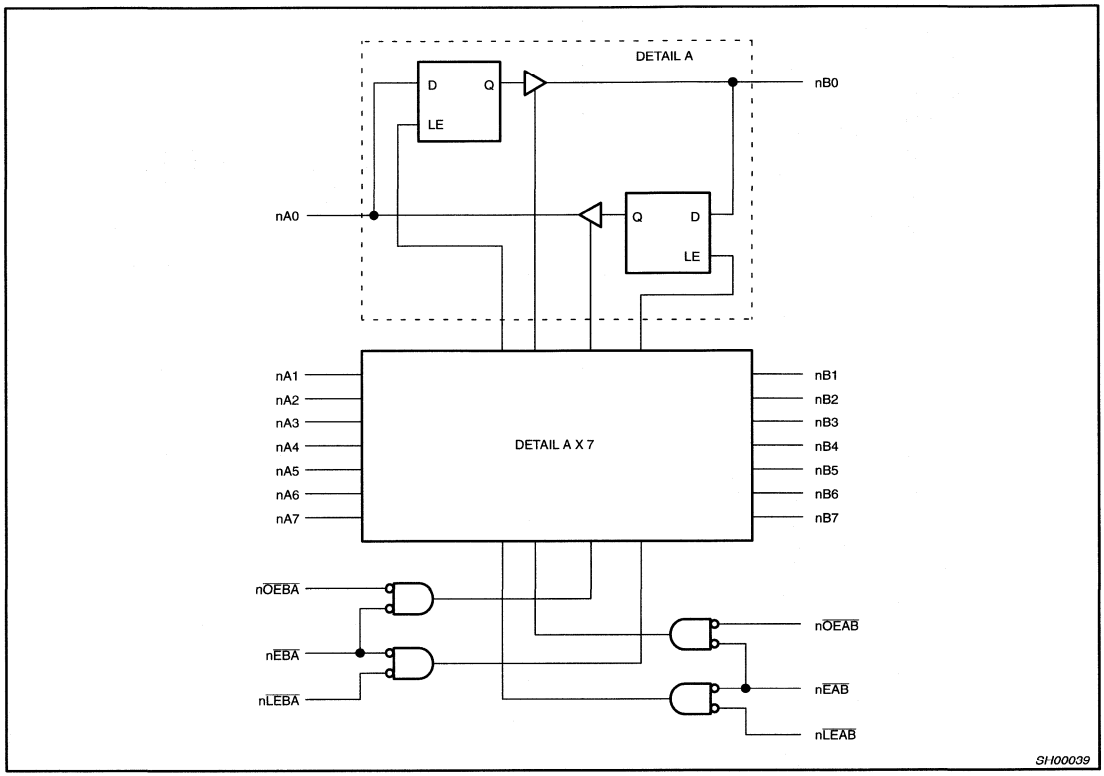


SH00038

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	A Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	B Data inputs/outputs
1, 56 28, 29	$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	$1\overline{EAB}$, $1\overline{EBA}$, $2\overline{EAB}$, $2\overline{EBA}$	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	$1\overline{LEAB}$, $1\overline{LEBA}$, $2\overline{LEAB}$, $2\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
nOEXX	nEXX	nLEXX	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of nLEXX or nEXX (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of nLEXX or nEXX (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of nLEXX or nEXX (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.6	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			120		µA
		V_{CC} = 2.3V; V_I = 1.7V			–6		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.6	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	0.5 0.5	1.6 1.8	2.5 3.0	ns
t_{PLH} t_{PHL}	Propagation delay n$\overline{LEBA}$ to nAx, n$\overline{LEAB}$ to nBx	1 2	1.0 1.0	2.4 2.4	4.0 4.0	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	1.0 1.0	2.3 1.8	4.0 3.1	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	1.0 1.0	3.1 2.7	4.7 4.0	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	1.0 1.0	2.5 1.9	4.2 3.1	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	1.0 1.0	2.9 2.4	4.5 3.8	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	0.0 0.7	–0.8 –0.3	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	1.5 1.5	0.4 0.8	ns
t_s(H) t_s(L)	Setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	0.5 1.1	–0.8 –0.2	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	1.2 2.0	0.3 1.1	ns
t_W(L)	Latch enable pulse width, Low	3	1.5		ns

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.0 1.0	1.8 2.7	5.1 4.5	ns
t_{PLH} t_{PHL}	Propagation delay n$\overline{LEBA}$ to nAx, n$\overline{LEAB}$ to nBx	1 2	1.5 1.5	3.9 3.6	6.4 5.9	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	1.5 1.5	4.0 2.7	6.5 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5	1.5 1.5	3.7 2.6	5.6 4.0	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	1.5 1.5	4.2 2.8	7.0 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5	1.5 1.5	3.6 2.4	5.6 3.9	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

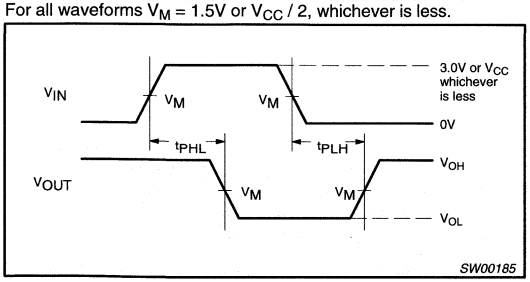
AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

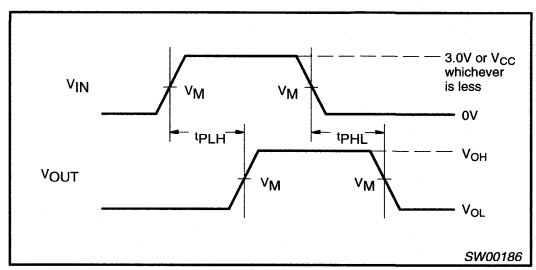
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	0 1.0	–0.9 0.2	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3	0.8 1.7	–0.2 1.0	ns
t_s(H) t_s(L)	Setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	0 1.5	–1.0 0.4	ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3	0.5 2.0	–0.2 1.3	ns
t_W(L)	Latch enable pulse width, Low	3	1.5		ns

AC WAVEFORMS

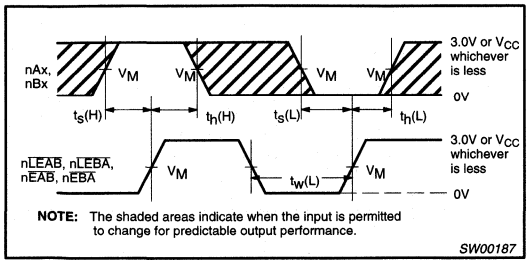
For all waveforms V_M = 1.5V or V_{CC} / 2, whichever is less.



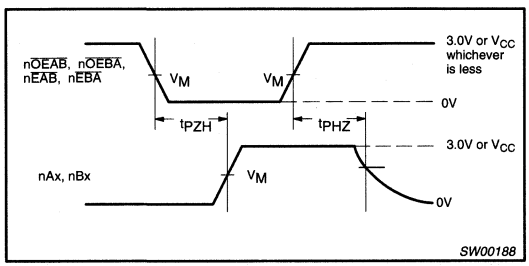
Waveform 1. Propagation Delay For Inverting Output



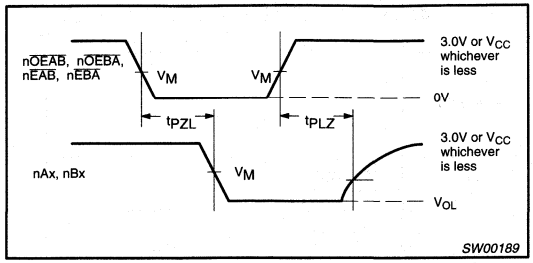
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width

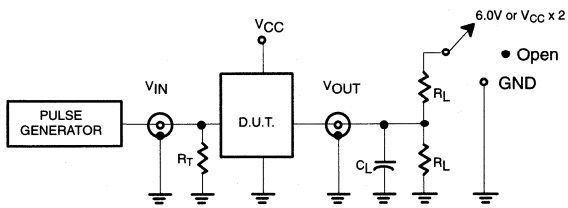


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

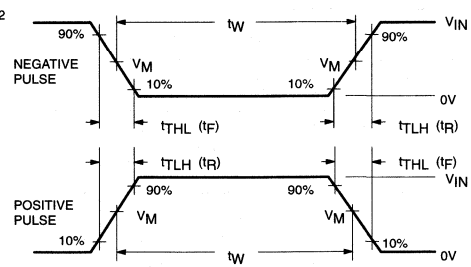


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	10MHz	500ns	2.5ns	2.5ns

SW00025

2.5V/3.3V 18-bit universal bus transceiver (3-State) 74ALVT16600

FEATURES

- 18-bit bidirectional bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Negative edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16600 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V and 3.3V with I/O compatibility up to 5V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock ($\overline{CPAB}$ and $\overline{CPBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if $\overline{CPAB}$ is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of $\overline{CPAB}$. When $\overline{OEAB}$ is Low, the outputs are active. When $\overline{OEAB}$ is High, the outputs are in the high-impedance state. The High clock can be controlled with the clock-enable inputs ($\overline{CEBA}$/$\overline{CEAB}$).

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and $\overline{CPBA}$.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF	1.9 2.5	1.6 1.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or V_{CC}	8	8	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16600 DL	AV16600 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16600 DGG	AV16600 DGG	SOT364-1

PIN DESCRIPTION

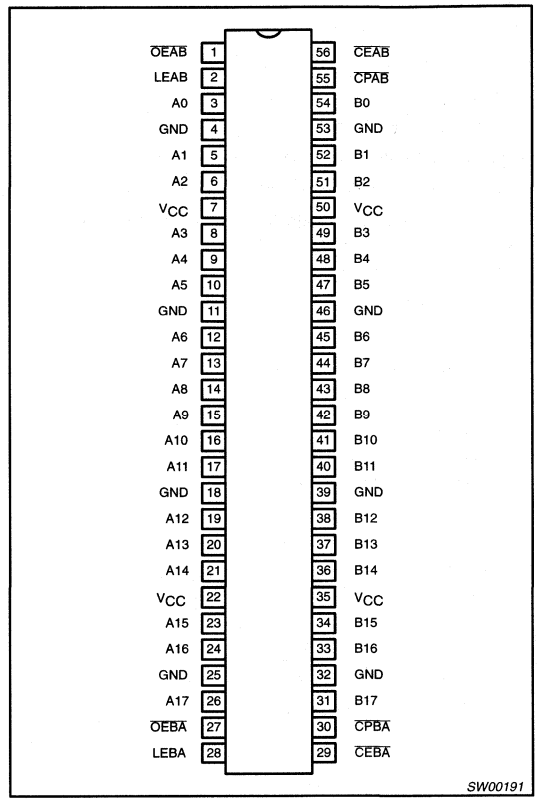
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 27	$\overline{OEAB}$/$\overline{OEBA}$	A-to-B Output enable input (active Low)
29, 56	$\overline{CEBA}$/$\overline{CEAB}$	B-to-A / A-to-B clock enable (active Low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	$\overline{CPAB}$/$\overline{CPBA}$	A-to-B/B-to-A Clock input (active falling edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

FUNCTION TABLE

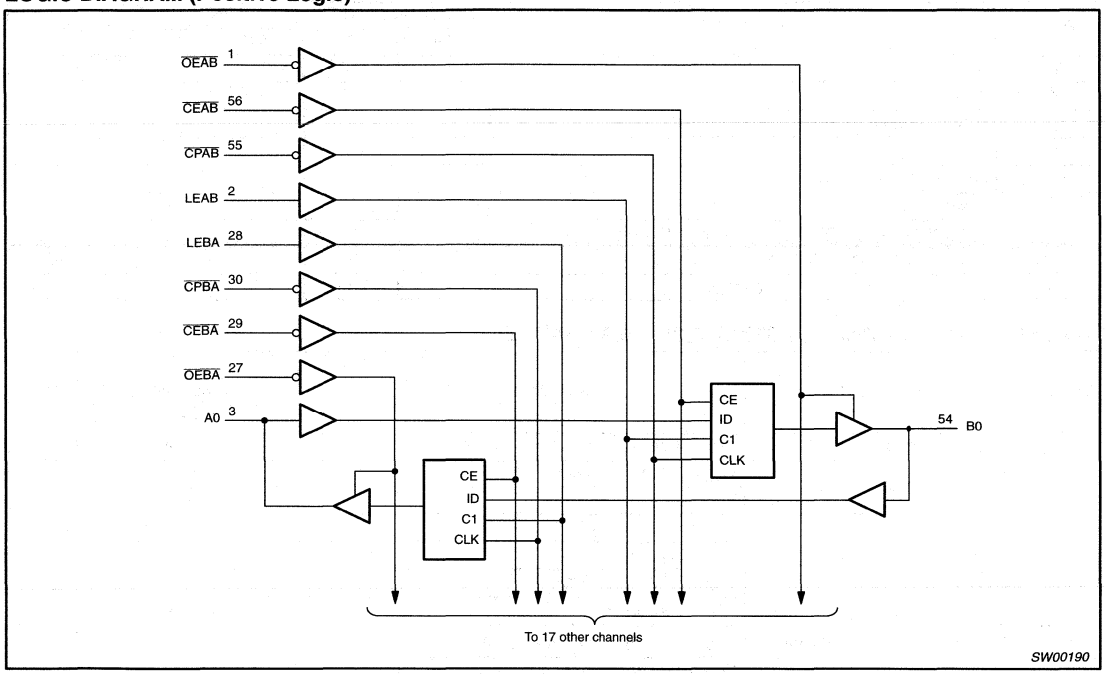
INPUTS					OUTPUT
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	$\overline{CPAB}$	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_O‡
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B_O‡
L	L	L	L	X	B_O§

X =Don't care
H =High voltage level
L =Low voltage level
↓ =High-to-Low clock transition
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CPBA}$, and $\overline{CEBA}$.
‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was Low before LEAB went Low.

PIN CONFIGURATION



LOGIC DIAGRAM (Positive Logic)



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1.0	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.06	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.0	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1		300		MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.6 1.9	2.3 2.8	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	1.5 1.5	2.2 2.5	3.3 4.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An	1	1.5 1.5	2.6 3.2	4.2 4.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.5 1.0	2.2 1.6	3.4 2.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	2.6 2.3	3.8 3.5	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	2.0 2.0	0.8 0.9	ns
th(H) th(L)	Hold time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	0.0 0.0	−0.9 −0.7	ns
ts(H) ts(L)	Setup time, High or Low Clock Low An to LEAB or Bn to $\overline{CPBA}$	4	1.0 1.0	−0.4 −0.1	ns
th(H) th(L)	Hold time, High or Low Clock High An to LEAB or Bn to LEBA	4	1.0 1.0	0.1 0.4	ns
ts(H) ts(L)	Setup time $\overline{CEAB}$ before $\overline{CPAB}$ or $\overline{CEBA}$ before $\overline{CPBA}$	4	1.5 1.0	0.3 −0.6	ns
th(H) th(L)	Hold time $\overline{CEAB}$ after $\overline{CPAB}$ or $\overline{CEBA}$ after $\overline{CPBA}$	4	1.5 1.0	0.7 −0.2	ns
tw(H) tw(L)	Pulse width, High or Low $\overline{CPAB}$ or $\overline{CPBA}$	1	1.5 1.5		ns
tw(H)	LEAB or LEBA pulse width, High	3	1.5		ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8			
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–75		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			1	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.0	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1		250		MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.5	1.9 2.5	3.0 3.6	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	2.0 2.5	3.0 3.3	4.5 5.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An	1	2.5 2.5	3.8 4.5	5.6 6.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	2.0 1.0	3.1 2.0	4.4 3.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	2.5 2.3	4.1 3.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = −40°C to +85°C.

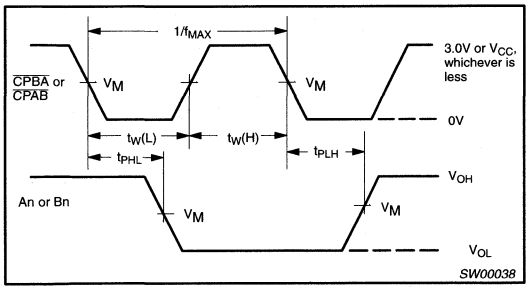
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	1.5 2.0	0.5 1.1	ns
th(H) th(L)	Hold time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4	0.0 1.0	−1.1 −0.4	ns
ts(H) ts(L)	Setup time, High or Low Clock Low An to LEAB or Bn to $\overline{CPBA}$	4	0.0 1.5	−0.8 0.4	ns
th(H) th(L)	Hold time, High or Low Clock High An to LEAB or Bn to LEBA	4	1.0 1.5	−0.4 0.9	ns
ts(H) ts(L)	Setup time $\overline{CEAB}$ before $\overline{CPAB}$ or $\overline{CEBA}$ before $\overline{CPBA}$	4	1.0 1.0	−0.3 −0.5	ns
th(H) th(L)	Hold time $\overline{CEAB}$ after $\overline{CPAB}$ or $\overline{CEBA}$ after $\overline{CPBA}$	4	1.5 1.5	0.8 0.5	ns
tw(H) tw(L)	Pulse width, High or Low $\overline{CPAB}$ or $\overline{CPBA}$	1	2.5 2.5		ns
tw(H)	LEAB or LEBA pulse width, High	3	1.5		ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

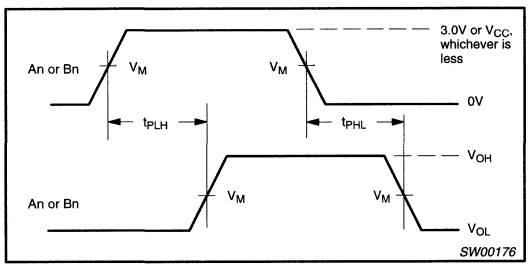
AC WAVEFORMS

NOTES:

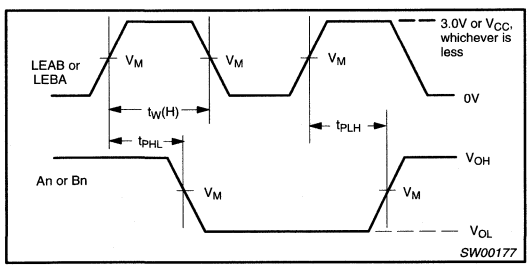
1. $V_M = 1.5V$ at $V_{CC} \geq 3.0V$, $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7V$
2. $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 3.0V$, $V_X = V_{OL} + 0.15V$ at $V_{CC} \leq 2.7V$
3. $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 3.0V$, $V_Y = V_{OH} - 0.15V$ at $V_{CC} \leq 2.7V$



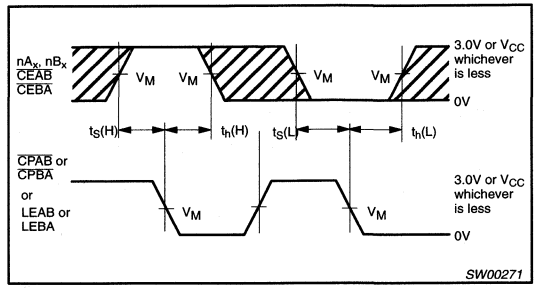
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



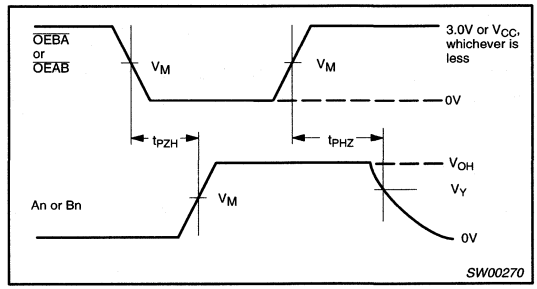
Waveform 2. Propagation Delay, Transparent Mode



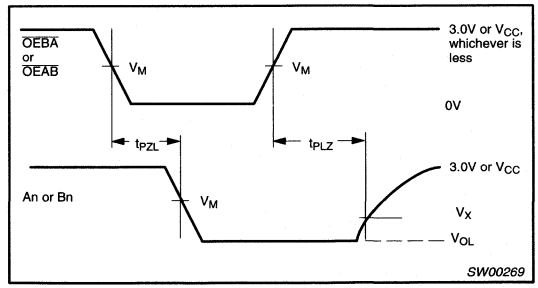
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 4. Data Setup and Hold Times

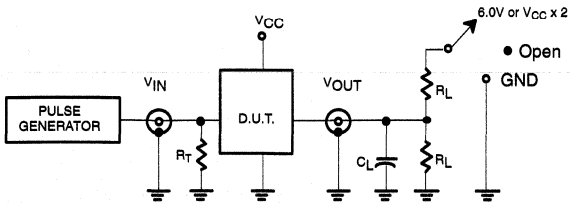


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

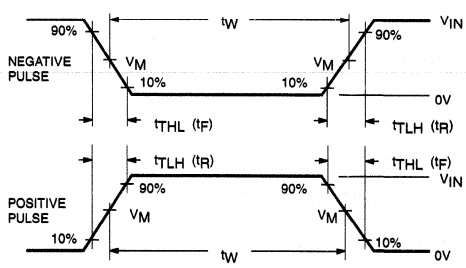


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

2.5V/3.3V 18-bit universal bus transceiver (3-State) 74ALVT16601

FEATURES

- 18-bit bidirectional bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Positive edge triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16601 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V and 3.3V with I/O compatibility up to 5V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When $\overline{OEAB}$ is Low, the outputs are active. When $\overline{OEAB}$ is High, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs ($\overline{CEBA}$/$\overline{CEAB}$).

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and CPBA.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF	1.9 2.5	1.5 1.9	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or V_{CC}	4	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or V_{CC}	8	8	pF
I_{CCZ}	Total supply current	Outputs disabled	40	60	µA

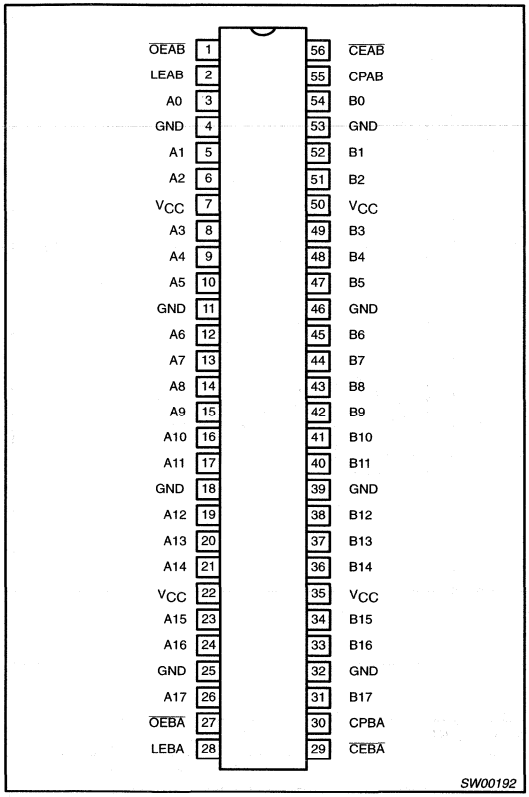
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16601 DL	AV16601 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16601 DGG	AV16601 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 27	$\overline{OEAB}$/$\overline{OEBA}$	A-to-B/ B-to-A Output enable input (active Low)
29, 56	$\overline{CEBA}$/$\overline{CEAB}$	B-to-A/A-to-B clock enable
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION

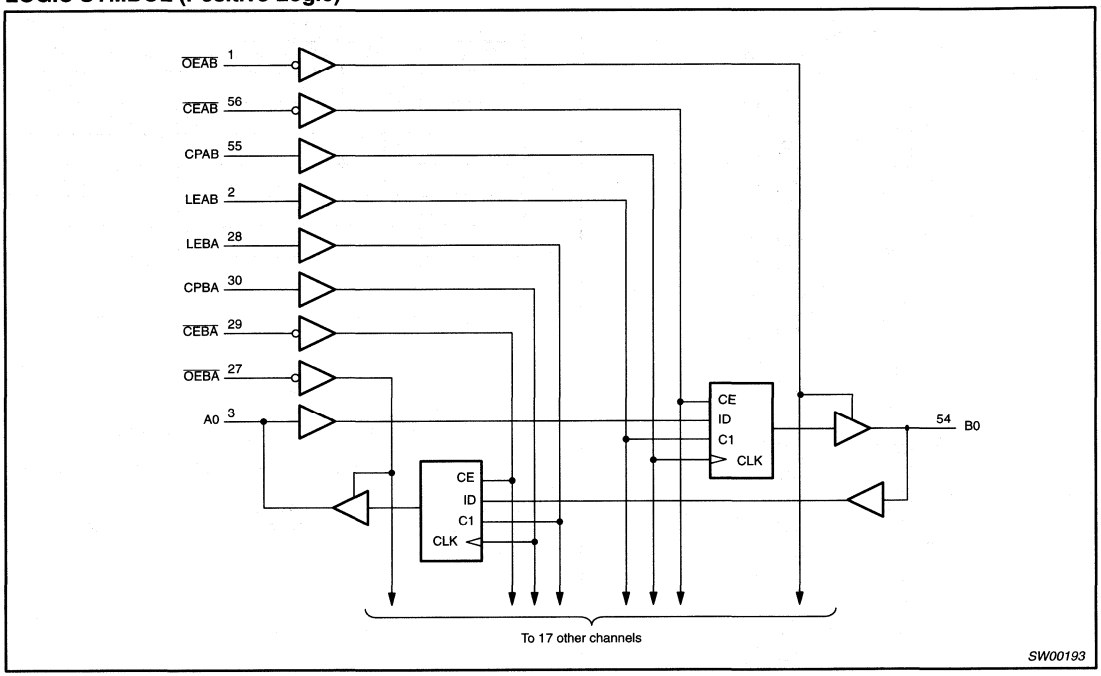


FUNCTION TABLE

INPUTS					OUTPUT
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CPAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	$B_O^{\pm}$
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	H	X	$B_O^{\pm}$
L	L	L	L	X	$B_O^{\S}$

X = Don't care
H = High voltage level
L = Low voltage level
↑ = Low to High
Z = High impedance "off" state
† = A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CPBA, and $\overline{CEBA}$.
$^{\pm}$ = Output level before the indicated steady-state input conditions were established.
§ = Output level before the indicated steady-state input conditions were established, provided that CPAB was Low before LEAB went Low.

LOGIC SYMBOL (Positive Logic)



ABSOLUTE MAXIMUM RATINGS [1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1.0	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.06	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1				MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.5 1.9	2.3 2.9	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	1.5 1.5	2.2 2.6	3.5 3.9	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.5 1.5	2.2 2.9	3.3 4.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.0 1.0	2.3 1.6	3.9 2.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	2.9 2.4	4.1 3.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low An to CPAB or Bn to CPBA	4	1.5 1.5	0.4 0.6	ns
th(H) th(L)	Hold time, High or Low An to CPAB or Bn to CPBA	4	1.0 1.0	–0.5 –0.3	ns
ts(H) ts(L)	Setup time, High or Low Clock Low An to LEAB or Bn to LEBA	4	1.0 1.0	–0.5 –0.1	ns
th(H) th(L)	Hold time, High or Low Clock High An to LEAB or Bn to LEBA	4	1.5 1.5	0.1 0.5	ns
ts(H) ts(L)	Setup time $\overline{CEAB}$ before CPAB or $\overline{CEBA}$ before CPBA	4	1.5 1.0	0.3 –0.4	ns
th(H) th(L)	Hold time $\overline{CEAB}$ after CPAB or $\overline{CEBA}$ after CPBA	4	1.5 1.0	0.7 –0.3	ns
tw(H) tw(L)	Pulse width, High or Low CPAB or CPBA	1	2.0 2.0		ns
tw(H)	LEAB or LEBA pulse width, High	3	1.5		ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8			
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	Data pins[4]		0.1	20	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–75		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			1	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.5	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1				MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.9 2.5	3.0 3.7	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	2.0 2.0	3.1 3.5	4.6 5.2	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.0 2.0	3.4 4.0	5.0 5.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	2.0 1.0	3.3 2.1	4.8 3.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.0	2.6 1.9	4.2 3.4	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

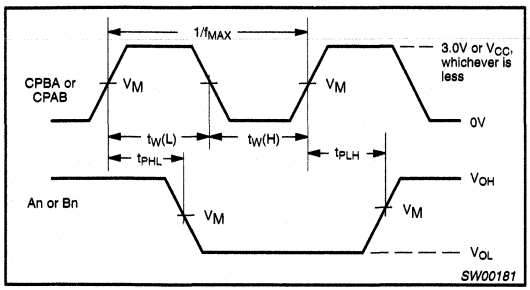
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low An to CPAB or Bn to CPBA	4	2.0 2.0	0.4 1.2	ns
th(H) th(L)	Hold time, High or Low An to CPAB or Bn to CPBA	4	0.0 0.0	–1.1 –0.3	ns
ts(H) ts(L)	Setup time, High or Low Clock Low or High An to LEAB or Bn to LEBA	4	0.0 1.5	–1.0 0.4	ns
th(H) th(L)	Hold time, High or Low Clock Low or High An to LEAB or Bn to LEBA	4	1.5 1.9	0.4 1.0	ns
ts(H) ts(L)	Setup time $\overline{CEAB}$ before CPAB or $\overline{CEBA}$ before CPBA	4	1.0 0.3	0.3 –0.4	ns
th(H) th(L)	Hold time $\overline{CEAB}$ after CPAB or $\overline{CEBA}$ after CPBA	4	2.0 0.5	0.4 –0.1	ns
tw(H) tw(L)	Pulse width, High or Low CPAB or CPBA	1	3.0 3.0		ns
tw(H)	LEAB or LEBA pulse width, High	3	1.5		ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

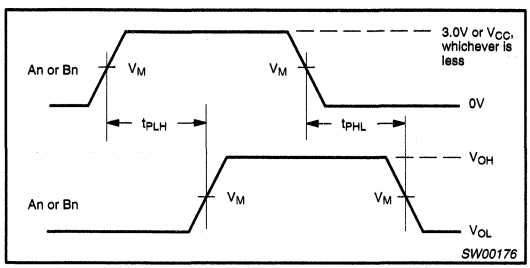
AC WAVEFORMS

NOTES:

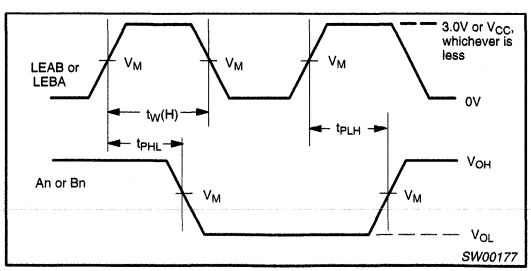
1. V_M = 1.5V at V_{CC} ≥ 3.0V, $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V
2. $V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V, $V_X = V_{OL}$ + 0.150V · V_{CC} at V_{CC} ≤ 2.7V
3. $V_Y = V_{OH}$ − 0.3V at V_{CC} ≥ 3.0V, $V_Y = V_{OH}$ − 0.150V · V_{CC} at V_{CC} ≤ 2.7V



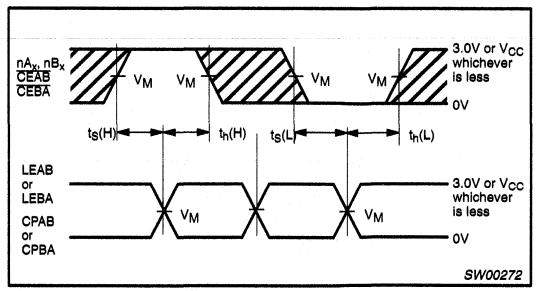
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



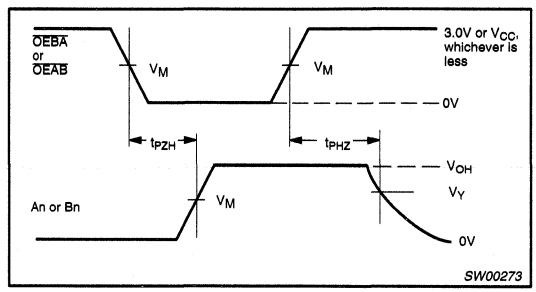
Waveform 2. Propagation Delay, Transparent Mode



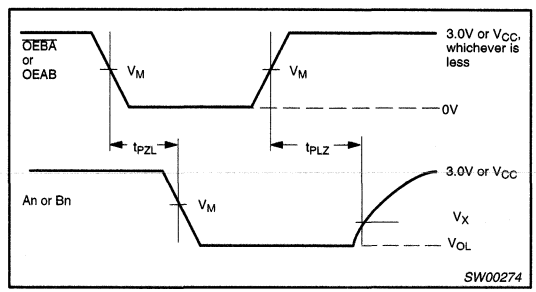
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 4. Data Setup and Hold Times

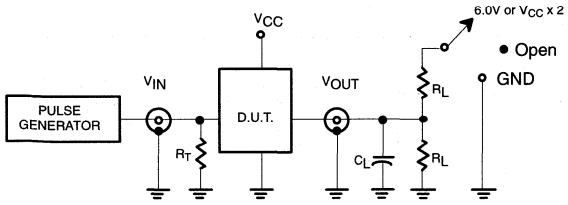


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

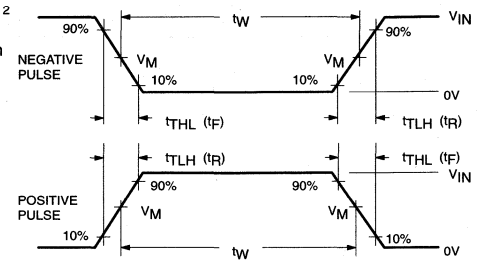


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤2.5ns	≤2.5ns

SW00220

2.5V/3.3V 16-bit bus transceiver (3-State) 74ALVT16646

FEATURES

- 16-bit universal bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16646 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

Data on the A or B bus is clocked into the registers on the Low to High transition of the appropriate clock (CPAB or CPBA). The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode data).

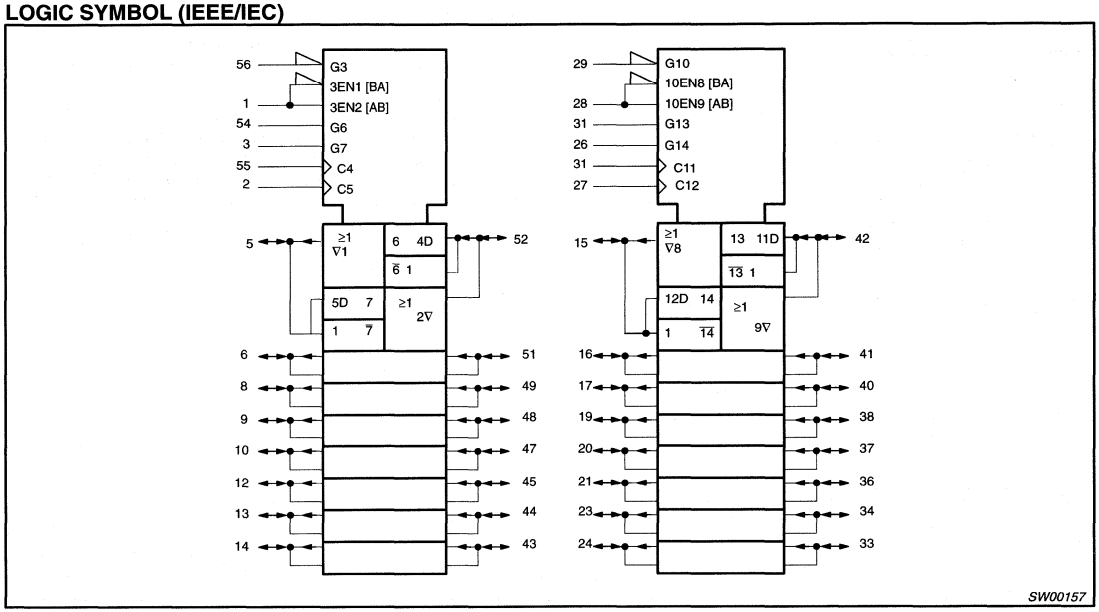
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF	2.2 2.3	1.7 1.8	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

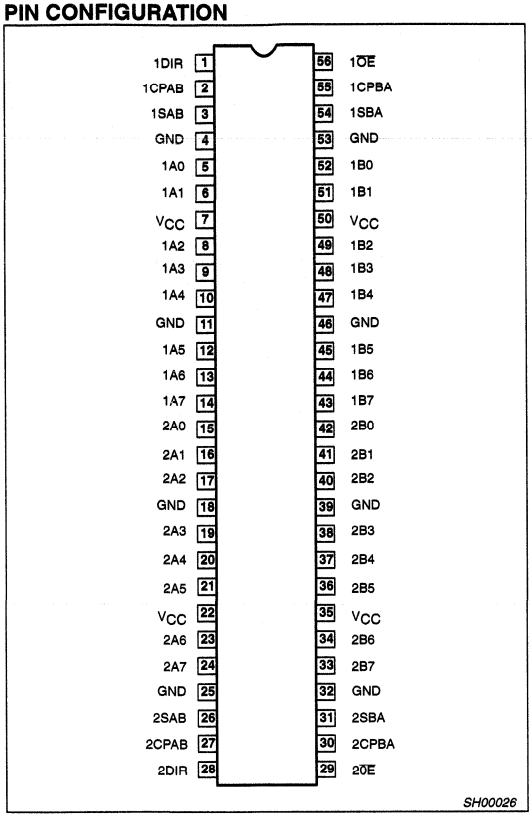
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT166646 DL	AV16646 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16646 DGG	AV16646 DGG	SOT364-1

LOGIC SYMBOL (IEEE/IEC)

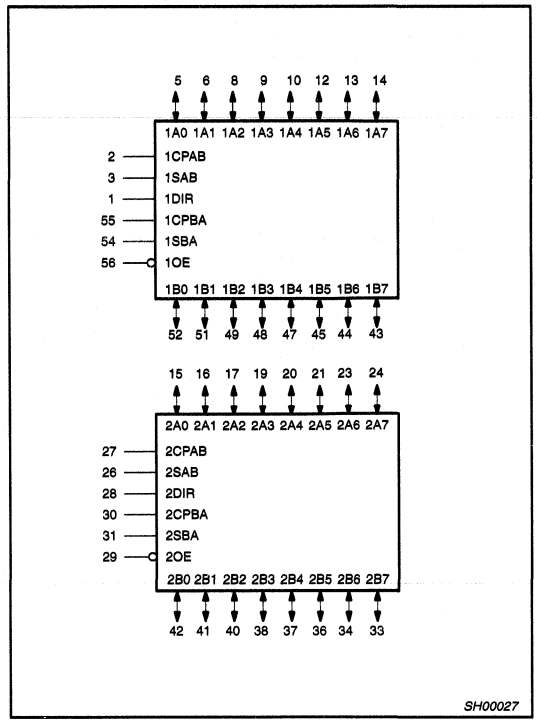


2.5V/3.3V 16-bit bus transceiver (3-State) 74ALVT16646

PIN CONFIGURATION



LOGIC SYMBOL

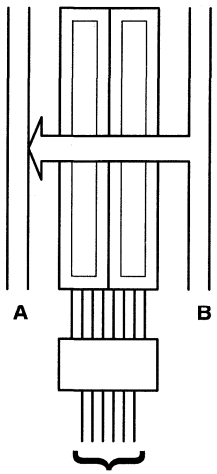


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
1, 28	1DIR, 2DIR	Direction control inputs
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 - 1A7, 2A0 - 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 - 1B7, 2B0 - 2B7	Data inputs/outputs (B side)
56, 29	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

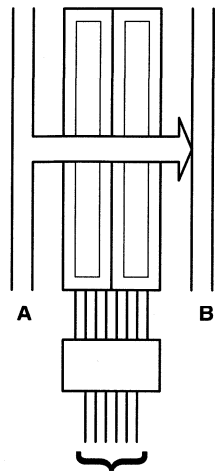
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ALVT16646.

REAL TIME BUS TRANSFER BUS B TO BUS A



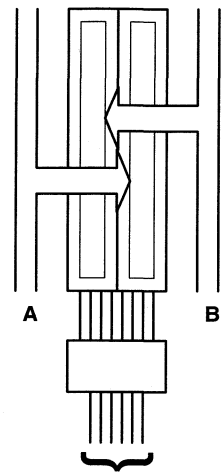
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



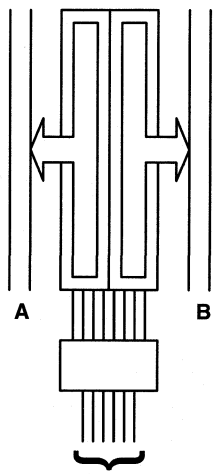
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	↑	X	X	X
L	L	X	↑	X	X
H	X	↑	↑	X	X

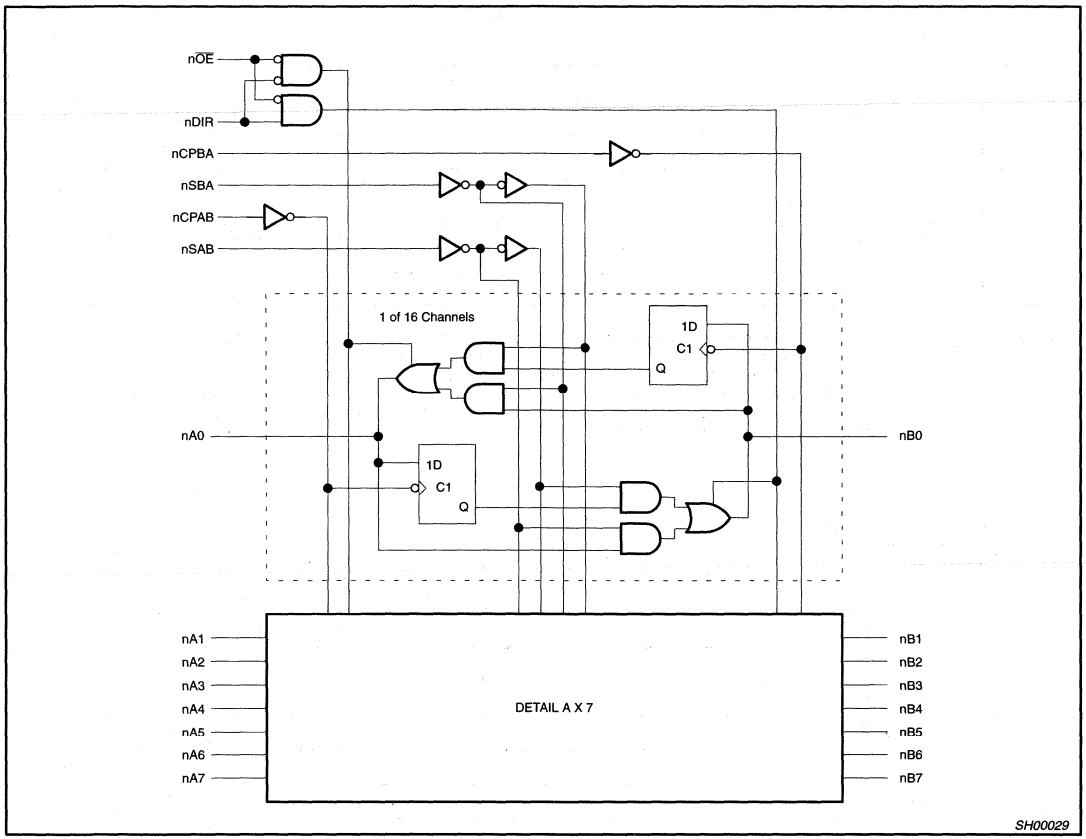
TRANSFER STORED DATA TO A OR B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

SH00028

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOE	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOE input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		µA
		V_{CC} = 3.0V; V_I = 0V to 3.6V		±500			µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.14	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.2	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.14	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.0 1.0	2.6 2.1	3.7 3.1	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	2	1.0 1.0	2.4 2.1	4.0 3.8	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2 3	0.5 0.5	1.7 1.8	2.4 2.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	0.5 0.5	2.3 2.0	3.9 4.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	3.4 2.8	5.0 4.2	ns
t_{PZH} t_{PZL}	Output enable time nDIR to nAx or nBx	5 6	1.0 0.5	2.8 2.2	5.0 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time nDIR to nAx or nBx	5 6	1.5 1.0	3.5 3.1	5.4 4.7	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP[1]	
t_S(H) t_S(L)	Setup time, High or Low nAx to nCPAB or nBx to nCPBA	4	1.6 1.6	1.0 1.0	ns
t_h(H) t_h(L)	Hold time, High or Low nAx to nCPAB or nBx or nCPBA	4	0.0 0.0	–0.5 –0.7	ns
t_w(H) t_w(L)	Pulse width, High or Low nCPAB or nCPBA	1	1.5 1.5		ns

NOTE:
1. This data sheet limit may vary among suppliers.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.0 1.0	3.2 2.8	4.8 4.2	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	2	1.5 1.5	3.4 3.4	5.8 6.0	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2 3	0.5 0.5	2.2 2.3	3.2 3.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.5 1.0	3.4 2.7	5.8 6.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.0	3.2 2.5	5.2 3.7	ns
t_{PZH} t_{PZL}	Output enable time nDIR to nAx or nBx	5 6	2.0 1.0	4.1 2.5	7.0 4.1	ns
t_{PHZ} t_{PLZ}	Output disable time nDIR to nAx or nBx	5 6	1.5 1.0	3.9 3.1	6.1 4.9	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

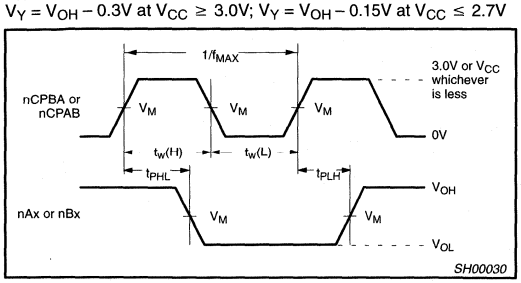
AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

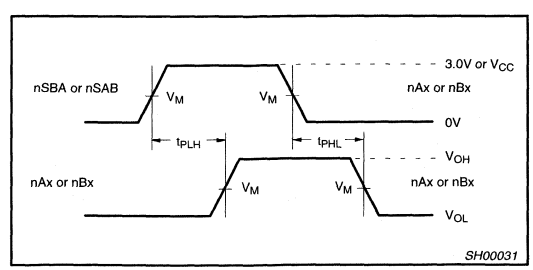
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP	
t_S(H) t_S(L)	Setup time, High or Low nAx to nCPAB or nBx to nCPBA	4	2.0 2.0	1.2 1.2	ns
t_h(H) t_h(L)	Hold time, High or Low nAx to nCPAB or nBx or nCPBA	4	0.0 0.0	–1.0 –1.0	ns
t_w(H) t_w(L)	Pulse width, High or Low nCPAB or nCPBA	1	1.5 1.5		ns

AC WAVEFORMS

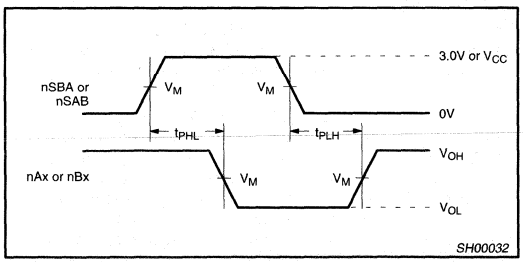
V_M = 1.5V at V_{CC} ≥ 3.0V; $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V; $V_X = V_{OL}$ + 0.15V at V_{CC} ≤ 2.7V
$V_Y = V_{OH}$ – 0.3V at V_{CC} ≥ 3.0V; $V_Y = V_{OH}$ – 0.15V at V_{CC} ≤ 2.7V



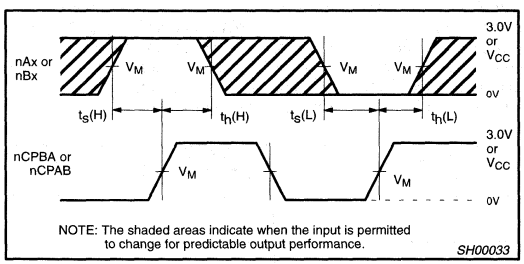
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



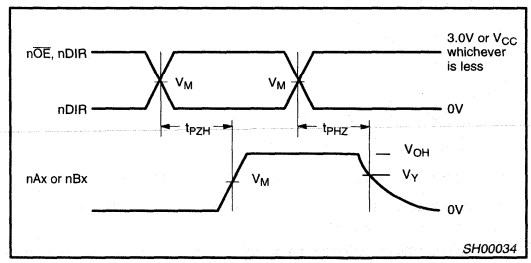
Waveform 2. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx



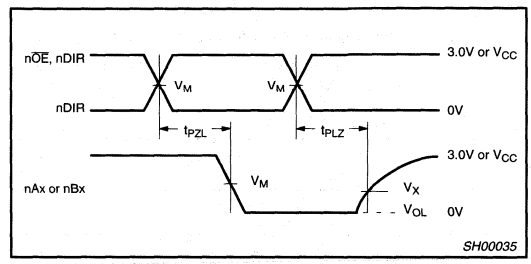
Waveform 3. Propagation Delay, nSBA to nAx or nSAB to nBx



Waveform 4. Data Setup and Hold Times

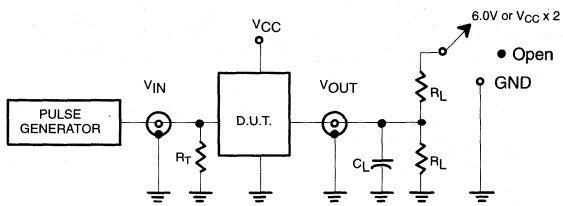


Waveform 5. 3–State Output Enable Time to High Level and Output Disable Time from High Level

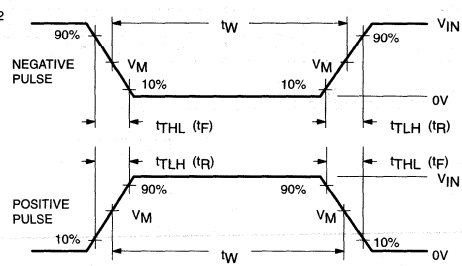


Waveform 6. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

2.5V/3.3V 16-bit bus transceiver/register (3-State)

74ALVT16652

FEATURES

- 16–bit bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16652 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complimentary output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A Low-input level selects real-time data, and a High input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

Data on the A or B bus, or both, can be stored in the internal flip-flops by Low-to-High transitions at the appropriate clock (CPAB or CPBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

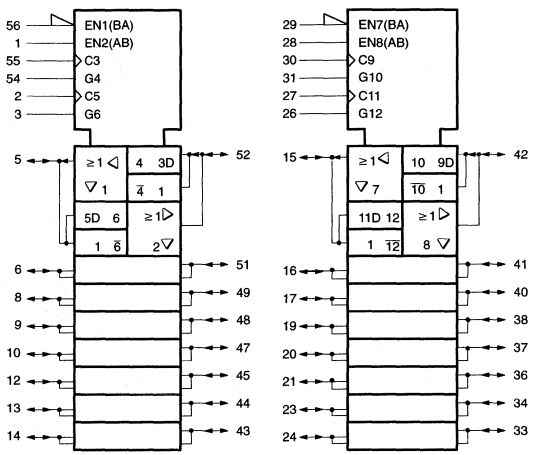
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF	2.0 2.1	1.5 1.6	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16652 DL	AV16652 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16652 DGG	AV16652 DGG	SOT364-1

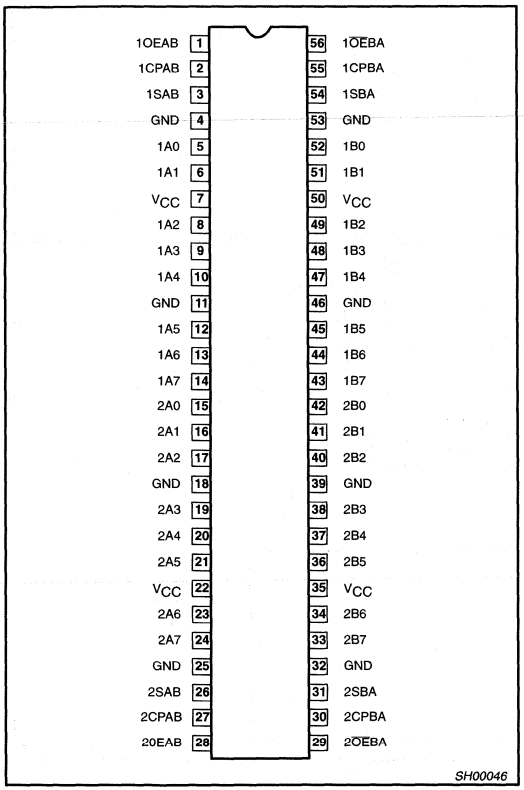
LOGIC SYMBOL (IEEE/IEC)



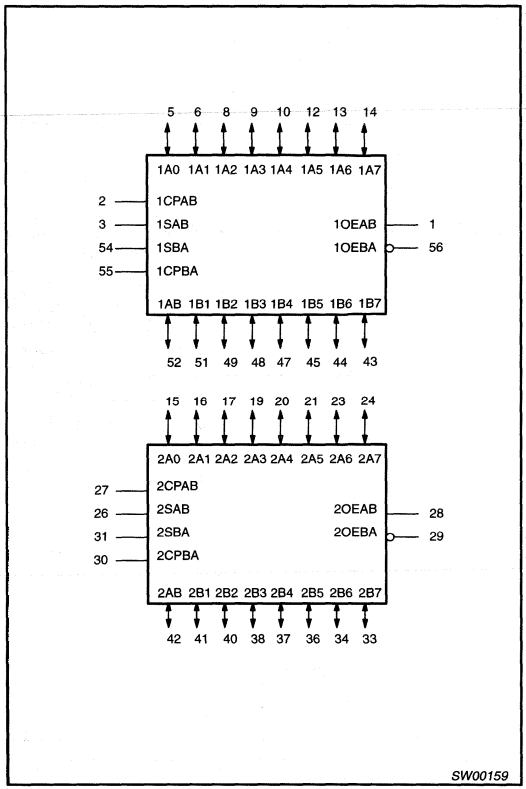
2.5V/3.3V 16-bit bus transceiver/register (3-State)

74ALVT16652

PIN CONFIGURATION



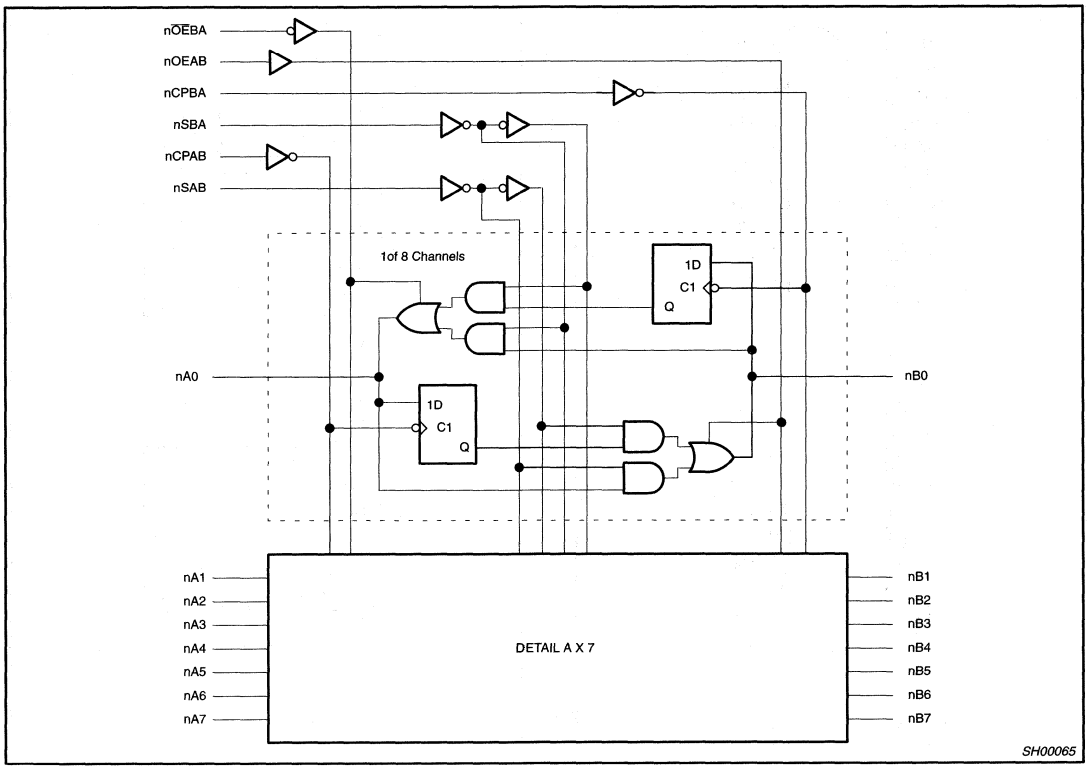
LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
1, 56, 28, 29	1OEAB, 1$\overline{\text{OEBA}}$, 2OEAB, 2$\overline{\text{OEBA}}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



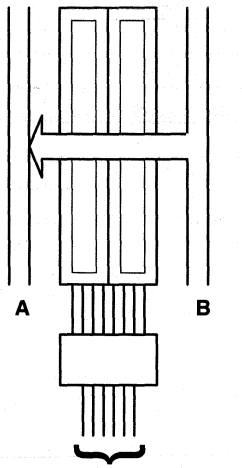
FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOEBA and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (nSAB and nSBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

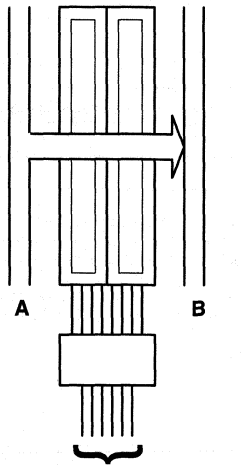
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ALVT16652. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

REAL TIME BUS TRANSFER BUS B TO BUS A



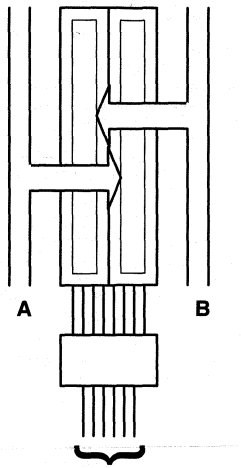
nOEAB	nŌEBA	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



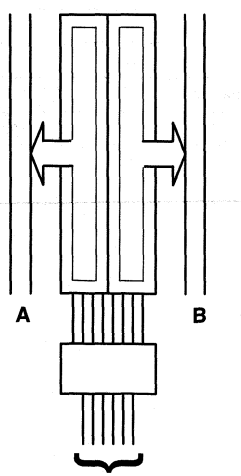
nOEAB	nŌEBA	nCPAB	nCPBA	nSAB	nSBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



nOEAB	nŌEBA	nCPAB	nCPBA	nSAB	nSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



nOEAB	nŌEBA	nCPAB	nCPBA	nSAB	nSBA
H	L	H|L	H|L	H	H

SH00066

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		µA
		V_{CC} = 3.0V; V_I = 0V to 3.6V		±500			µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.14	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.2	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.14	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	150	300		MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.0 1.0	2.4 2.1	3.6 3.2	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	0.5 0.5	1.5 1.6	2.5 2.7	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	3	0.5 0.5	2.4 2.1	3.9 3.9	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OEBA}$ to nAx	5 6	0.5 0.5	2.3 1.5	3.6 2.5	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OEBA}$ to nAx	5 6	1.5 1.0	3.4 2.6	5.0 3.8	ns
t_{PZH} t_{PZL}	Output enable time nOEAB to nBx	5 6	0.5 0.5	2.4 1.7	3.6 2.6	ns
t_{PHZ} t_{PLZ}	Output disable time nOEAB to nBx	5 6	1.5 1.5	3.8 3.1	5.8 4.5	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V, t_R = 2.5ns, t_F = 2.5ns, C_L = 50pF, R_L = 500Ω, T_{amb} = −40 °C to +85 °C

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time nAx to nCPAB, nBx to nCPBA	4	1.6 1.6	0.8 0.6	ns
t_h(H) t_h(L)	Hold time nAx to nCPAB, nBx to nCPBA	4	0.5 0	−0.5 −0.8	ns
t_w(H) t_w(L)	Pulse width, High or Low nCPAB or nCPBA	1	1.5 1.5		ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			40	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.5	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ± 0.2V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	150	200		MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.0 1.0	3.0 2.7	4.9 4.2	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	0.5 0.5	2.0 2.1	3.2 3.5	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	3	1.5 1.5	3.4 3.2	5.2 5.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{nOEBA}$ to nAx	5 6	1.5 0.5	3.2 2.0	4.7 3.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{nOEBA}$ to nAx	5 6	1.5 1.8	3.2 2.3	4.8 3.5	ns
t_{PZH} t_{PZL}	Output enable time nOEAB to nBx	5 6	1.5 1.0	3.3 2.5	4.9 3.6	ns
t_{PHZ} t_{PLZ}	Output disable time nOEAB to nBx	5 6	2.0 1.0	3.9 2.3	5.9 6.0	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

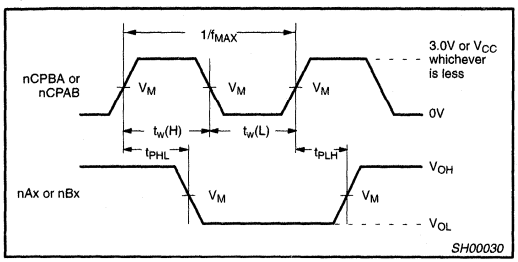
GND = 0V, t_R = 2.5ns, t_F = 2.5ns, C_L = 50pF, R_L = 500Ω, T_{amb} = –40 °C to +85 °C

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time [1] nAx to nCPAB, nBx to nCPBA	4	1.8 2.0	0.9 1.0	ns
t_h(H) t_h(L)	Hold time [1] nAx to nCPAB, nBx to nCPBA	4	0.0 0.0	–1.0 –1.0	ns
t_w(H) t_w(L)	Pulse width, High or Low nCPAB or nCPBA	1	1.5 1.5		ns

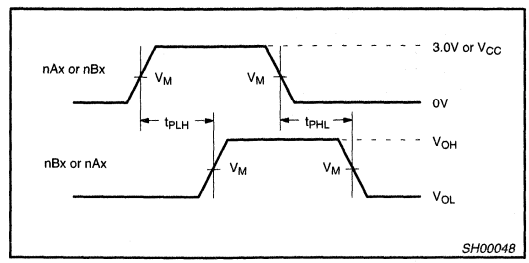
NOTE:
1. This data sheet limit may vary among suppliers.

AC WAVEFORMS

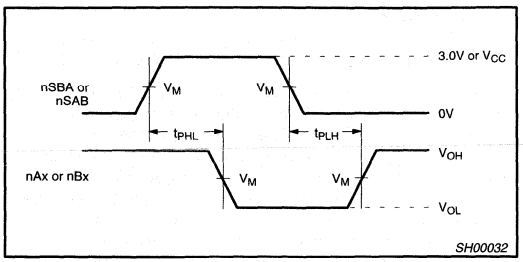
V_M = 1.5V at V_{CC} ≥ 3.0V; $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V; $V_X = V_{OL}$ + 0.15V at V_{CC} ≤ 2.7V
$V_Y = V_{OH}$ – 0.3V at V_{CC} ≥ 3.0V; $V_Y = V_{OH}$ – 0.15V at V_{CC} ≤ 2.7V



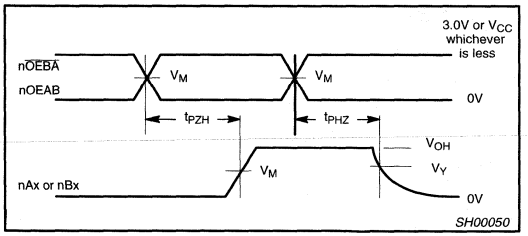
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



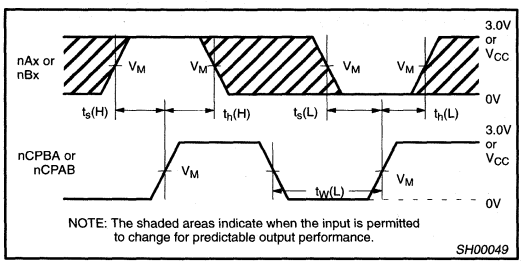
Waveform 2. Propagation Delay, nAx to nBx or nBx to nAx



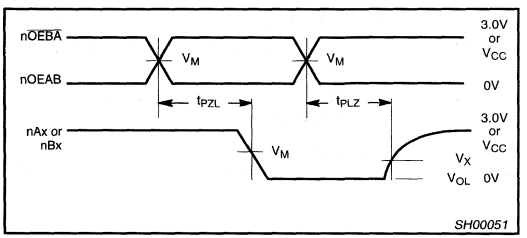
Waveform 3. Propagation Delay, SBA to nAx or SAB to nBx



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

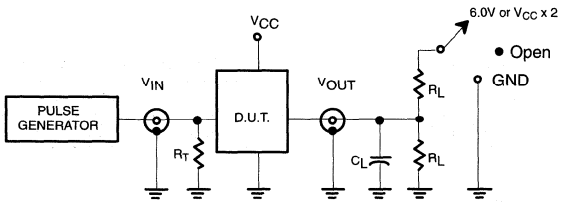


Waveform 4. Data Setup and Hold Times

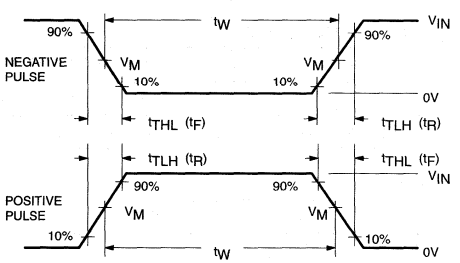


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00025

2.5V/3.3V 1-to-4 address register/driver (3-State) 74ALVT16731

FEATURES

- 5V I/O Compatible
- 3-State outputs
- Output capability: +64 mA/-32 mA
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Positive edge triggered registers
- Latch-up protection exceeds 500 mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per machine model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT16731 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V to 3.3V with I/O compatibility up to 5V.

This device is a 1-to-4 address register/driver featuring non-inverting 3-State outputs. The state of the outputs are controlled by two enable inputs (OE1 and OE2). Each enable input controls the state of two of the four common outputs for each input. When an OEn input is a logic High, the respective outputs will be in the high impedance state. When an OEn input is a logic Low, the respective outputs are active. The device can be configured for a transparent mode from input to output or a register mode by the SEL input. When SEL is a logic High the device is configured for transparent mode and when SEL is a logic Low it is configured for register mode. While in the register mode the output follows the input on the rising edge of the CLK input. The function of the data registers is not effected by either SEL or OEn.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF	2.4	1.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

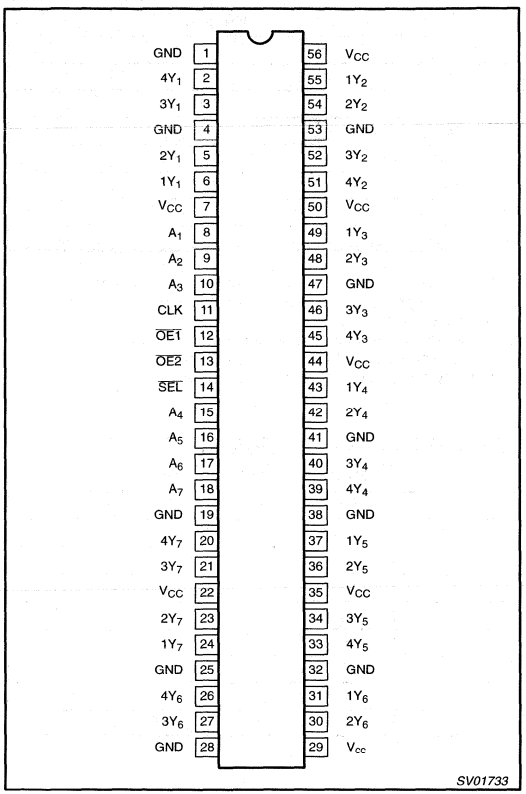
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16731 DL	AV16731 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16731 DGG	AV16731 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 19, 25, 28, 32, 38, 41, 47, 53	GND	Ground
5, 6, 23, 24, 30, 31, 36, 37, 42, 43, 48, 49, 54, 55	$1Y_n$, $2Y_n$	Output, controlled by OE1
2, 3, 20, 21, 26, 27, 33, 34, 39, 40, 45, 46, 51, 52	$3Y_n$,$4Y_n$	Output, controlled by OE2
7, 22, 29, 35, 44, 50, 56	V_{CC}	Positive power supply
8, 9, 10, 15, 16, 17, 18	A_n	Data inputs
14	SEL	Select input, controls mode of device
11	CLK	Clock input
12, 13	OE_n	Output enable

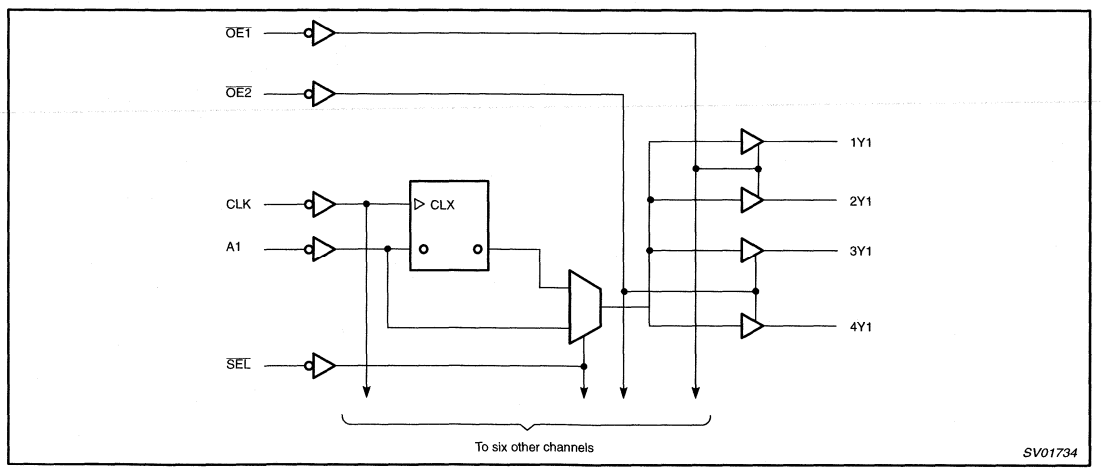
PIN CONFIGURATION



FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}$	$\overline{SEL}$	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	H	↑	H	H

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			6	8	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	1.7 1.7	2.4 2.4	ns
t_{PLH} t_{PHL}	Propagation delay CLK to Y	3	1.5 1.5	2.3 2.3	3.2 3.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.3 2.0	3.8 3.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	2.7 2.3	4.2 3.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low Ax to nYx	4	1.5 1.5	1.0 1.0	ns
th(H) th(L)	Hold time, High or Low Ax to nYx	4	0 0	–0.9 –0.9	ns
tw(H) tw(L)	Pulse width, High or Low CLK	3	1.5 1.5		ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.3	6.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 2.5V ±0.2V MIN	TYP[1]	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	1.8 1.9	3.0 3.0	ns
t_{PLH} t_{PHL}	Propagation delay CLK to Y	3	2.2 2.2	3.2 3.2	4.4 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	2.0 2.0	3.5 3.5	5.9 5.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.5 3.0	5.0 4.0	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

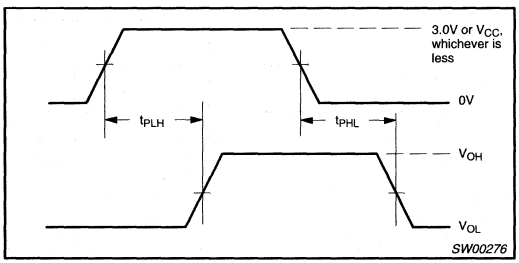
GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low Ax to nYx	4	2.4 2.3	0.9 0.8	ns
th(H) th(L)	Hold time, High or Low Ax to nYx	4	0 0	–0.7 –0.6	ns
tw(H) tw(L)	Pulse width, High or Low CLK	3	1.5 1.5		ns

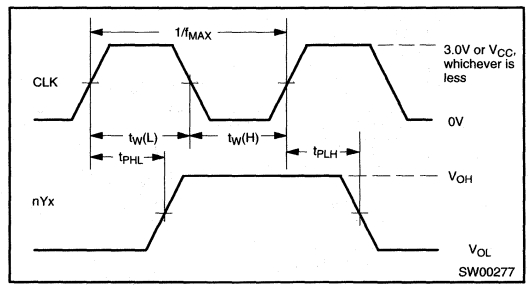
NOTE:
1. All typical values are at $V_{CC} = 2.5V$ and $T_{amb} = 25°C$.

AC WAVEFORMS

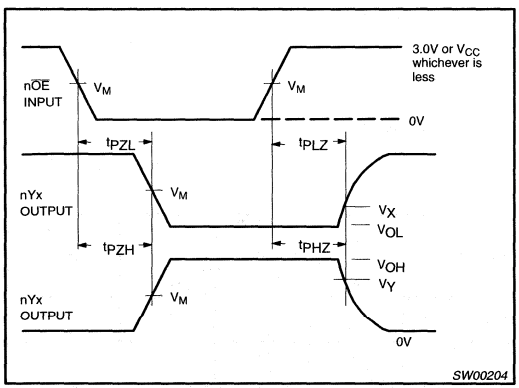
NOTES:
1. $V_M = 1.5V$ at $V_{CC} \geq 3.0V$, $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7V$
2. $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 3.0V$, $V_X = V_{OL} + 0.150V$ at $V_{CC} \leq 2.7V$
3. $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 3.0V$, $V_Y = V_{OH} - 0.150V$ at $V_{CC} \leq 2.7V$



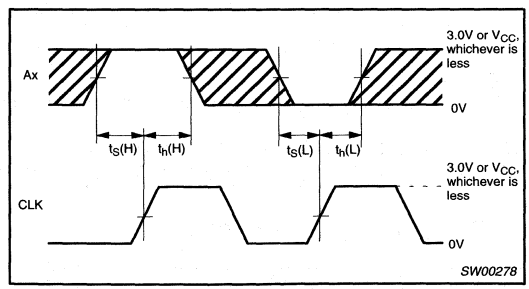
Waveform 1. Input (Ax) to Output (nYx) Propagation Delay, transparent mode



Waveform 3. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

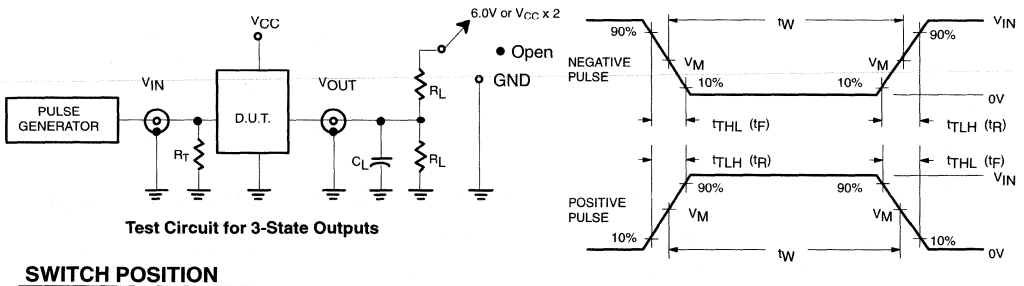


Waveform 2. 3-State Output Enable and Disable Times



Waveform 4. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

2.5V/3.3V 1-to-4 address register/driver with 30Ω termination resistors (3-State)

74ALVT162731

FEATURES

- 5V I/O Compatible
- 3-State outputs
- Output capability: +64 mA/-32 mA
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Positive edge triggered registers
- Latch-up protection exceeds 500 mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per machine model
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT162731 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V to 3.3V with I/O compatibility up to 5V.

This device is a 1-to-4 address register/driver featuring non-inverting 3-State outputs. The state of the outputs are controlled by two enable inputs (OE1 and OE2). Each enable input controls the state of two of the four common outputs for each input. When an OEn input is a logic High, the respective outputs will be in the high impedance state. When an OEn input is a logic Low, the respective outputs are active. The device can be configured for a transparent mode from input to output or a register mode by the SEL input. When SEL is a logic High the device is configured for transparent mode and when SEL is a logic Low it is configured for register mode. While in the register mode the output follows the input on the rising edge of the CLK input. The function of the data registers is not effected by either SEL or OEn.

The 74ALVT162731 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF	2.4	1.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162731 DL	AV162731 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162731 DGG	AV162731 DGG	SOT364-1

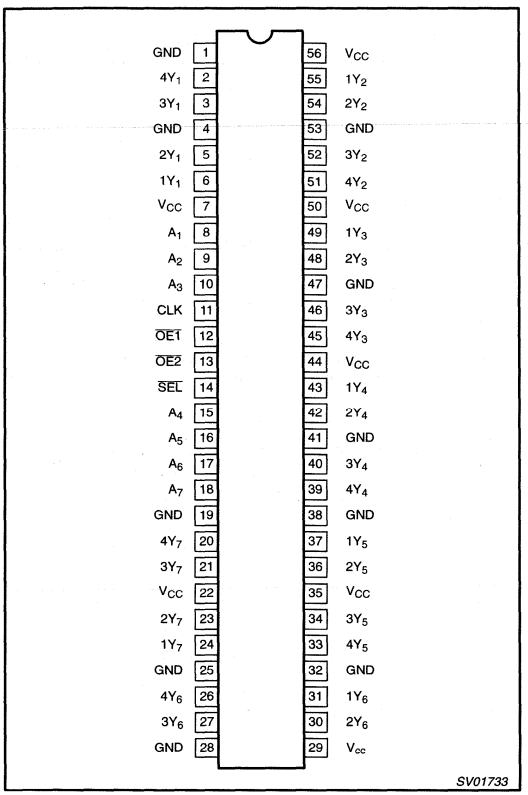
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 19, 25, 28, 32, 38, 41, 47, 53	GND	Ground
5, 6, 23, 24, 30, 31, 36, 37, 42, 43, 48, 49, 54, 55	$1Y_n$, $2Y_n$	Output, controlled by OE1
2, 3, 20, 21, 26, 27, 33, 34, 39, 40, 45, 46, 51, 52	$3Y_n$,$4Y_n$	Output, controlled by OE2
7, 22, 29, 35, 44, 50, 56	V_{CC}	Positive power supply
8, 9, 10, 15, 16, 17, 18	A_n	Data inputs
14	SEL	Select input, controls mode of device
11	CLK	Clock input
12, 13	OE_n	Output enable

2.5V/3.3V 1-to-4 address register/driver with 30Ω termination resistors (3-State)

74ALVT162731

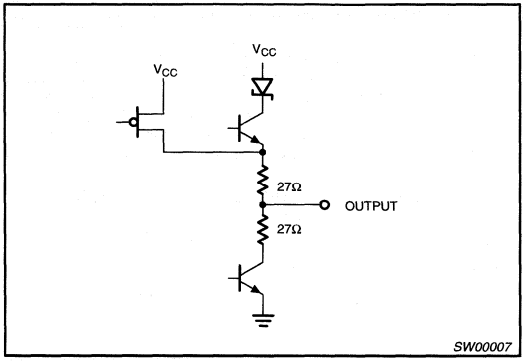
PIN CONFIGURATION



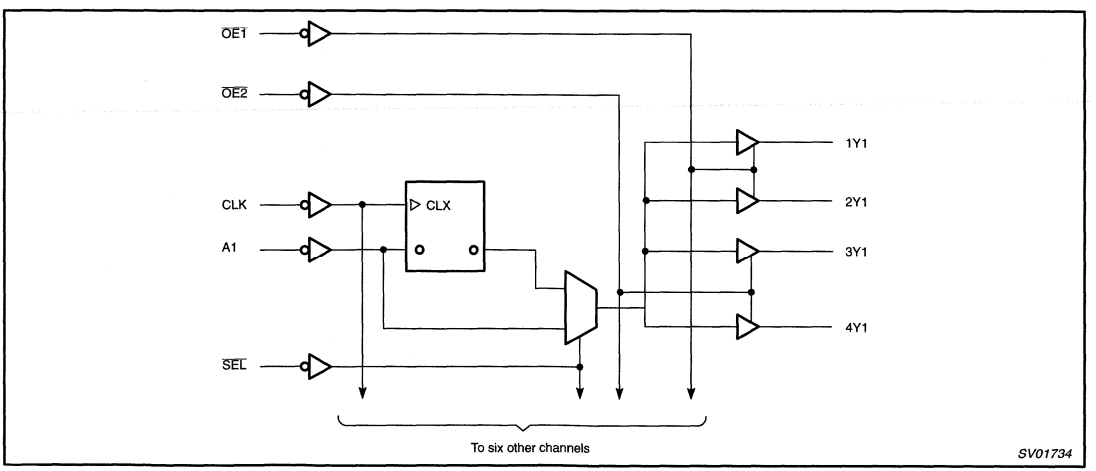
FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}$	SEL	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	H	↑	H	H

SCHEMATIC OF EACH OUTPUT



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			6	8	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.5 1.5	2.7 2.7	3.5 3.5	ns
t_{PLH} t_{PHL}	Propagation delay CLK to Y	3	2.0 2.0	3.3 3.3	4.2 4.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	3.3 3.0	4.8 4.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	2.0 2.0	3.7 3.2	5.2 4.8	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low Ax to nYx	4	1.5 1.5	1.0 1.0	ns
th(H) th(L)	Hold time, High or Low Ax to nYx	4	0 0	−0.9 −0.9	ns
tw(H) tw(L)	Pulse width, High or Low CLK	3	1.5 1.5		ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} OE/$\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.3	6.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 2.5V ±0.2V MIN	TYP[1]	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.5 1.5	2.9 2.9	4.0 4.0	ns
t_{PLH} t_{PHL}	Propagation delay CLK to Y	3	3.0 3.0	4.2 4.2	5.4 5.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	2.0 2.0	3.5 3.5	5.9 5.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	2.7 2.0	5.0 4.0	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

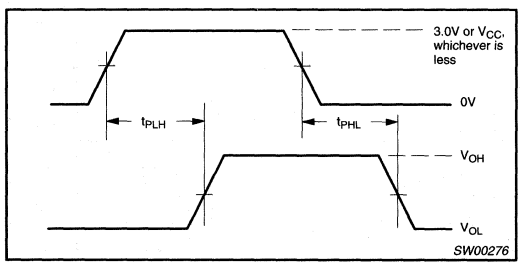
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low nYx to CLK	4	2.4 2.3	0.9 0.8	ns
th(H) th(L)	Hold time, High or Low nYx to CLK	4	0 0	–0.7 –0.6	ns
tw(H) tw(L)	Pulse width, High or Low CLK	3	1.5 1.5		ns

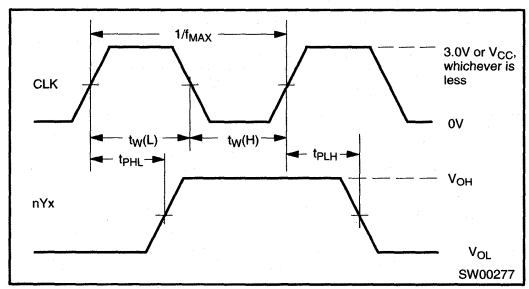
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS

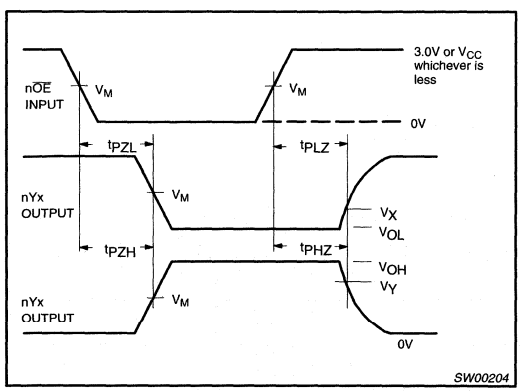
NOTES:
1. V_M = 1.5V at $V_{CC} \geq$ 3.0V, $V_M = V_{CC}/2$ at $V_{CC} \leq$ 2.7V
2. $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq$ 3.0V, $V_X = V_{OL} + 0.150V$ at $V_{CC} \leq$ 2.7V
3. $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq$ 3.0V, $V_Y = V_{OH} - 0.150V$ at $V_{CC} \leq$ 2.7V



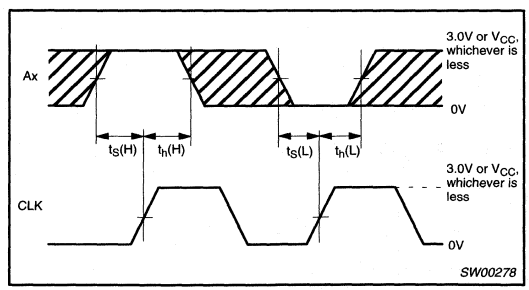
Waveform 1. Input (Ax) to Output (nYx) Propagation Delay, transparent mode



Waveform 3. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

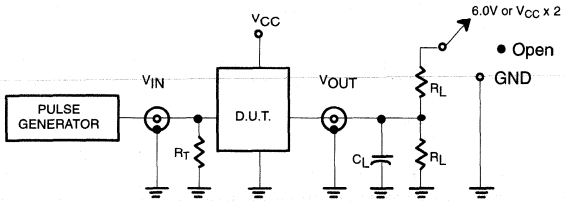


Waveform 2. 3-State Output Enable and Disable Times

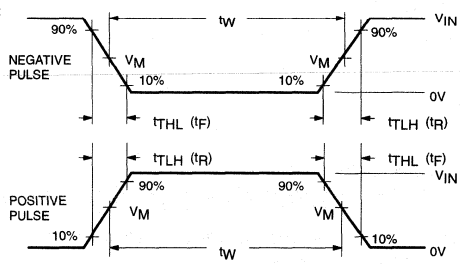


Waveform 4. Data setup and hold times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤2.5ns	≤2.5ns

SW00025

2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVT16821

FEATURES

- 20-bit positive-edge triggered register
- 5V I/O Compatible
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT16821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT16821 has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($n\overline{OE}$) controls all ten 3-State buffers independent of the register operation. When $n\overline{OE}$ is Low, the data in the register appears at the outputs. When $n\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nCP to nQ	C_L = 50pF	2.6 2.7	1.7 1.8	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	V_O = 0 or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

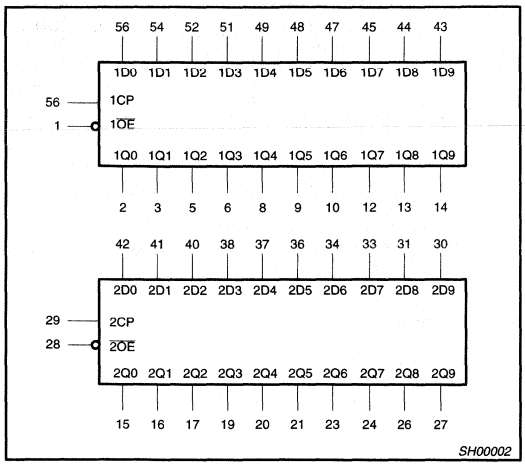
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16821 DL	AV16821 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16821 DGG	AV16821 DGG	SOT364-1

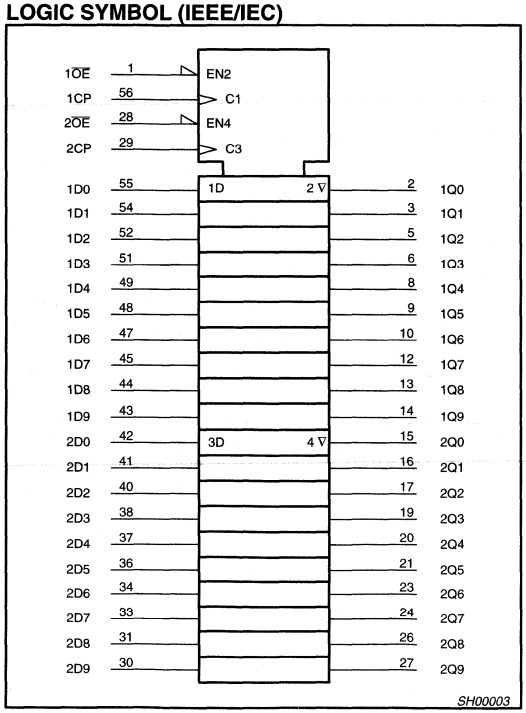
2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVT16821

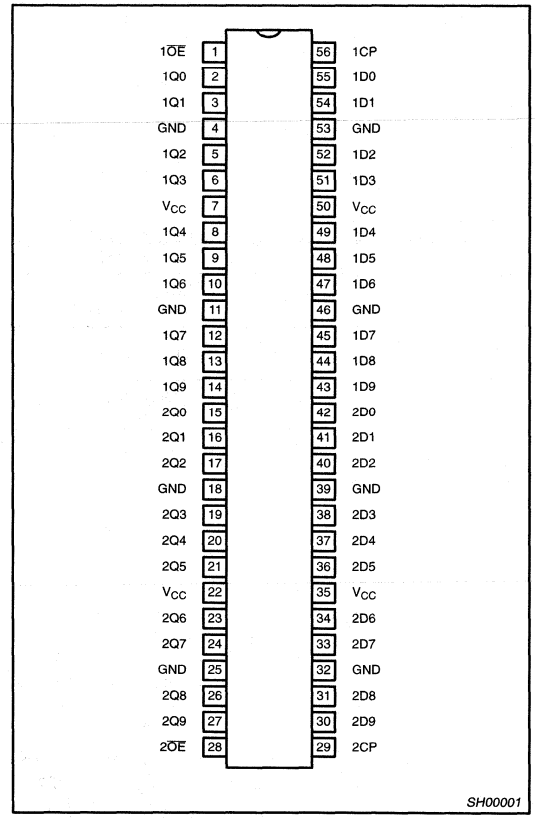
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVT16821

PIN DESCRIPTION

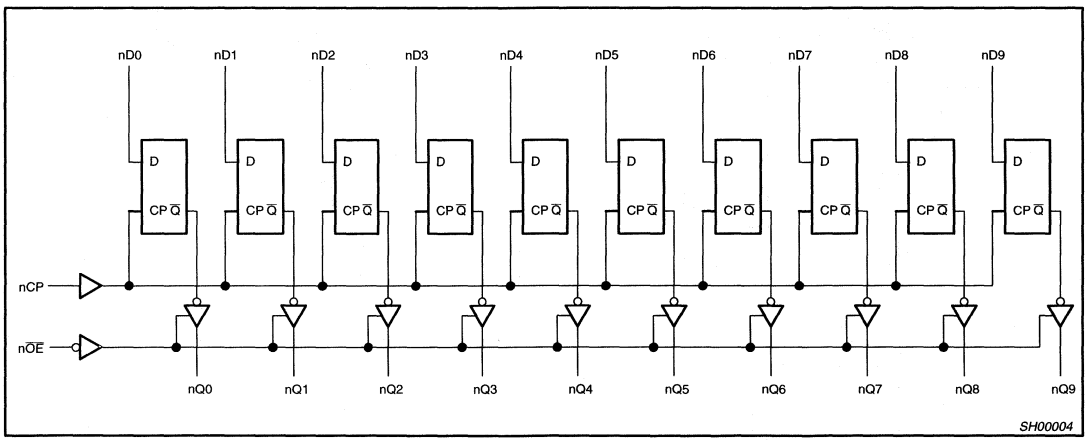
PIN NUMBER	SYMBOL	FUNCTION
56, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 - 1D9 2D0 - 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 - 1Q9 2Q0 - 2Q9	Data outputs
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx		nQ0 - nQ9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			5.1	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = –40 to +85°C V_{CC} = +3.3V MIN	TYP	MAX	UNIT
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	0.5 0.5	1.7 1.8	3.2 3.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.0 0.5	2.1 1.4	3.5 2.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.5 1.5	2.9 2.4	4.2 3.4	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = -40 to +85°C, V_{CC} = +3.3V ±0.3V		UNIT
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	2	1.5 1.5	0.1 0.1	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	2	0.5 0.5	0.1 0.1	ns
t_w(H) t_w(L)	nCP pulse width High or Low	1	1.5 1.5		ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.0 1.0	2.6 2.7	4.0 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.5 1.0	2.8 1.8	4.6 3.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.5 1.0	2.7 2.1	4.1 3.3	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

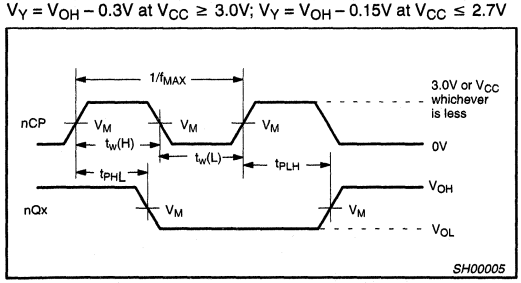
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5 ±0.2V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	2	1.5 2.0	0.1 0.5	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	2	0.3 0.5	−0.5 −0.1	ns
t_w(H) t_w(L)	nCP pulse width High or Low	1	1.5 1.5		ns

AC WAVEFORMS

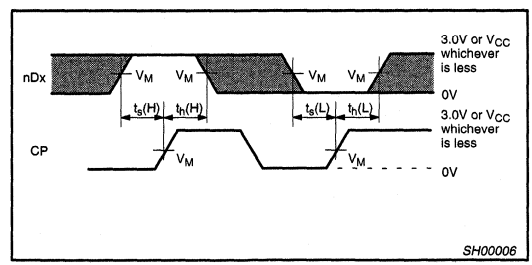
V_M = 1.5V at V_{CC} ≥ 3.0V; $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V

$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V; $V_X = V_{OL}$ + 0.15V at V_{CC} ≤ 2.7V

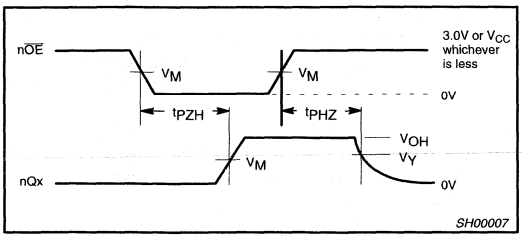
$V_Y = V_{OH}$ − 0.3V at V_{CC} ≥ 3.0V; $V_Y = V_{OH}$ − 0.15V at V_{CC} ≤ 2.7V



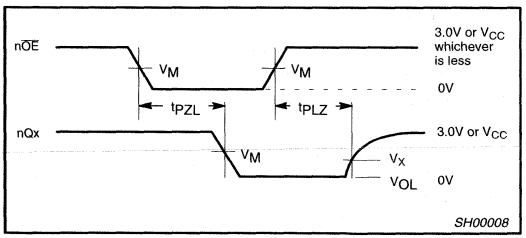
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock frequency



Waveform 2. Data Setup and Hold Times

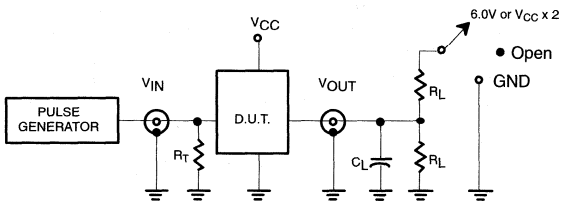


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

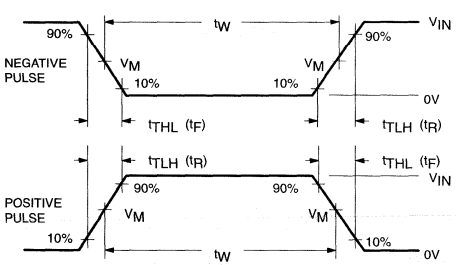


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤2.5ns	≤2.5ns

SW00025

2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with 30Ω termination resistors (3-State)

74ALVT162821

FEATURES

- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- 20-bit positive-edge triggered register
- 5V I/O Compatible
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Output capability +12mA/-12mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT162821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT162821 has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($n\overline{OE}$) controls all ten 3-State buffers independent of the register operation. When $n\overline{OE}$ is Low, the data in the register appears at the outputs. When $n\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74ALVT162821 is designed with 30Ω series resistance in both High and Low output stages. This design reduces the line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters. The series termination resistors reduce overshoot and undershoot and are ideal for driving memory arrays.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nCP to nQ	C_L = 50pF	4.4 3.8	3.2 3.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	V_O = 0 or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

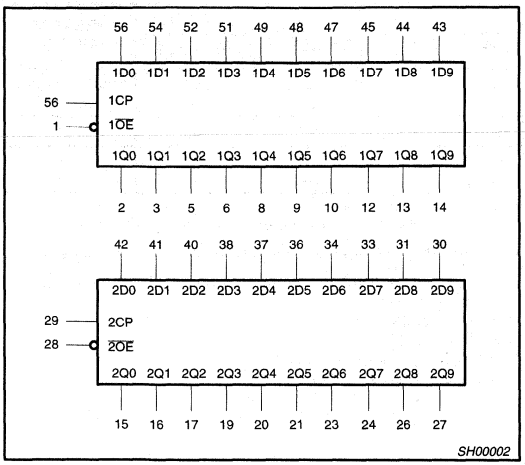
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162821 DL	AV162821 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162821 DGG	AV162821 DGG	SOT364-1

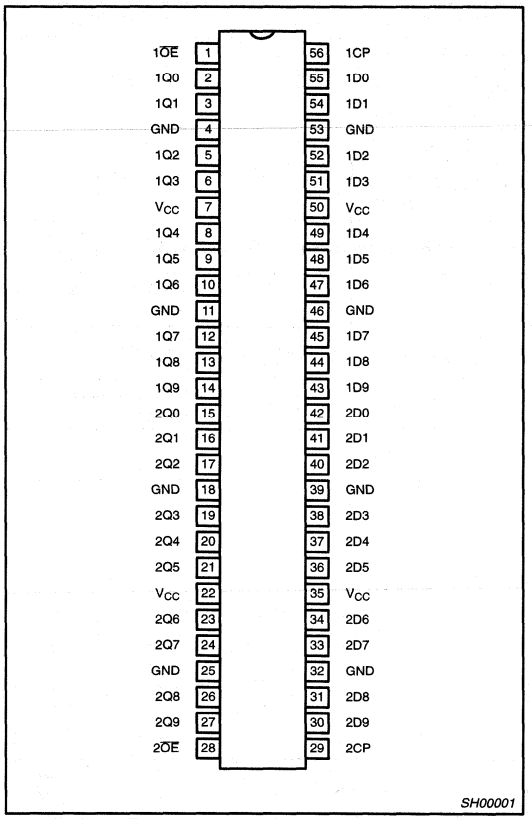
2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with 30Ω termination resistors (3-State)

74ALVT162821

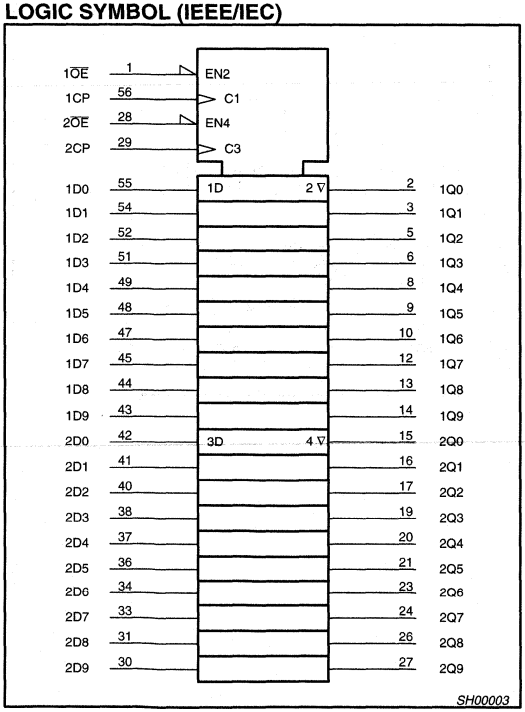
LOGIC SYMBOL



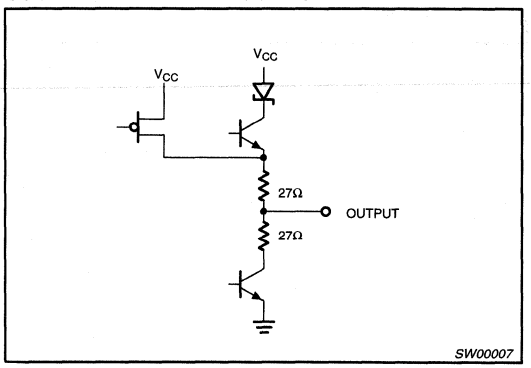
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



2.5V/3.3V 20-bit bus-interface D-type flip-flop; positive-edge trigger with 30Ω termination resistors (3-State)

74ALVT162821

PIN DESCRIPTION

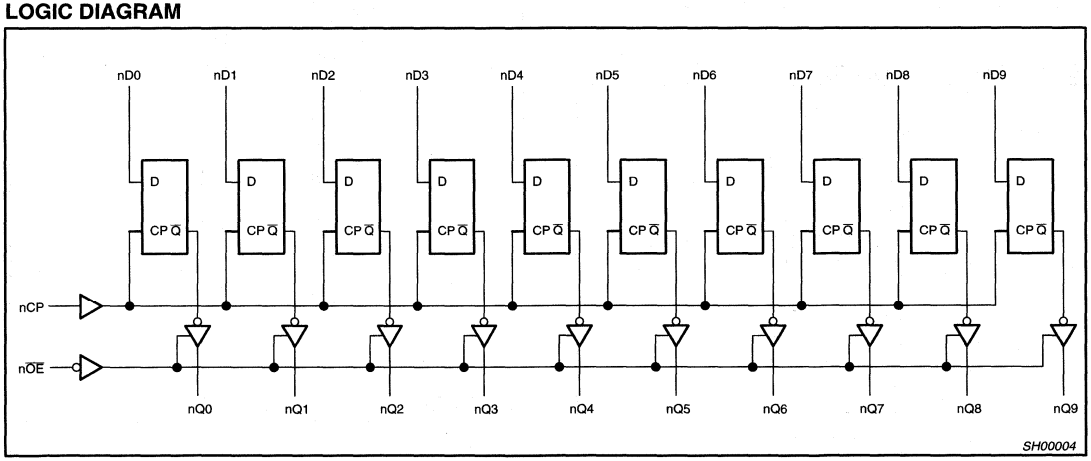
PIN NUMBER	SYMBOL	FUNCTION
56, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 - 1D9 2D0 - 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 - 1Q9 2Q0 - 2Q9	Data outputs
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx		nQ0 - nQ9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

				LIMITS			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = −18mA			−0.85	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = −100µA		V_{CC}−0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = −32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		−75	−140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	−5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			5.1	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}−0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = −40 to +85°C, V_{CC} = +3.3V			UNIT
			MIN	TYP	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH}	Propagation delay nCP to nQx	1	1.0	3.2	5.0	ns
t_{PHL}			1.0	3.2	4.7	
t_{PZH}	Output enable time to High and Low level	3	1.0	3.4	5.6	ns
t_{PZL}		4	0.5	2.3	3.7	
t_{PHZ}	Output disable time from High and Low level	3	1.5	3.7	5.4	ns
t_{PLZ}		4	1.5	3.0	4.3	

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			T_{amb} = -40 to +85°C V_{CC} = +3.3V ±0.3V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	1	1.5 1.5	0.1 0.1	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	2	0.5 0.5	0.1 0.1	ns
t_w(H) t_w(L)	nCP pulse width High or Low	2	1.5 1.5		ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/$\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.0 1.0	4.4 3.8	7.0 6.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.5 1.0	4.6 2.8	7.5 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.5 1.0	3.5 3.7	5.5 5.7	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

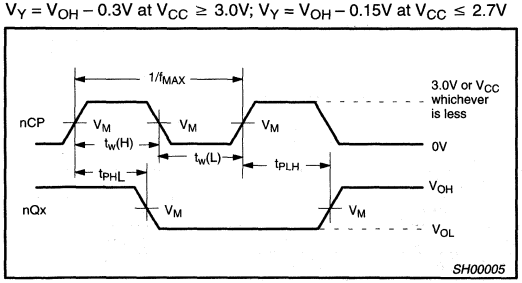
AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

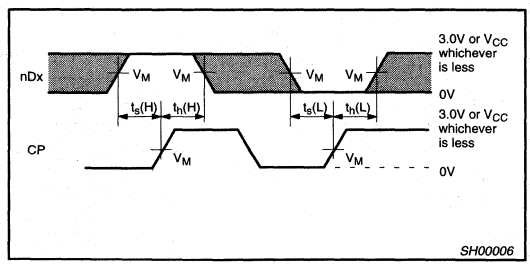
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5 ±0.2V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	1	1.5 2.0	0.1 0.5	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	2	0.3 0.5	–0.5 –0.1	ns
t_w(H) t_w(L)	nCP pulse width High or Low	2	1.5 1.5		ns

AC WAVEFORMS

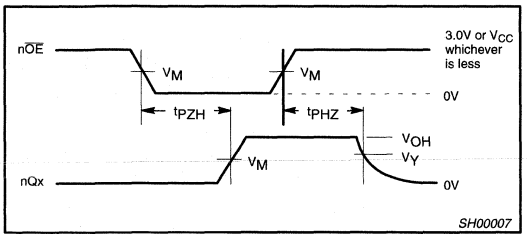
V_M = 1.5V at V_{CC} ≥ 3.0V; $V_M = V_{CC}/2$ at V_{CC} ≤ 2.7V
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 3.0V; $V_X = V_{OL}$ + 0.15V at V_{CC} ≤ 2.7V
$V_Y = V_{OH}$ – 0.3V at V_{CC} ≥ 3.0V; $V_Y = V_{OH}$ – 0.15V at V_{CC} ≤ 2.7V



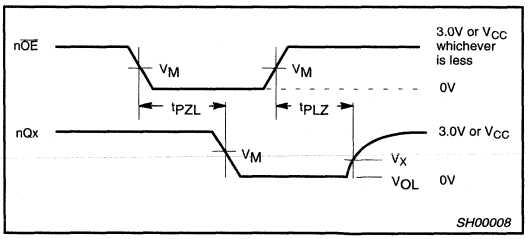
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock frequency



Waveform 2. Data Setup and Hold Times

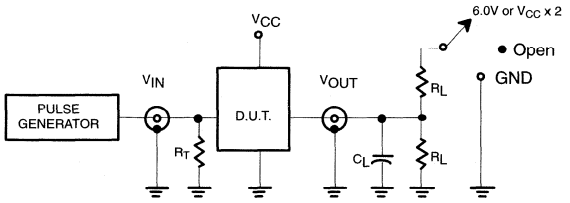


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

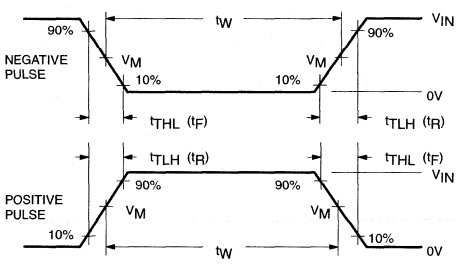


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ALVT16823

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- 5V I/O Compatible
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT16823 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ALVT16823 has two 9-bit wide buffered registers with Clock Enable ($n\overline{CE}$) and Master Reset ($n\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF			ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	$V_{I/O}$ = 0V or 3.0V	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16823 DL	AV16823 DL	SOT371–1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16823 DGG	AV16823 DGG	SOT364–1

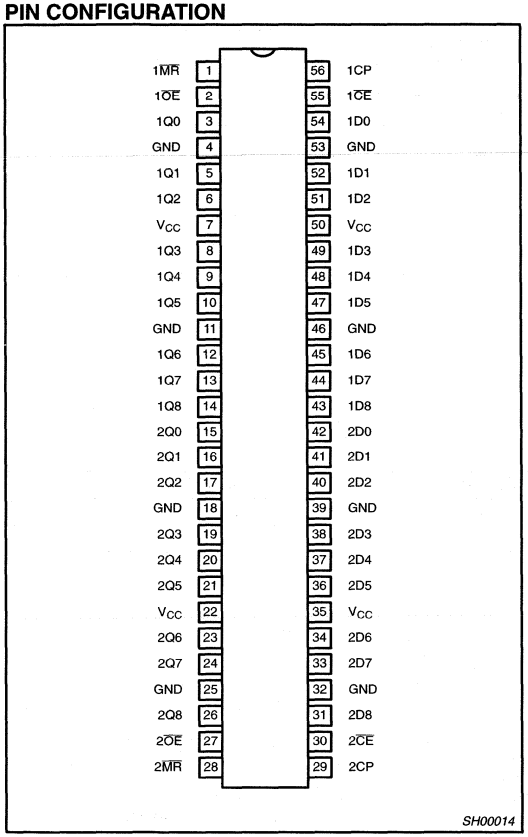
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active-Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active-Low)
1, 28	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

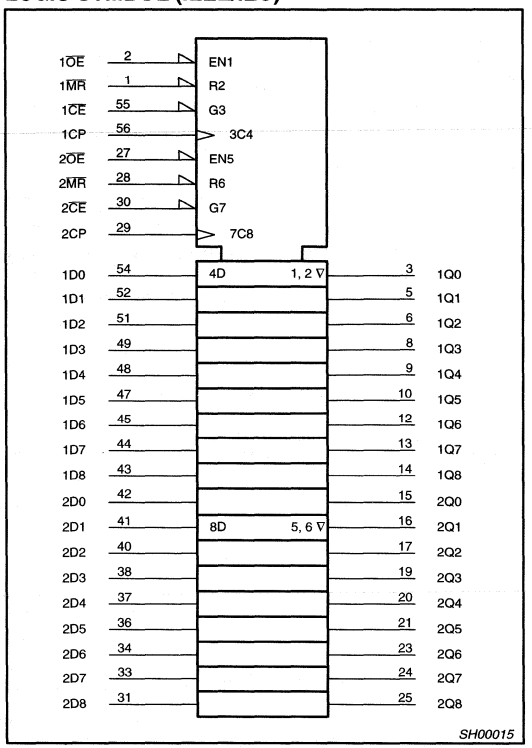
2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ALVT16823

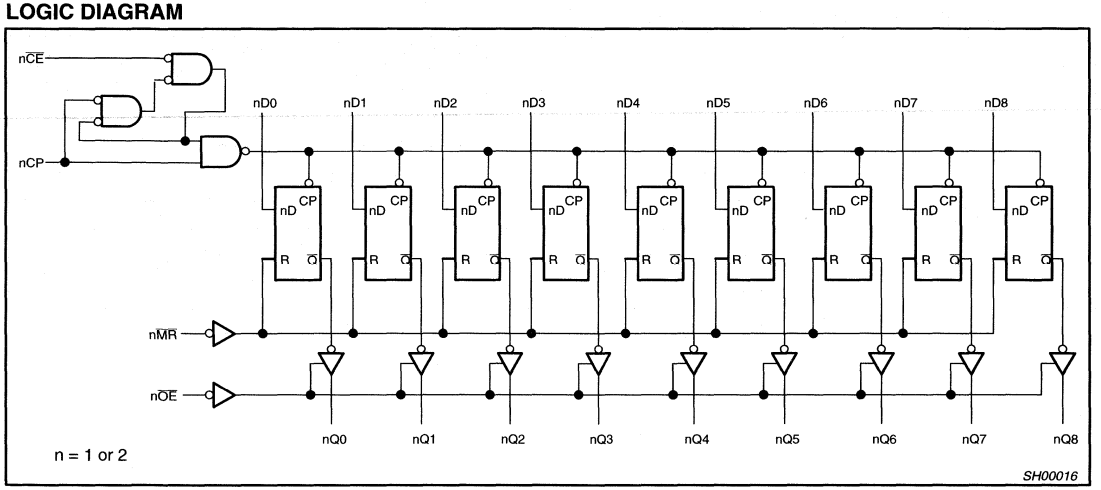
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$n\overline{OE}$	$n\overline{MR}$	$n\overline{CE}$	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.9	5.5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +3.3V			T_{amb} = −40°C to +85°C V_{CC} = +3.3V ±0.3V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1						MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1						ns
t_{PHL}	Propagation delay n$\overline{MR}$ to nQx	2						ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5						ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5						ns

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C V_{CC} = +3.3V ±0.3V			
			MIN	TYP	MAX	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	3				ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	3				ns
t_w(H) t_w(L)	nCP pulse width High or Low	1				ns
t_s(H) t_s(L)	Setup time, High or Low n$\overline{CE}$ to nCP	3				ns
t_h(H) t_h(L)	Hold time, High or Low n$\overline{CE}$ to nCP	3				ns
t_w(L)	n$\overline{MR}$ pulse width, Low	2				ns
t_{rec}	Recovery time n$\overline{MR}$ to nCP	2				ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.5		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			10		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.7	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +2.5V			T_{amb} = −40°C to +85°C V_{CC} = +2.5V ±0.2V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1						MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1						ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQx	2						ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5						ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5						ns

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

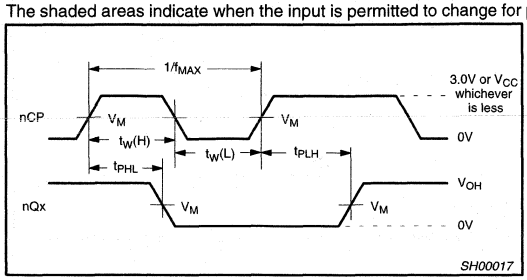
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nCP	3				ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	3				ns
$t_w(H)$ $t_w(L)$	nCP pulse width High or Low	1				ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $n\overline{CE}$ to nCP	3				ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $n\overline{CE}$ to nCP	3				ns
$t_w(L)$	$n\overline{MR}$ pulse width, Low	2				ns
t_{rec}	Recovery time $n\overline{MR}$ to nCP	2				ns

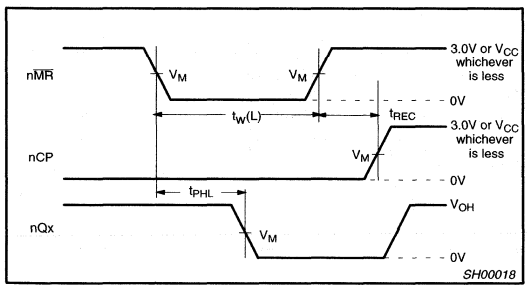
AC WAVEFORMS

For all waveforms, V_M = 1.5V or $V_{CC}/2$ whichever is less

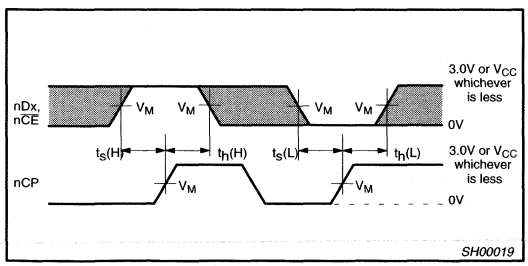
The shaded areas indicate when the input is permitted to change for predictable output performance.



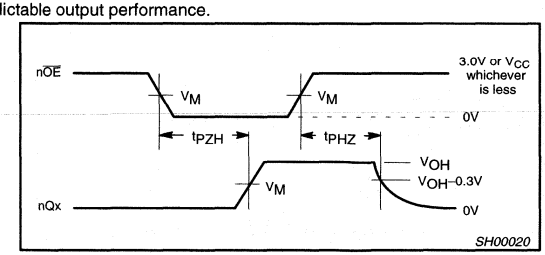
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



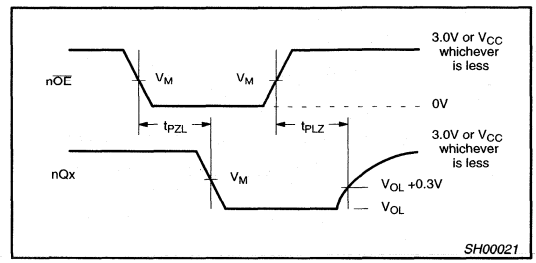
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Setup and Hold Times

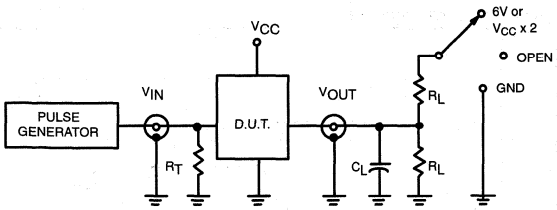


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

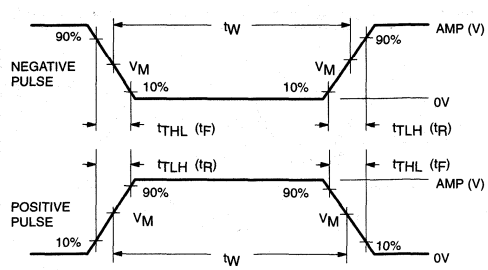


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

74ALVT162823

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- 5V I/O Compatible
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Outputs include series resistance of 30Ω making external termination resistors unnecessary

DESCRIPTION

The 74ALVT162823 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ALVT162823 has two 9-bit wide buffered registers with Clock Enable ($n\overline{CE}$) and Master Reset ($n\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 74ALVT162823 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF	2.8	2.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	$V_{I/O}$ = 0V or 3.0V	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162823 DL	AV162823 DL	SOT371–1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162823 DGG	AV162823 DGG	SOT364–1

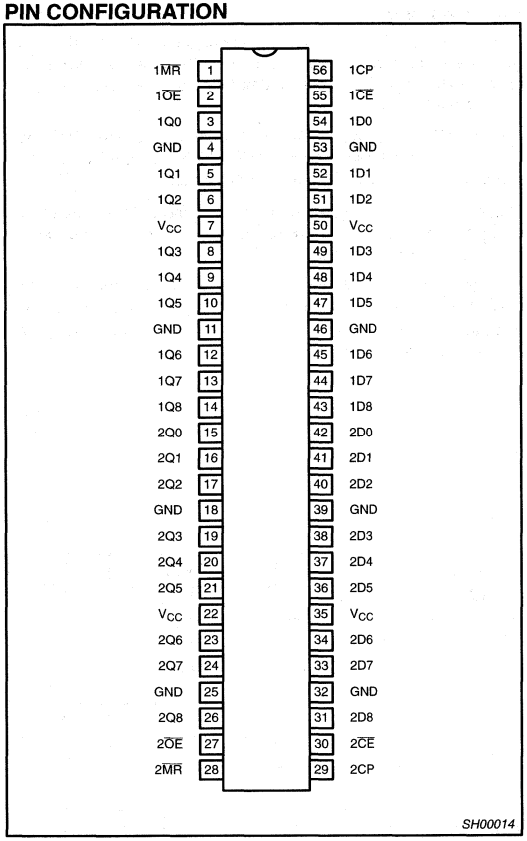
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active-Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active-Low)
1, 28	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

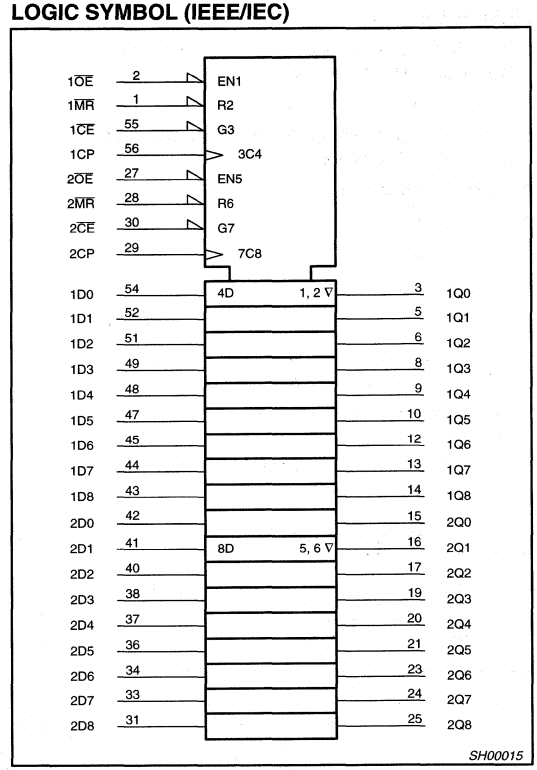
2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

74ALVT162823

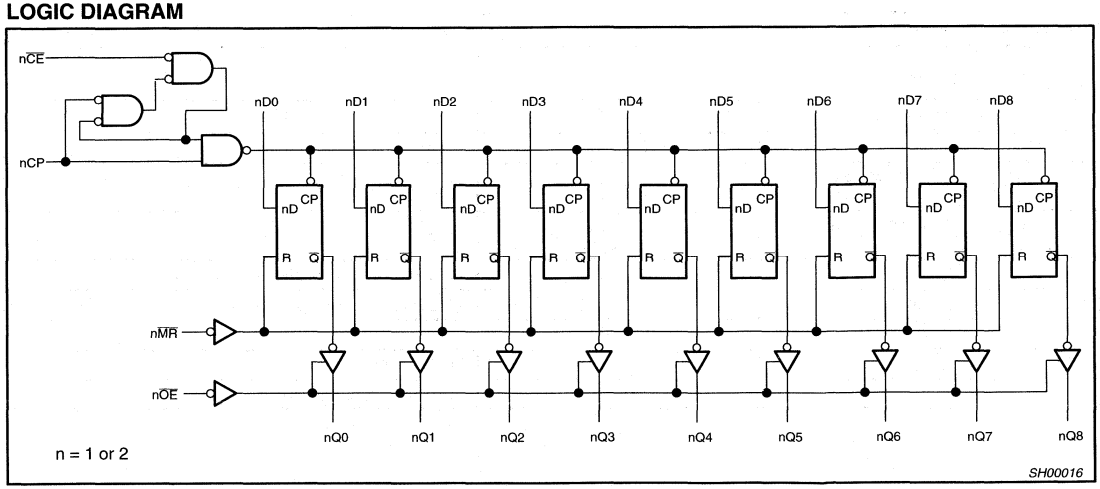
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM

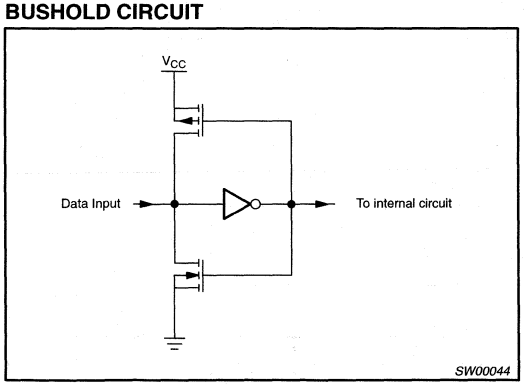


FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$n\overline{OE}$	$n\overline{MR}$	$n\overline{CE}$	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↕	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↕ = Not a Low-to-High clock transition

BUSHOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current D inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.9	5.5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = –40°C to +85°C V_{CC} = +3.3V ±0.3V			
			MIN	TYP	MAX	
f_{MAX}	Maximum clock frequency	1				MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.8 1.9		3.3 3.1	ns
t_{PHL}	Propagation delay n$\overline{MR}$ to nQx	2	1.6		3.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.6 2.0		3.6 4.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	2.2 1.9		3.8 2.9	ns

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			T_{amb} = -40 to +85°C V_{CC} = +3.3V ±0.3V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	3	0.4 0.4	0.7 1.1	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	3			ns
t_w(H) t_w(L)	nCP pulse width High or Low	1			ns
t_s(H) t_s(L)	Setup time, High or Low n$\overline{CE}$ to nCP	3	–0.2 –0.8	0.2 –0.2	ns
t_h(H) t_h(L)	Hold time, High or Low n$\overline{CE}$ to nCP	3			ns
t_w(L)	n$\overline{MR}$ pulse width, Low	2			ns
t_{rec}	Recovery time n$\overline{MR}$ to nCP	2	0.7	1.1	ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.7	2.5		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = GND	Control pins		0.1	±1	µA
		V_{CC} = 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current D inputs[6]	V_{CC} = 2.5V; V_I = 0.7V			90		µA
		V_{CC} = 2.5V; V_I = 1.7V			–10		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.5V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.7	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = –40°C to +85°C V_{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
f_{MAX}	Maximum clock frequency	1				MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	2.0 2.1		5.0 4.7	ns
t_{PHL}	Propagation delay n$\overline{MR}$ to nQx	2	2.1		5.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	2.3 2.7		6.4 6.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	2.7 2.3		5.2 4.2	ns

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

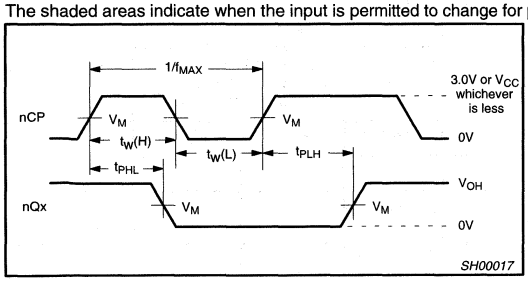
GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time, High or Low nDx to nCP	3	0.5 0.9	0.8 1.5	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nCP	3			ns
t_w(H) t_w(L)	nCP pulse width High or Low	1			ns
t_s(H) t_s(L)	Setup time, High or Low n$\overline{CE}$ to nCP	3	–1.7 –0.3	0.2 0.1	ns
t_h(H) t_h(L)	Hold time, High or Low n$\overline{CE}$ to nCP	3			ns
t_w(L)	n$\overline{MR}$ pulse width, Low	2			ns
t_{rec}	Recovery time n$\overline{MR}$ to nCP	2	0.8	1.4	ns

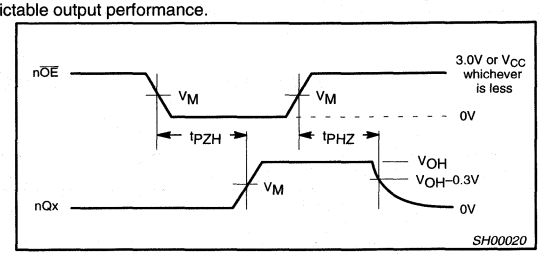
AC WAVEFORMS

For all waveforms, V_M = 1.5V or $V_{CC}/2$ whichever is less

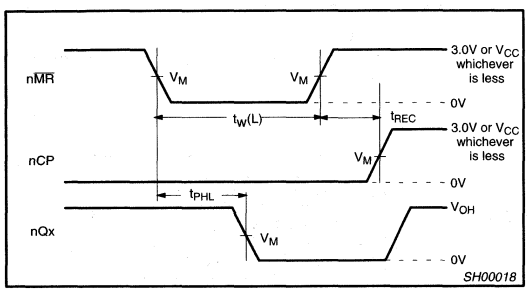
The shaded areas indicate when the input is permitted to change for predictable output performance.



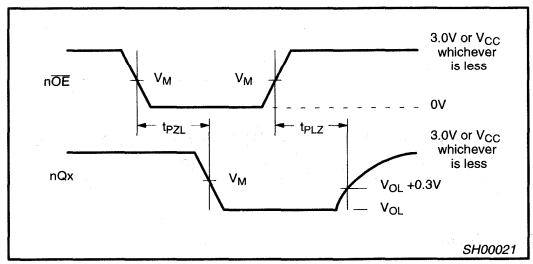
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



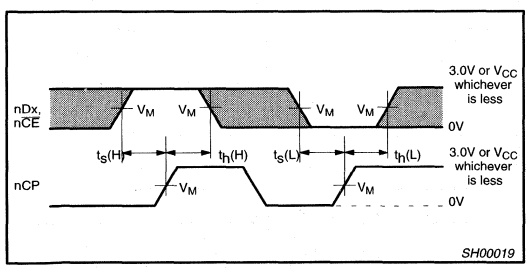
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

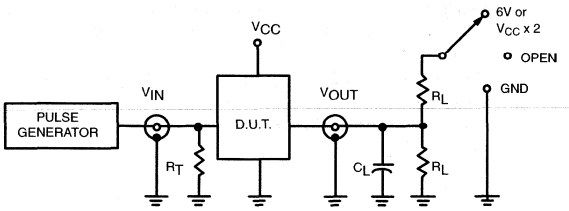


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

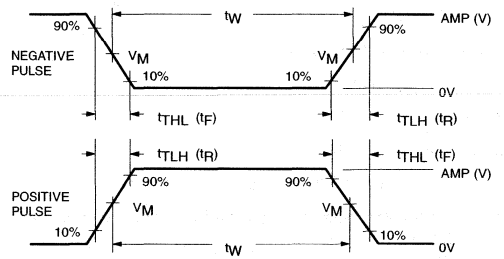


Waveform 3. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC} / 2, whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00162

2.5V/3.3V 20-bit buffer/line driver, non-inverting (3-State)

74ALVT16827

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- 5V I/O Compatible
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT16827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT16827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF	1.7 1.8	1.3 1.3	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16827 DL	AV16827 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16827 DGG	AV16827 DGG	SOT364-1

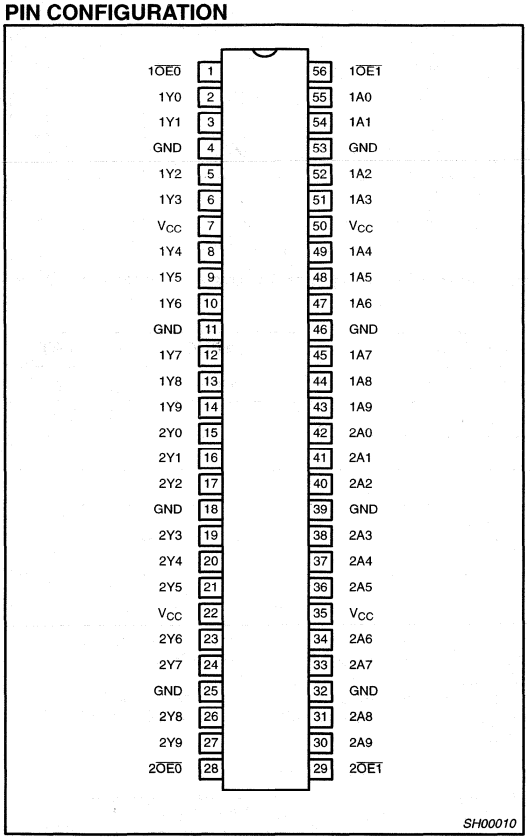
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 - 1A9 2A0 - 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 - 1Y9 2Y0 - 2Y9	Data outputs
1, 56, 28, 29	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

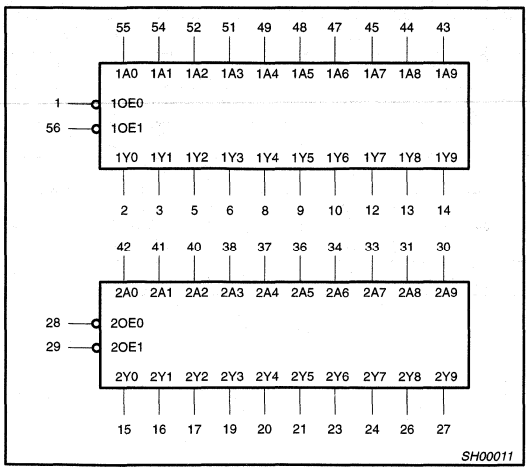
2.5V/3.3V 20-bit buffer/line driver, non-inverting (3-State)

74ALVT16827

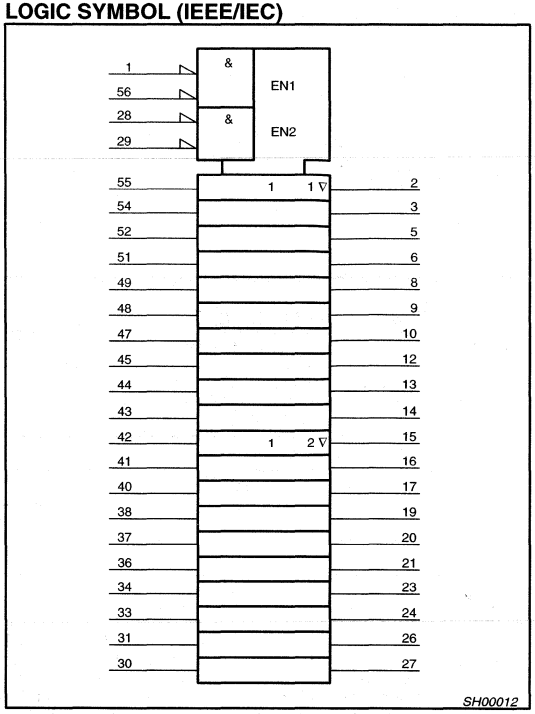
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

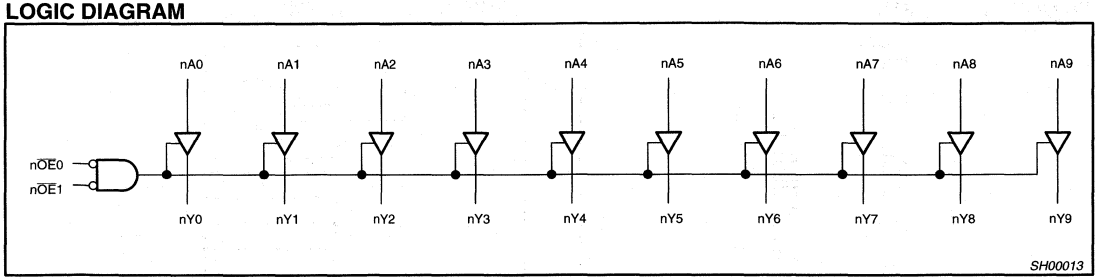


FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$n\overline{OE}x$	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = High voltage level
L = Low voltage level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.2	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = -40 to +85°C V_{CC} = +3.3V ±0.3V MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	1.3 1.3	2.3 2.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 0.5	2.2 1.6	3.8 2.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.0 1.0	3.2 2.5	4.8 3.8	ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 2.7V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.47	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	± 100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.5V; V_I = 0.8V			115		µA
		V_{CC} = 2.5V; V_I = 2.0V			–10		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.6	5.0	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

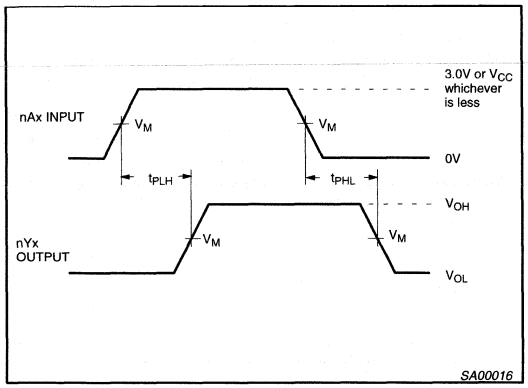
AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

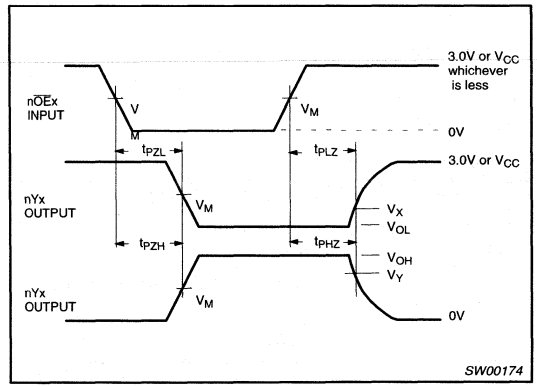
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	1.7 1.8	2.9 3.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.1 2.1	5.5 4.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.0 1.0	3.1 2.3	5.1 3.9	ns

AC WAVEFORMS

V_M = 1.5V for V_{CC} ≥ 3.0V; V_M = V_{CC}/2 for V_{CC} ≤ 2.7V
V_X = V_{OL} + 0.3V for V_{CC} ≥ 3.0V; V_X = V_{OL} + 0.15V for V_{CC} ≤ 2.7V
V_Y = V_{OH} − 0.3V for V_{CC} ≥ 3.0V; V_Y = V_{OH} − 0.15V for V_{CC} ≤ 2.7V

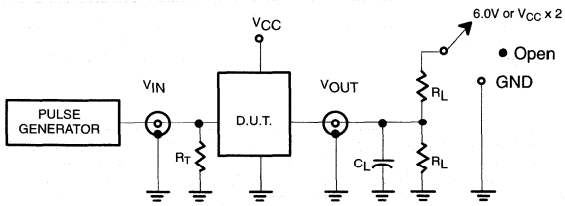


Waveform 1. The Input (nAx) to Output (nYx) Propagation Delays

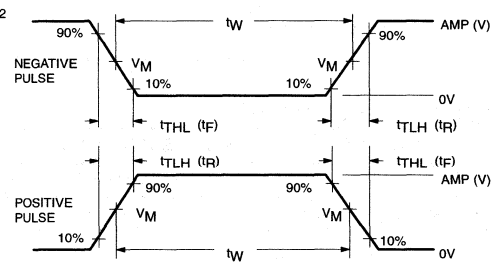


Waveform 2. The 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC *CHARACTERISTICS for value.*

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00205

2.5V/3.3V 20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

74ALVT162827

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- 5V I/O Compatible
- Live insertion/extraction permitted
- 3-State output buffers
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- Output capability: +12mA/–12mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT162827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT162827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

The 74ALVT162827 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF	2.7 2.3	2.2 2.0	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162827 DL	AV162827 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162827 DGG	AV162827 DGG	SOT364-1

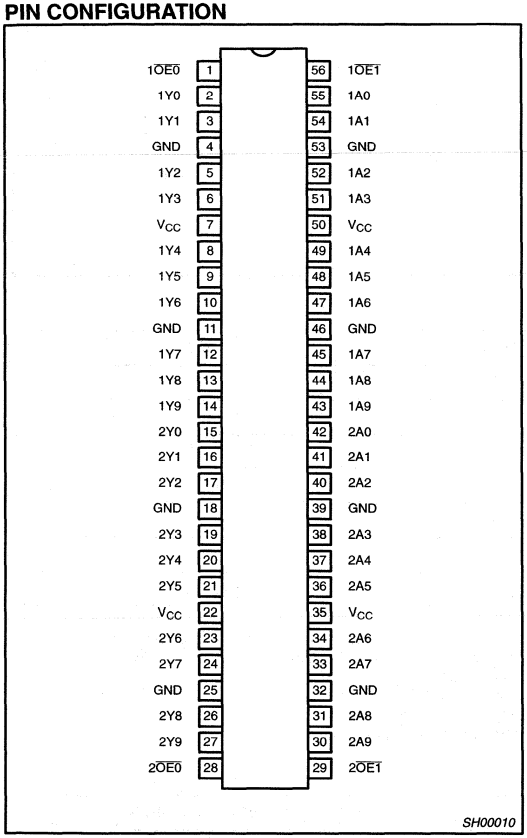
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 - 1A9 2A0 - 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 - 1Y9 2Y0 - 2Y9	Data outputs
1, 56, 28, 29	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

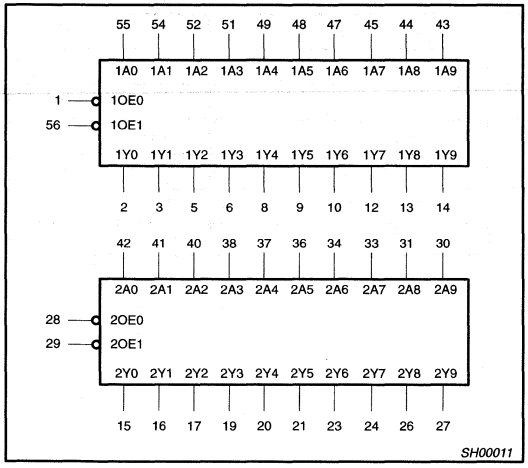
2.5V/3.3V 20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

74ALVT162827

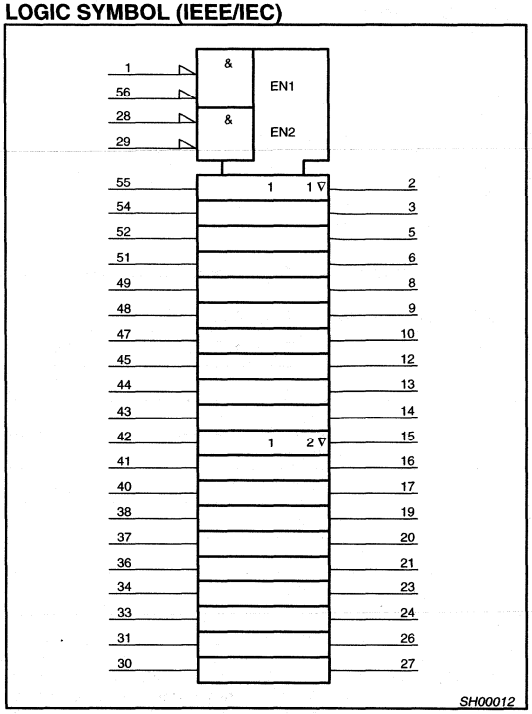
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

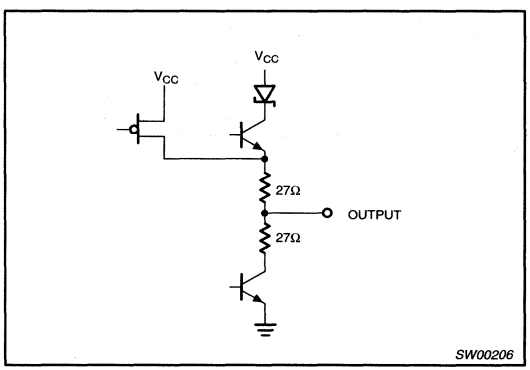


FUNCTION TABLE

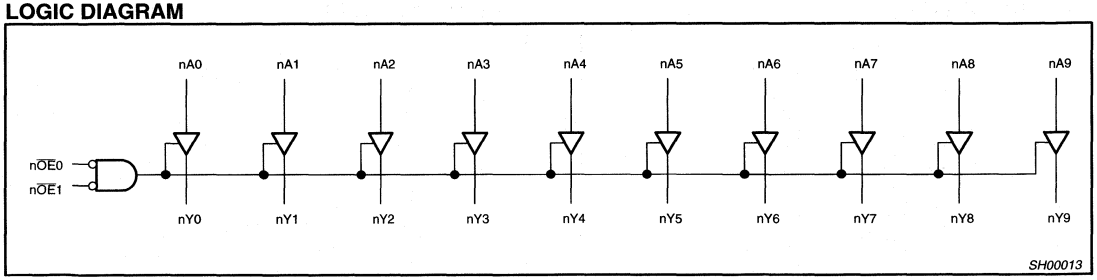
INPUTS		OUTPUTS	OPERATING MODE
$n\overline{OE}x$	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = High voltage level
L = Low voltage level

SCHEMATIC OF EACH OUTPUT



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0	2.3		V
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA			0.5	0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		µA
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.9	5.5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = -40 to +85°C V_{CC} = +3.3V ±0.3V MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	2.2 2.0	3.3 3.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.0	3.4 2.4	5.6 3.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.0	3.4 2.7	5.2 4.5	ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3V; I_{OH} = –8mA		1.7	2.3		V
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 12mA			0.5	0.7	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			115		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	5.0	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

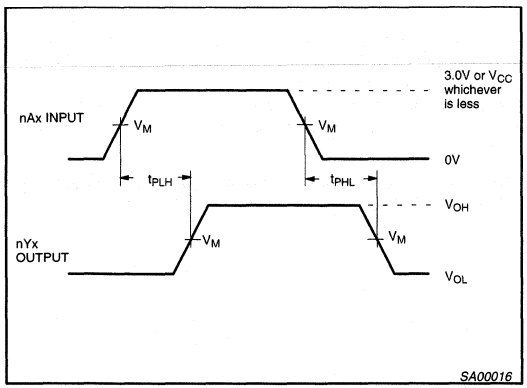
AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

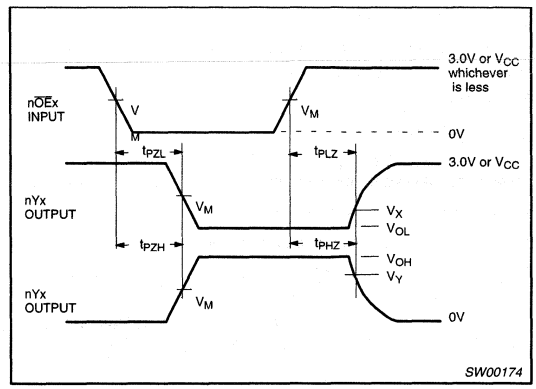
SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.5 1.5	2.7 2.3	4.5 3.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	2.5 1.5	4.7 2.9	7.5 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.0	3.2 2.4	5.2 4.0	ns

AC WAVEFORMS

V_M = 1.5V for V_{CC} ≥ 3.0V; V_M = V_{CC}/2 for V_{CC} ≤ 2.7V
V_X = V_{OL} + 0.3V for V_{CC} ≥ 3.0V; V_X = V_{OL} + 0.15V for V_{CC} ≤ 2.7V
V_Y = V_{OH} − 0.3V for V_{CC} ≥ 3.0V; V_Y = V_{OH} − 0.15V for V_{CC} ≤ 2.7V

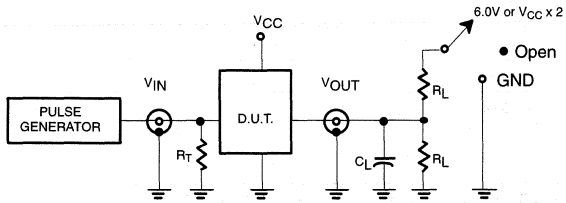


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

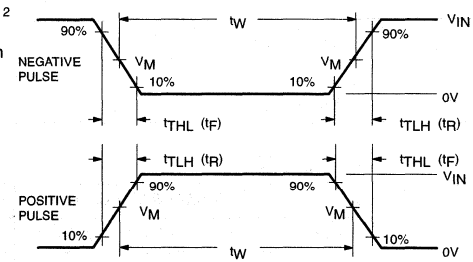


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V or V_{CC}/2 whichever is less
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

2.5V/3.3V 20-bit bus interface latch (3-State) 74ALVT16841

FEATURES

- High speed parallel latches
- 5V I/O Compatible
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16841 Bus interface latch is designed to provide extra data width for wider data/address paths of buses carrying parity. It is designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility to 5V.

The 74ALVT16841 consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($n\overline{OE}$) is Low. When $n\overline{OE}$ is High the output is in the High-impedance state.

QUICK REFERENCE DATA

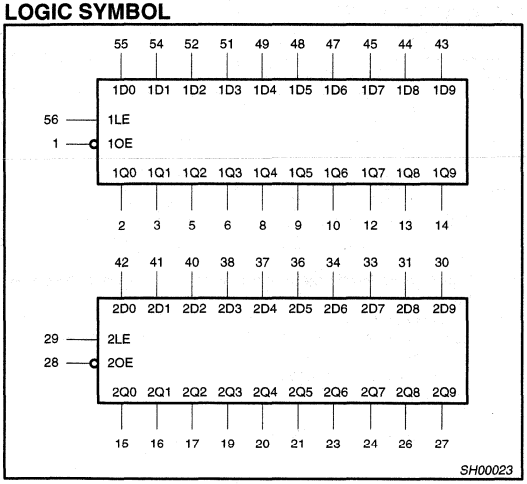
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF	1.8 2.1	1.5 1.7	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	3	3	pF
C_{Out}	Output pin capacitance	$V_{I/O}$ = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

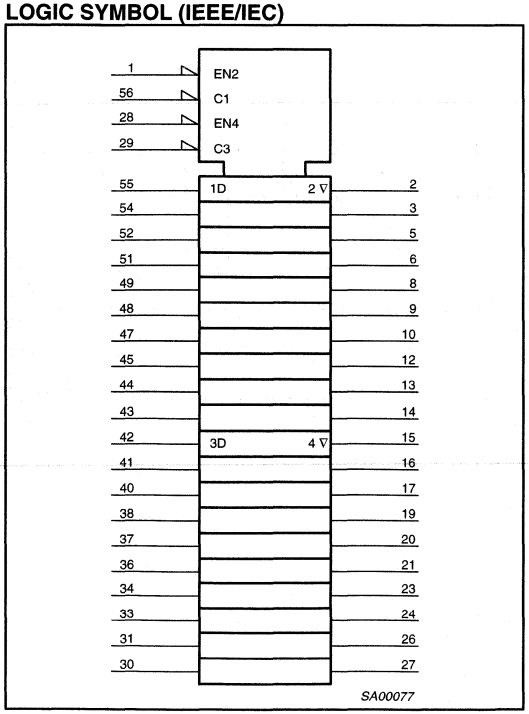
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16841 DL	AV16841 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16841 DGG	AV16841 DGG	SOT364-1

2.5V/3.3V 20-bit bus interface latch (3-State) 74ALVT16841

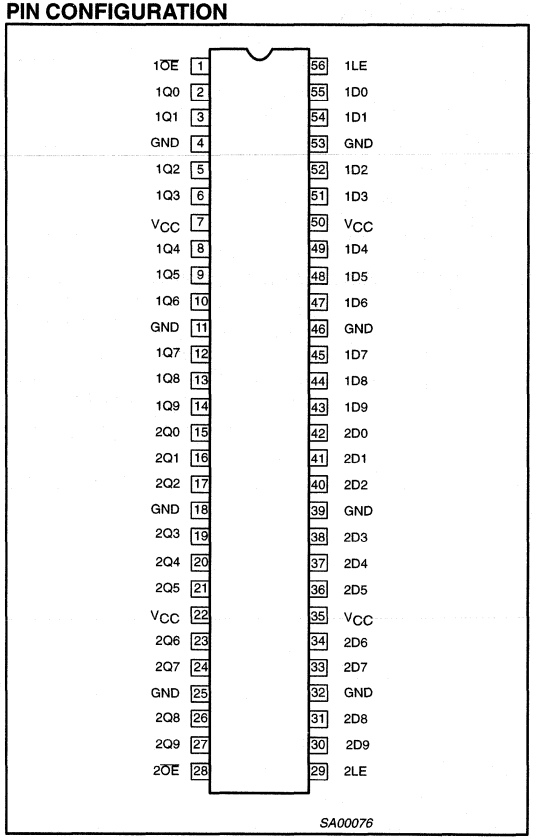
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

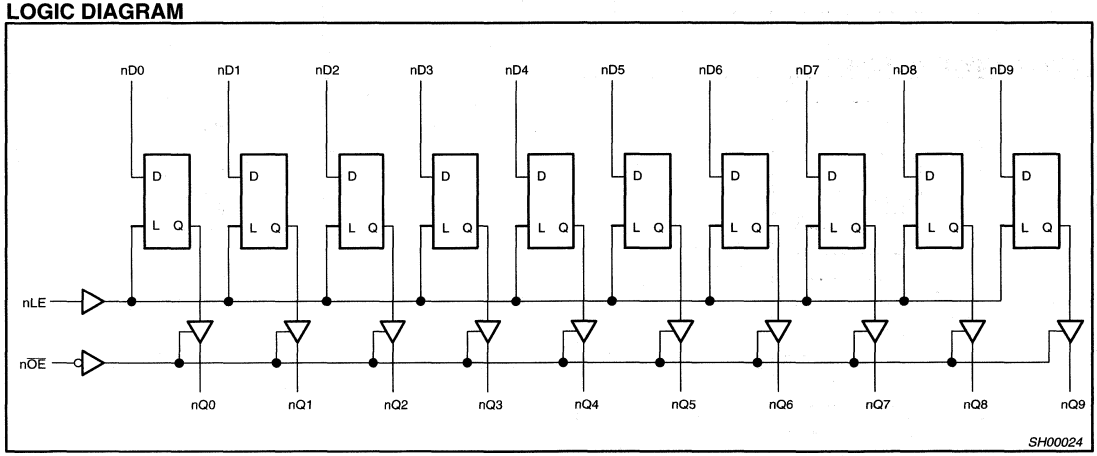
PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 – 1D9 2D0 – 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
56, 29	1LE, 2LE	Latch enable inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$n\overline{OE}$	nLE	nDx	nQ0 – nQ9	
L L	H H	L H	L H	Transparent
L L	↓ ↓	l h	L H	Latched
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
↓ = High-to-Low LE transition
NC= No change
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.2	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C V_{CC} = +3.3V ±0.3V			
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	0.5 0.5	1.5 1.7	2.5 2.7	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.0 1.5	2.1 3.4	3.2 5.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.0 0.5	2.3 1.3	3.6 2.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.5 1.5	3.2 2.8	4.9 4.3	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			T_{amb} = -40 to +85°C V_{CC} = +3.3V ±0.3V		
			Min	Typ	
t_s(H) t_s(L)	Setup time, High or Low nDx to nLE	3	1.0 1.0	0 0	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nLE	3	1.2 1.2	0.1 0.3	ns
t_w(H)	nLE pulse width High	1	1.5		ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	± 100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	± 100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.3	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	0.5 0.5	1.8 2.1	3.0 3.6	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQx	1	1.0 2.0	2.7 4.2	4.3 6.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.5 0.5	3.0 1.8	4.0 3.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	1.5 1.0	3.1 2.4	4.5 3.8	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

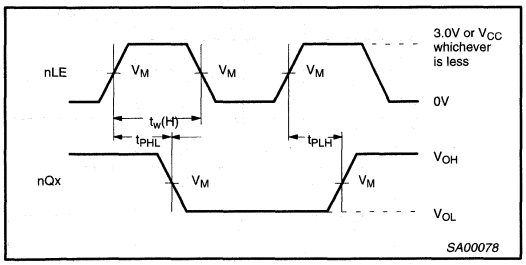
AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

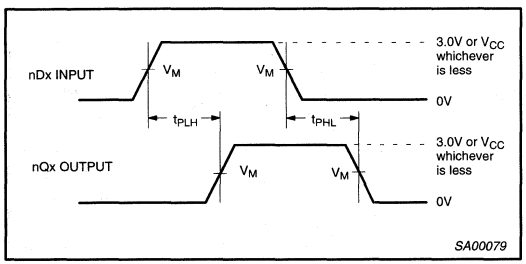
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			T_{amb} = -40 to +85°C V_{CC} = +2.5V ±0.2V		
			Min	Typ	
t_s(H) t_s(L)	Setup time, High or Low nDx to nLE	3	0.5 1.5	0 0.2	ns
t_h(H) t_h(L)	Hold time, High or Low nDx to nLE	3	1.8 2.0	0 0.8	ns
t_w(H)	nLE pulse width High	1	1.5		ns

AC WAVEFORMS

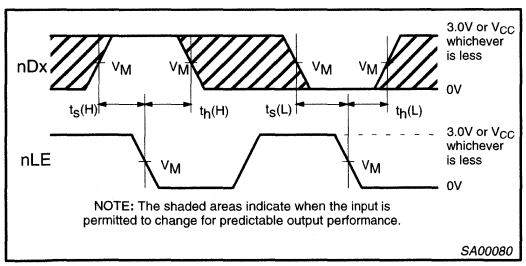
V_M = 1.5V at V_{CC} ≥ 3.0V; V_M = V_{CC}/2 at V_{CC} ≤ 2.7V
V_X = V_{OL} + 0.3V at V_{CC} ≥ 3.0V; V_X = V_{OL} + 0.15V at V_{CC} ≤ 2.7V
V_Y = V_{OH} − 0.3V at V_{CC} ≥ 3.0V; V_Y = V_{OH} − 0.15V at V_{CC} ≤ 2.7V



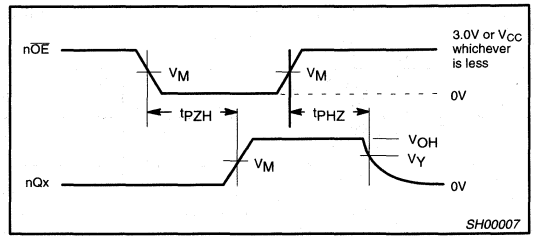
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



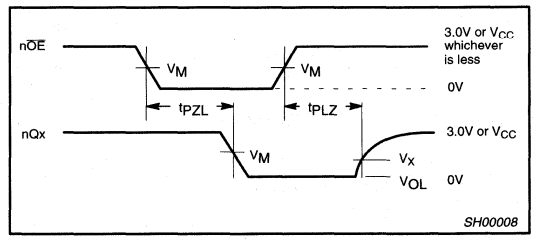
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

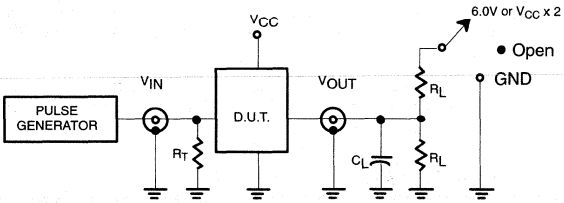


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

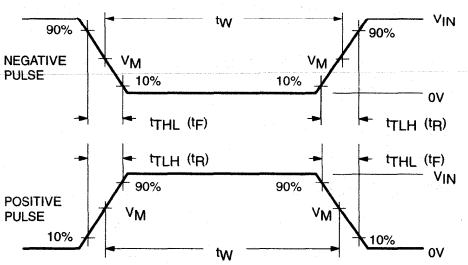


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

2.5V/3.3V 16-bit latch transceiver with 8-bit parity generator/checker (3-State)

74ALVT16899

FEATURES

- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/$\overline{\text{EVEN}}$ parity
- Continuously checks parity of both A bus and B bus latches as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$
- Open-collector $\overline{\text{ERR}}$ output
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data
- Output capability: +64 mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up 3-State
- Power-up reset
- No bus current loading when output if tied to 5 V bus
- Live insertion/extraction permitted
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT16899 is a 16-bit to 16-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the $\overline{\text{SEL}}$ input.

The 74ALVT16899 features independent latch enables for the A and B bus latches, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION:

The 74ALVT16899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEA and LEB are High and the Mode Select ($\overline{\text{SEL}}$) is Low, the parity generated from A0-A7 and B0-B7 can be checked and monitored by $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$. (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:
Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is High. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ and can be used as an interrupt to signal a data/parity bit error to the CPU.

Latched input, Generate/Feed-through parity, Check A (and B) bus parity:
Independent latch enables (LEA and LEB) allow other permutations of:

- Transparent latch / 1 bus latched / both buses latched
- Feed-through parity / generate parity
- Check in bus parity / check out bus parity / check in and out bus parity

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5 V	3.3 V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF			ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{\text{ERRA}}$	C_L = 50pF			ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
$C_{I/O}$	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	9	9	pF
I_{CCZ}	Quiescent supply current	Outputs disabled	40	70	µA

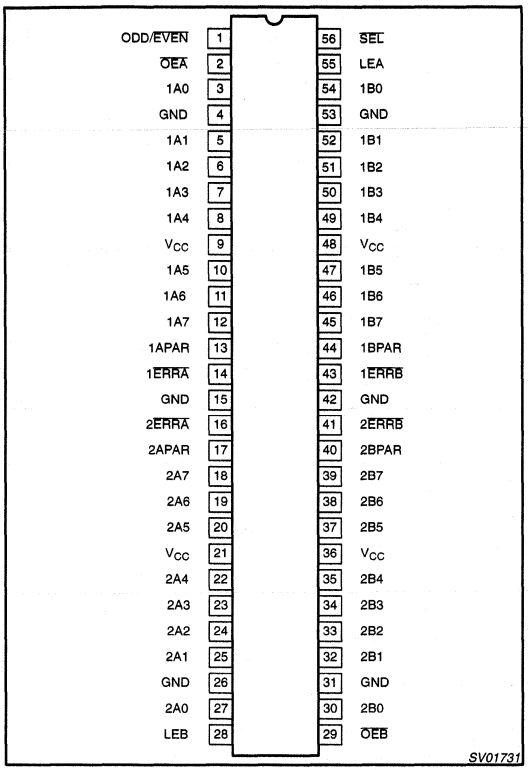
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16899	AV16899 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16899 DGG	AV16899 DGG	SOT364-1

2.5V/3.3V 16-bit latch transceiver with 8-bit parity generator/checker (3-State)

74ALVT16899

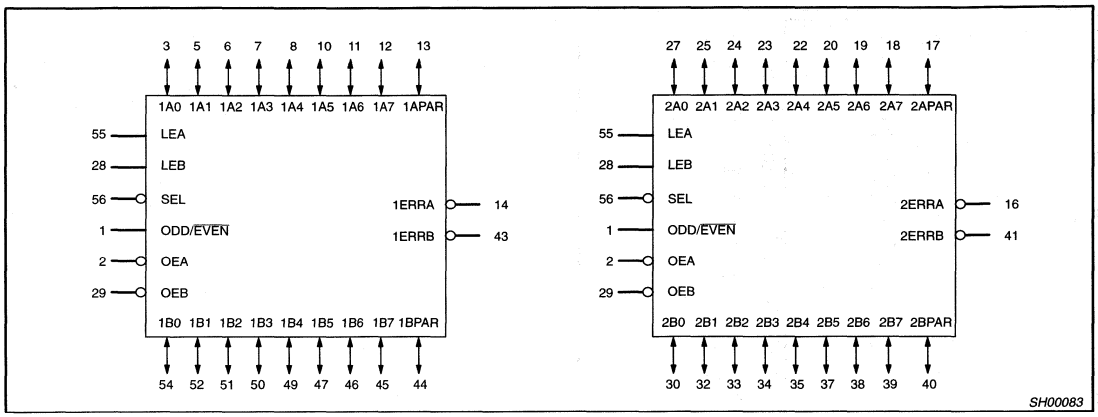
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1A0 - 1A7 2A0 - 2A7	3, 5, 6, 7, 8, 10, 11, 12 27, 25, 24, 23, 22, 20, 19, 18	Latched A bus 3-State inputs/outputs
1B0 - 1B7 2B0 - 2B7	54, 52, 51, 50, 49, 47, 46, 45 30, 32, 33, 34, 35, 37, 38, 39	Latched B bus 3-State inputs/outputs
1APAR 2APAR	13, 17	A bus parity 3-State input/output
1BPAR 2BPAR	44, 40	B bus parity 3-State input/output
ODD/$\overline{\text{EVEN}}$	1	Parity select input (Low for EVEN parity)
$\overline{\text{OEA}}$, $\overline{\text{OEB}}$	2, 29	Output enable inputs (gate A to B, B to A)
$\overline{\text{SEL}}$	56	Mode select input (Low for generate)
LEA, LEB	55, 28	Latch enable inputs (transparent High)
1$\overline{\text{ERRA}}$, 1$\overline{\text{ERRB}}$ 2$\overline{\text{ERRA}}$, 2$\overline{\text{ERRB}}$	14, 43, 16, 41	Error signal outputs (active-Low)
GND	4, 15, 26, 31, 42, 53	Ground (0V)
V_{CC}	9, 21, 36, 48	Positive supply voltage

LOGIC SYMBOL



PARITY AND ERROR FUNCTION TABLE

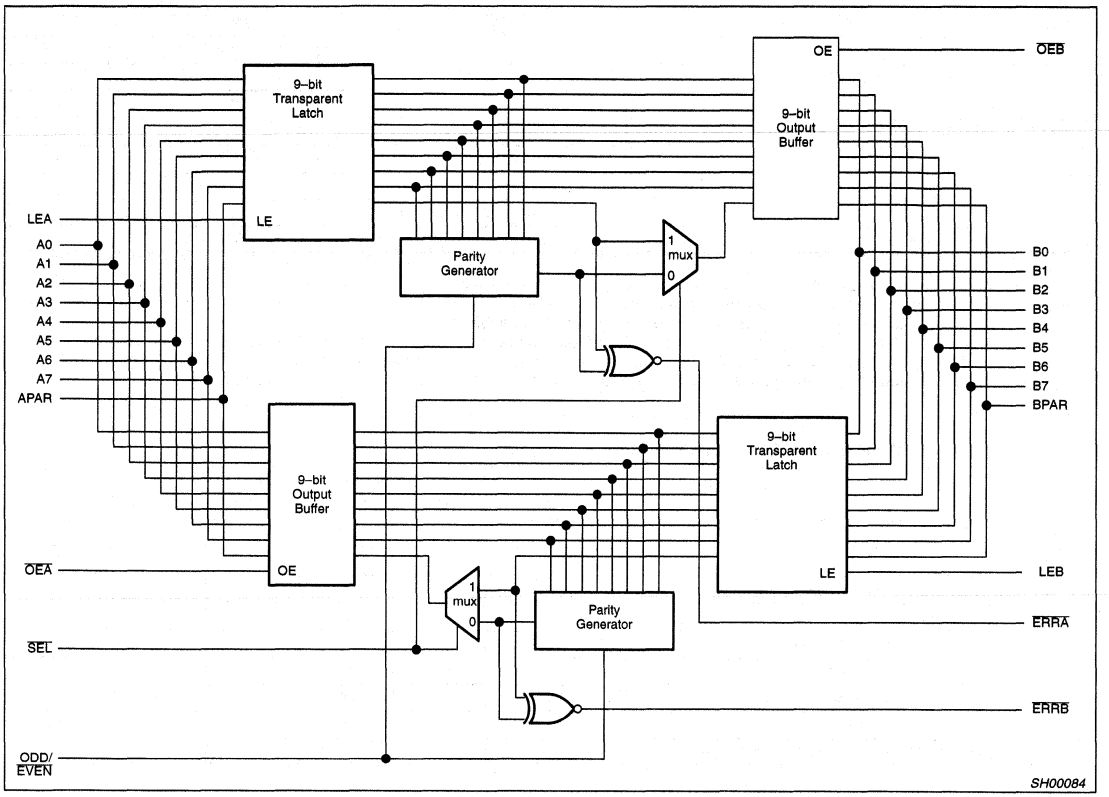
INPUTS				OUTPUTS			PARITY MODES	
$\overline{SEL}$	ODD/$\overline{EVEN}$	xPAR (A or B)	Σ of High Inputs	xPAR (B or A)	$\overline{ERRt}$	$\overline{ERRr}$*		
H	H	H	Even Odd	H H	H L	H L	Odd Mode	Feed-through/check parity
H	H	L	Even Odd	L L	L H	L H		
H	L	H	Even Odd	H H	L H	L H	Even Mode	
H	L	L	Even Odd	L L	H L	H L		
L	H	H	Even Odd	H L	H L	H H	Odd Mode	Generate parity
L	H	L	Even Odd	H L	L H	H H		
L	L	H	Even Odd	L H	L H	H H	Even Mode	
L	L	L	Even Odd	L H	H L	H H		

H = High voltage level
L = Low voltage level
t = Transmit–if the data path is from A→B then $\overline{ERRt}$ is $\overline{ERRA}$
r = Receive–if the data path is from A→B then $\overline{ERRr}$ is $\overline{ERRB}$
* Blocked if latch is not transparent

2.5V/3.3V 16-bit latch transceiver with 8-bit parity generator/checker (3-State)

74ALVT16899

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OEB}$	$\overline{OEA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	3-State A bus and B bus (input A & B simultaneously)
H	L	L	L	H	B → A, transparent B latch, generate parity from B0 - B7, check B bus parity
H	L	L	H	H	B → A, transparent A & B latch, generate parity from B0 - B7, check A & B bus parity
H	L	L	X	L	B → A, B bus latched, generate parity from latched B0 - B7 data, check B bus parity
H	L	H	X	H	B → A, transparent B latch, parity feed-through, check B bus parity
H	L	H	H	H	B → A, transparent A & B latch, parity feed-through, check A & B bus parity
L	H	L	H	X	A → B, transparent A latch, generate parity from A0 - A7, check A bus parity
L	H	L	H	H	A → B, transparent A & B latch, generate parity from A0 - A7, check A & B bus parity
L	H	L	L	X	A → B, A bus latched, generate parity from latched A0 - A7 data, check A bus parity
L	H	H	H	L	A → B, transparent A latch, parity feed-through, check A bus parity
L	H	H	H	H	A → B, transparent A & B latch, parity feed-through, check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0V			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.6	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1						ns
t_{PLH} t_{PHL}	Propagation delay An to BPAR or Bn to APAR	2						ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{ERRA}$ or Bn to $\overline{ERRB}$	3						ns
t_{PLH} t_{PHL}	Propagation delay APAR to BPAR or BPAR to APAR	1						ns
t_{PLH} t_{PHL}	Propagation delay APAR to $\overline{ERRA}$ or BPAR to $\overline{ERRB}$	6						ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to APAR or BPAR	5						ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$ or $\overline{ERRB}$	4						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to APAR or BPAR	8						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to $\overline{ERRA}$ or $\overline{ERRB}$	8						ns
t_{PLH} t_{PHL}	Propagation delay LEA to Bn or LEB to An	9						ns
t_{PLH} t_{PHL}	Propagation delay LEA to BPAR or LEB to APAR	9						ns
t_{PLH} t_{PHL}	Propagation delay LEA to $\overline{ERRA}$ or LEB to $\overline{ERRB}$	7						ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	11, 12						ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	11, 12						ns

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω		T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω	
			Min	Typ	Min	
t_s(H) t_s(L)	Setup time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10				ns
t_h(H) t_h(L)	Hold time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10				ns
t_w(H)	Pulse width, High LEA or LEB	10				ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.5		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA				0.4	
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}[6]	Bus Hold current Data inputs	V_{CC} = 2.3V; V_I = 0.8V			115		µA
		V_{CC} = 2.3V; V_I = 2.0V			10		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.5	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1						ns
t_{PLH} t_{PHL}	Propagation delay An to BPAR or Bn to APAR	2						ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{ERRA}$ or Bn to $\overline{ERRB}$	3						ns
t_{PLH} t_{PHL}	Propagation delay APAR to BPAR or BPAR to APAR	1						ns
t_{PLH} t_{PHL}	Propagation delay APAR to $\overline{ERRA}$ or BPAR to $\overline{ERRB}$	6						ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to APAR or BPAR	5						ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$ or $\overline{ERRB}$	4						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to APAR or BPAR	8						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SEL}$ to $\overline{ERRA}$ or $\overline{ERRB}$	8						ns
t_{PLH} t_{PHL}	Propagation delay LEA to Bn or LEB to An	9						ns
t_{PLH} t_{PHL}	Propagation delay LEA to BPAR or LEB to APAR	9						ns
t_{PLH} t_{PHL}	Propagation delay LEA to $\overline{ERRA}$ or LEB to $\overline{ERRB}$	7						ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	11, 12						ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An, APAR or $\overline{OEB}$ to Bn, BPAR	11, 12						ns

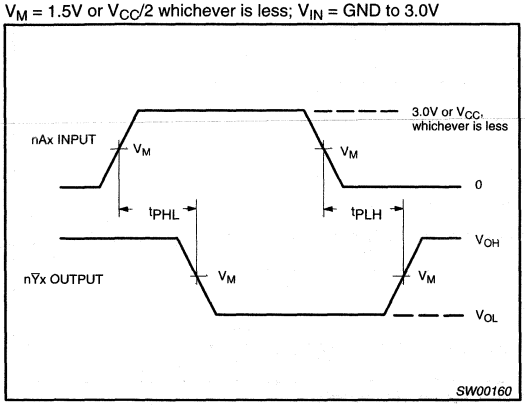
AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

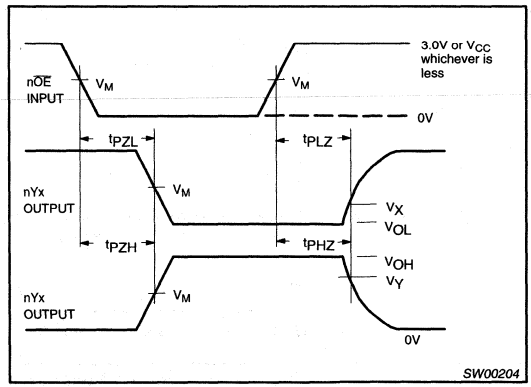
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω		T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω	
			Min	Typ	Min	
t_s(H) t_s(L)	Setup time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10				ns
t_h(H) t_h(L)	Hold time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10				ns
t_w(H)	Pulse width, High LEA or LEB	10				ns

AC WAVEFORMS

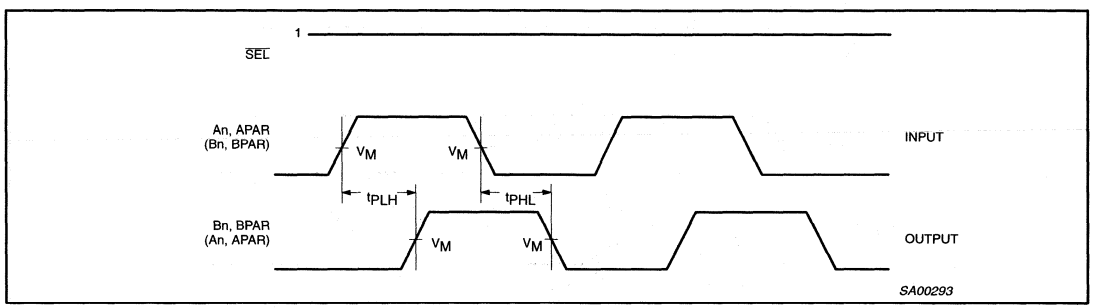
V_M = 1.5V or V_{CC}/2 whichever is less; V_{IN} = GND to 3.0V



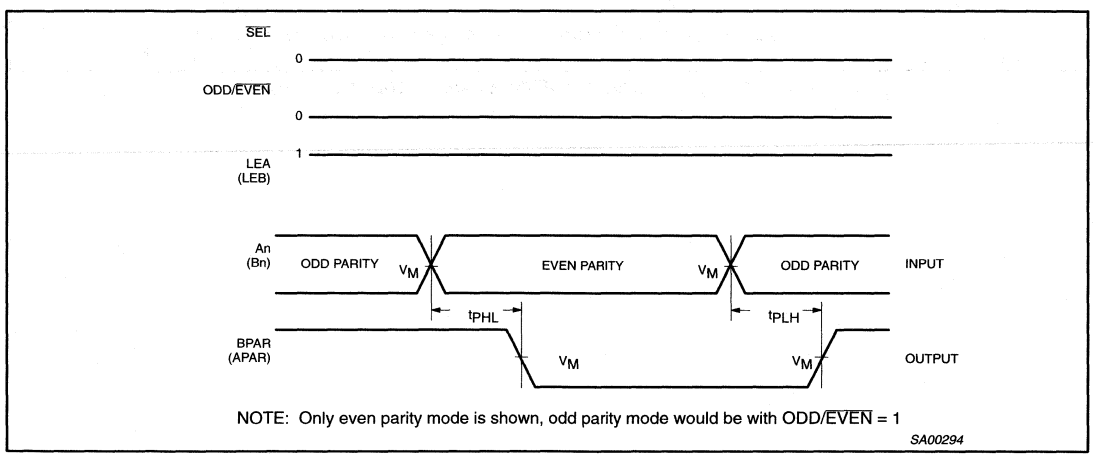
Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



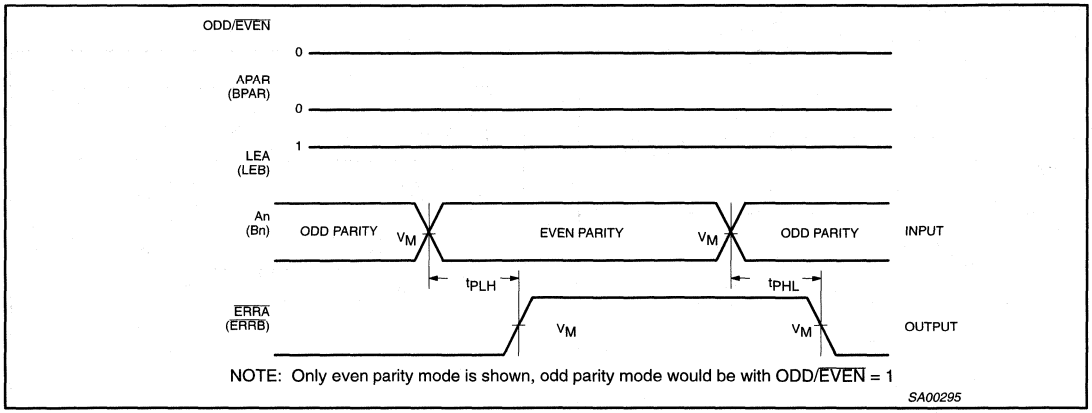
Waveform 2. 3-State Output Enable and Disable Times



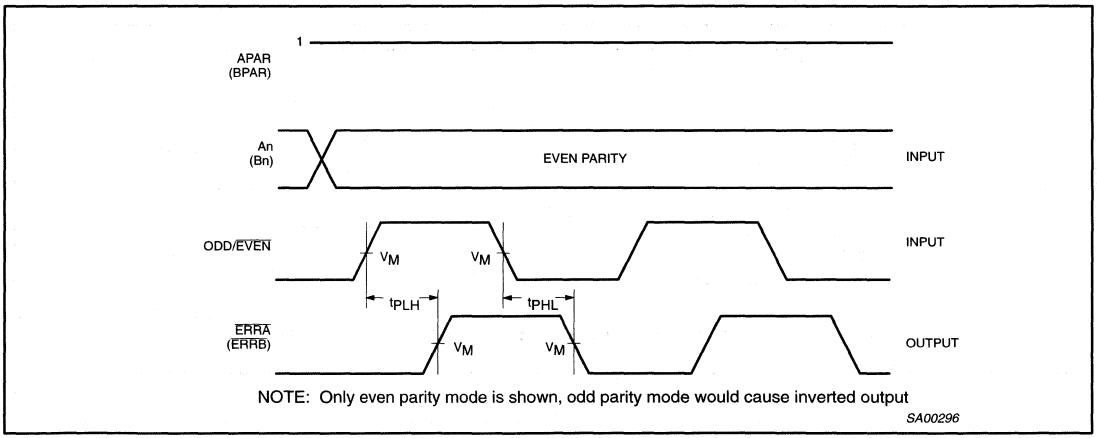
Waveform 3. Propagation Delay, An to Bn, Bn to An, APAR to BPAR, BPAR to APAR



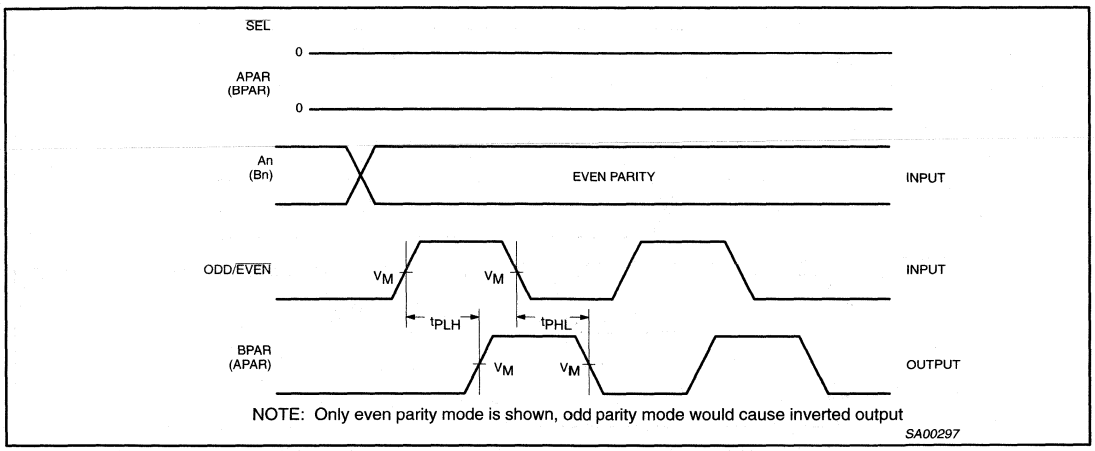
Waveform 4. Propagation Delay, An to BPAR or Bn to APAR



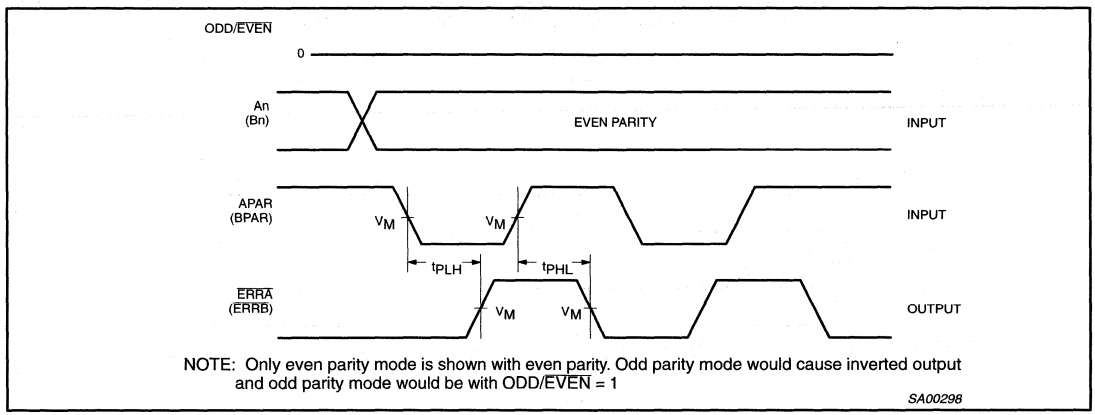
Waveform 5. Propagation Delay, An to ERRA or Bn to ERRB



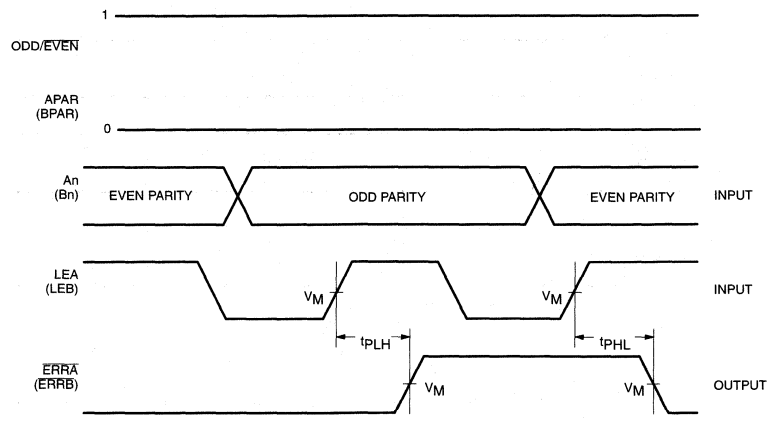
Waveform 6. Propagation Delay, ODD/EVEN to ERRA or ODD/EVEN to ERRB



Waveform 7. Propagation Delay, ODD/$\overline{\text{EVEN}}$ to APAR or ODD/$\overline{\text{EVEN}}$ to BPAR



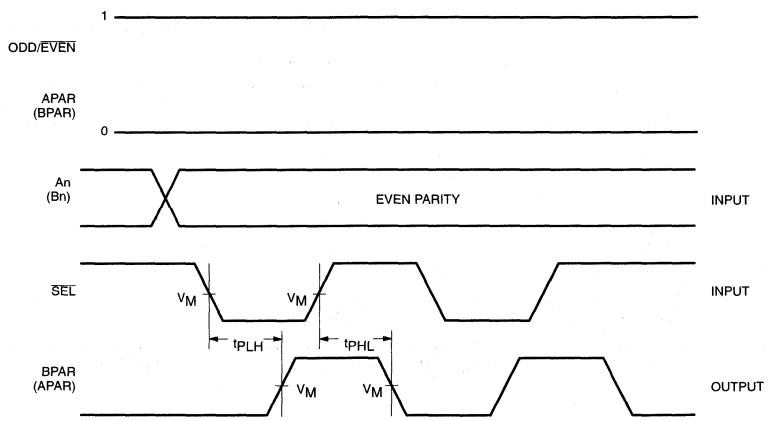
Waveform 8. Propagation Delay, APAR to $\overline{\text{ERRA}}$ or BPAR to $\overline{\text{ERRB}}$



NOTE: Only odd parity mode is shown. Even parity mode would be with ODD/$\overline{\text{EVEN}}$ = o

SA00299

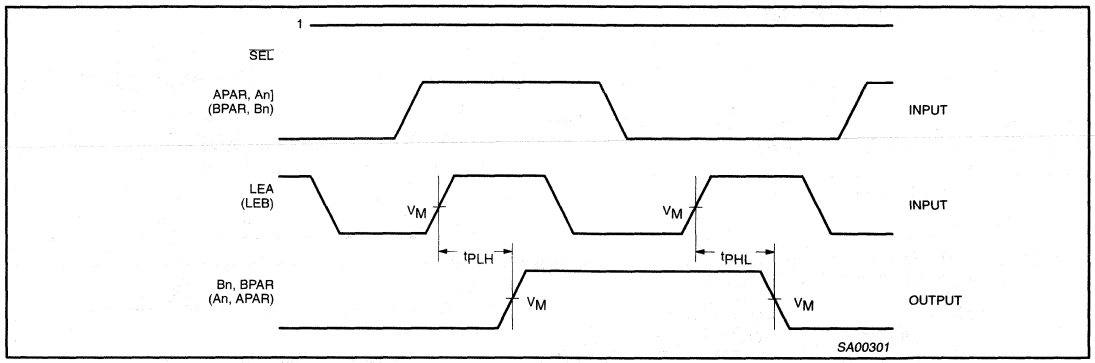
Waveform 9. Propagation Delay, LEA to $\overline{\text{ERRA}}$ or LEB to $\overline{\text{ERRB}}$



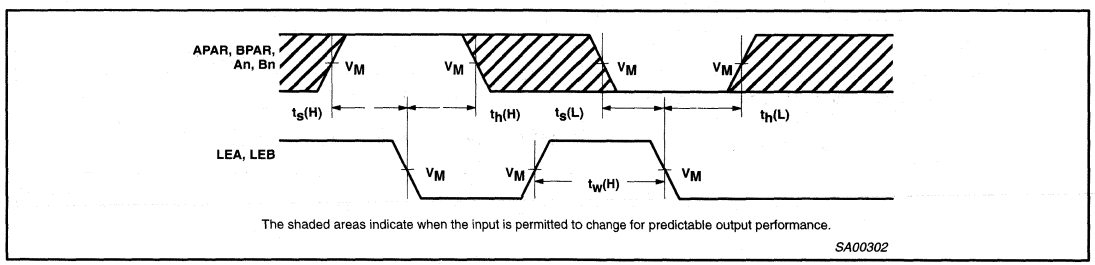
NOTE: Only even parity mode is shown with even parity. Odd parity mode would cause inverted output and odd parity mode would be with ODD/$\overline{\text{EVEN}}$ = 1

SA00300

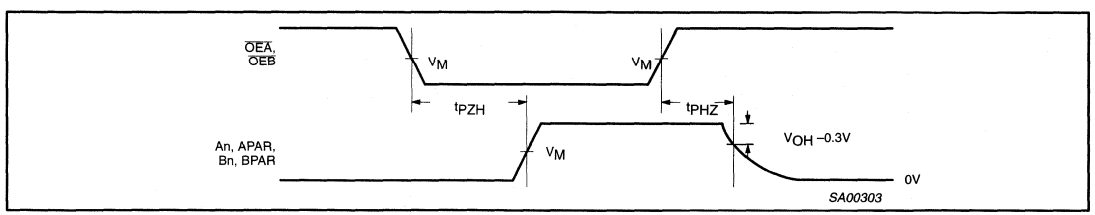
Waveform 10. Propagation Delay, $\overline{\text{SEL}}$ to BPAR or $\overline{\text{SEL}}$ to APAR



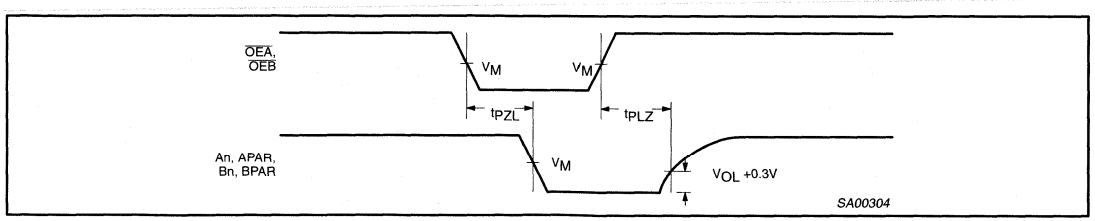
Waveform 11. Propagation Delay, LEA to BPAR or LEB to APAR, LEA to Bn or LEB to An



Waveform 12. Data Setup and Hold Times, Pulse Width High

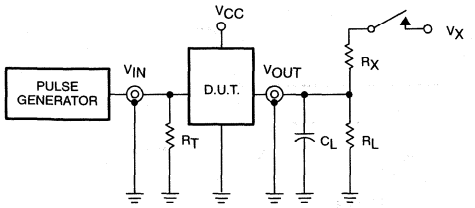


Waveform 13. 3-State Output Enable Time to High Level and Output Disable Time from High Level

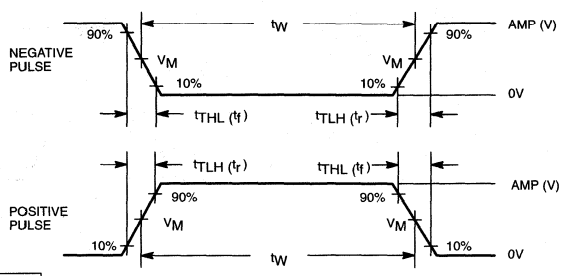


Waveform 14. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6 V or $V_{CC} \times 2$
t_{PLH}/t_{PHL}	open
t_{PHZ}/t_{PZH}	GND

LOAD VALUES

OUTPUT	R_X	V_X
$\overline{ERROR}$	100	V_{CC}
All other	500	switch

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC}, which ever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV01732

2.5V/3.3V 16-bit registered transceiver (3-State) 74ALVT16952

FEATURES

- Two 8-bit registered transceivers
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16952 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

The 74ALVT16952 is a dual octal registered transceiver. Two 8-bit registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (nCPXX) provided that the Clock Enable ($n\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($n\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

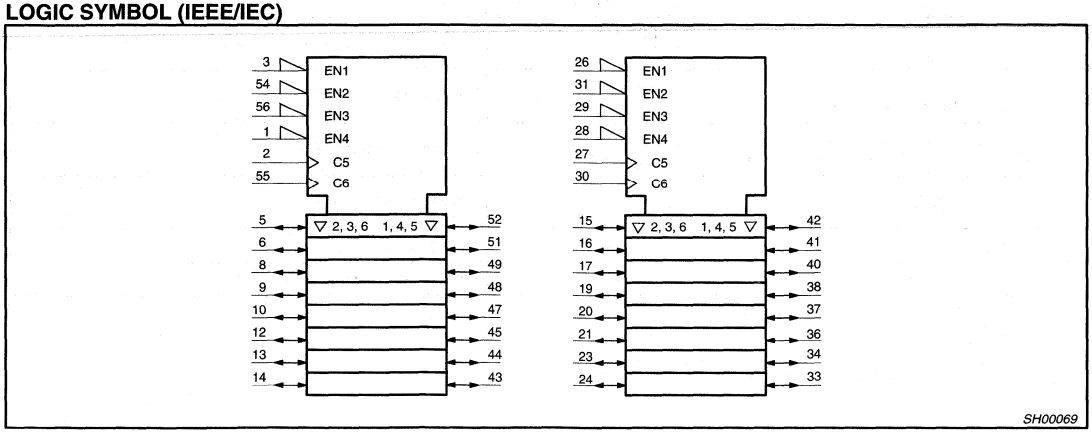
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL 2.5V	TYPICAL 3.3V	UNIT
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx or nCPAB to nBx	C_L = 50pF;	3.0 3.0	2.3 2.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or V_{CC} Outputs disabled	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	µA

ORDERING INFORMATION

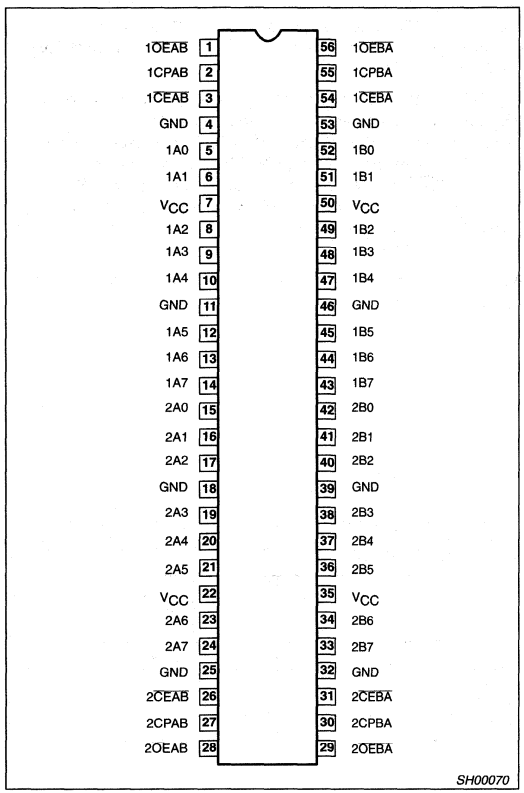
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT16952 DL	AV16952 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT16952 DGG	AV16952 DGG	SOT364-1

LOGIC SYMBOL (IEEE/IEC)

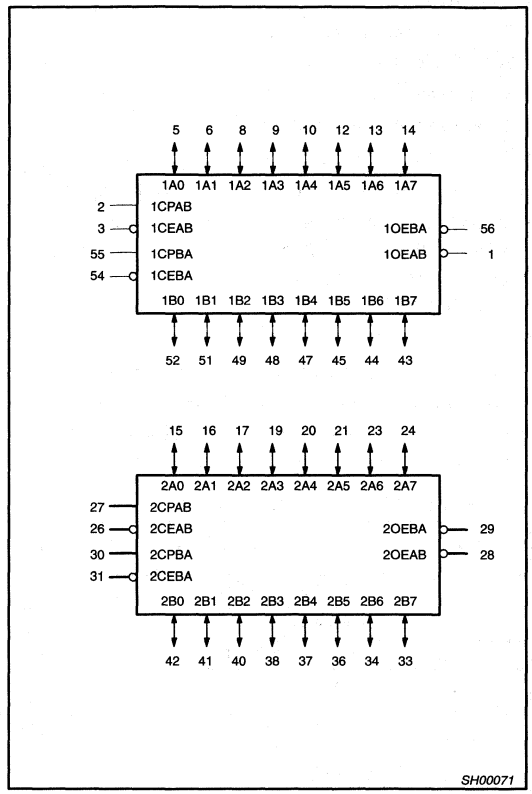


2.5V/3.3V 16-bit registered transceiver (3-State) 74ALVT16952

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55 27, 30	1CPAB / 1CPBA 2CPAB / 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	$1\overline{CEAB}$ / $1\overline{CEBA}$ $2\overline{CEAB}$ / $2\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7 2B0 – 2B7	Data inputs/outputs (B side)
1, 56 28, 29	$1\overline{OEAB}$ / $1\overline{OEBA}$ $2\overline{OEAB}$ / $2\overline{OEBA}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL Q	OPERATING MODE
nAx or nBx	nCPXX	$n\overline{CEXX}$		
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

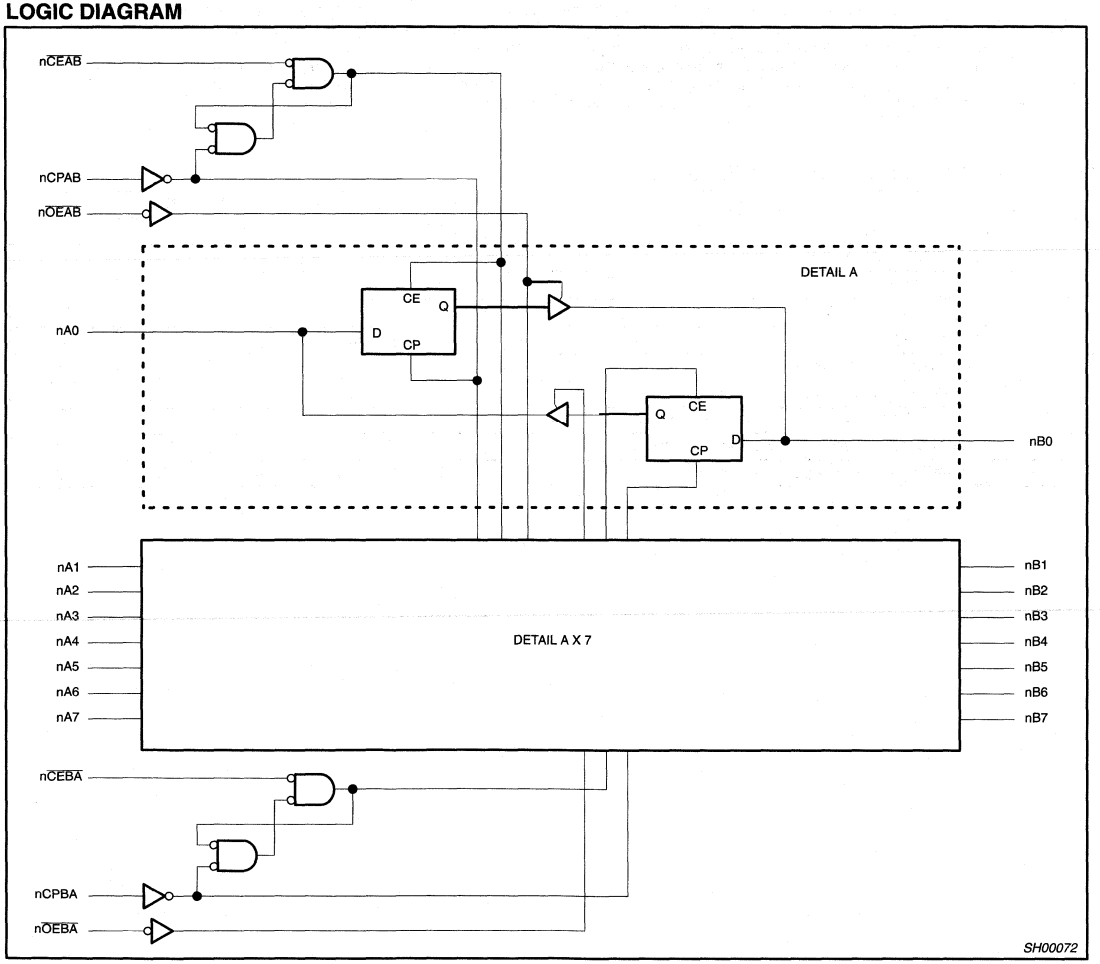
H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	nAx or nBx OUTPUTS	OPERATING MODE
$n\overline{OEXX}$			
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	output in Low state output in High state	128 –64	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B inputs	V_{CC} = 3V; V_I = 0.8V		75	120		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–130		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = −40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	100	142		MHz
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx, nCPAB to nBx	1	1.0 1.0	2.3 2.3	3.5 3.4	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	3 4	1.0 0.5	2.4 1.8	3.8 3.0	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	3 4	1.0 1.0	2.9 2.3	4.5 3.6	ns

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = −40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP	
$t_S(H)$ $t_s(L)$	Setup time nAx to nCPAB or nBx to nCPBA	2	1.5 1.5	0.9 0.7	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nCPAB or nBx to nCPBA	2	0.5 0.5	−0.6 −0.8	ns
$t_s(H)$ $t_s(L)$	Setup time n$\overline{CEAB}$ to nCPAB, n$\overline{CEBA}$ to nCPBA	2	1.1 0.5	0.2 −0.6	ns
$t_h(H)$ $t_h(L)$	Hold time n$\overline{CEAB}$ to nCPAB, n$\overline{CEBA}$ to nCPBA	2	1.5 1.0	0.6 −0.1	ns
$t_w(H)$ $t_w(L)$	nCPAB or nCPBA pulse width, High or Low	1	3.2 3.2	2.7 2.5	ns

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.8	2.1		
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 2.3V; I_{OL} = 8mA			0.3	0.4	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	Data pins[4]		0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B inputs[6]	V_{CC} = 2.5V; V_I = 0.7V			110		µA
		V_{CC} = 2.5V; V_I = 1.7V			–6		µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.5	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Bus hold current is not specified below V_{CC} =

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1	125	156		MHz
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx, nCPAB to nBx	1	1.0 1.0	3.0 3.0	3.8 3.9	ns
t_{PZH} t_{PZL}	Output enable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	3 4	1.0 0.5	3.5 2.5	5.0 3.7	ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	3 4	1.0 1.0	3.9 3.1	4.8 4.1	ns

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C

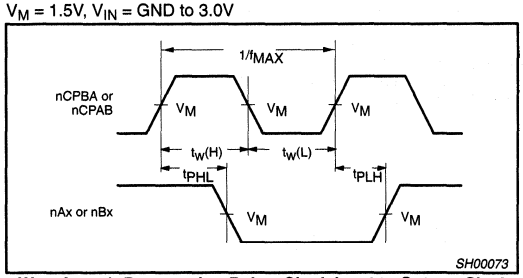
AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C

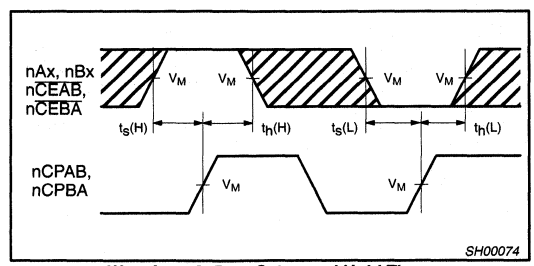
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP	
t_s(H) t_s(L)	Setup time nAx to nCPAB or nBx to nCPBA	2	1.5 2.0	0.8 1.2	ns
t_h(H) t_h(L)	Hold time nAx to nCPAB or nBx to nCPBA	2	0.5 0.5	–1.2 –0.8	ns
t_s(H) t_s(L)	Setup time n$\overline{CEAB}$ to nCPAB, n$\overline{CEBA}$ to nCPBA	2	1.0 1.0	0.0 –0.2	ns
t_h(H) t_h(L)	Hold time n$\overline{CEAB}$ to nCPAB, n$\overline{CEBA}$ to nCPBA	2	1.1 1.1	0.3 0.2	ns
t_w(H) t_w(L)	nCPAB or nCPBA pulse width, High or Low	1	3.2 2.0	2.7 1.5	ns

AC WAVEFORMS

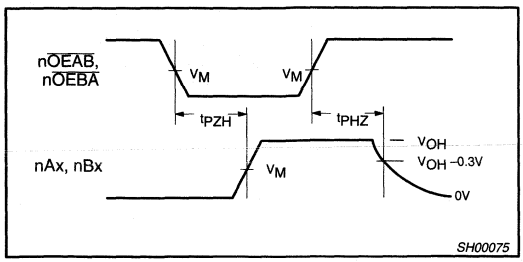
V_M = 1.5V, V_{IN} = GND to 3.0V



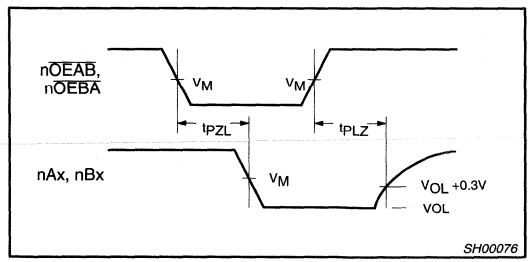
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

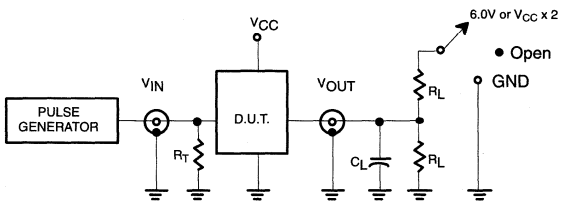


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

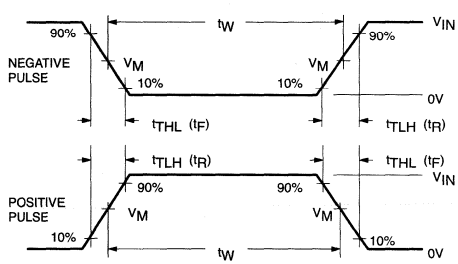


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00025

Section 5
3.3V Devices
BTL, GTL

BiCMOS Bus Interface Logic

CONTENTS

10-bit BTL transceiver with registers 74ABTL3205

FEATURES

- 10-bit BTL transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Tight output skew (0.5nsec typical)
- Glitch-free power up/down operation
- Low I_{CC} current
- Supports live insertion
- High density packaging
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

This transceiver is a 10 bit bidirectional transceiver and is intended to provide the electrical interface to a high performance wired-OR bus.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading (<6pF) by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

To support live insertion, OEB is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package. The LOGIC V_{CC} and BUS V_{CC} pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

This transceiver function is intended to operate in a half-duplex mode. Low current in standby mode is obtained by powering down unused circuitry. Likewise, transmit circuitry is powered down when in receive mode and receive circuitry is powered down while in transmit mode.

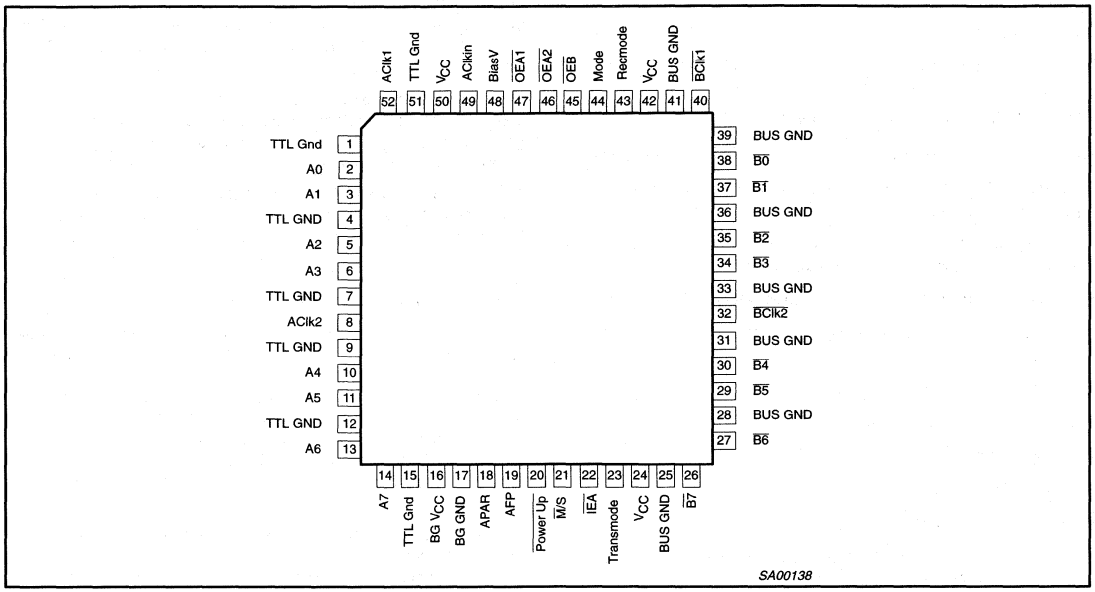
QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Bn}$		3.3 3.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to An		3.6 3.5	ns
C_{OB}	Output capacitance ($\overline{B0}$ - $\overline{B8}$) only)		6	pF
I_{OL}	Output current ($\overline{B0}$ - $\overline{B8}$) only)		100	mA
I_{CC}	Supply current	Standby	1	mA
		An to $\overline{Bn}$	7	
		$\overline{Bn}$ to An	18	

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52-PIN PQFP	–40°C to +85°C	74ABTL3205 BB	74ABTL3205 BB	SOT379-1

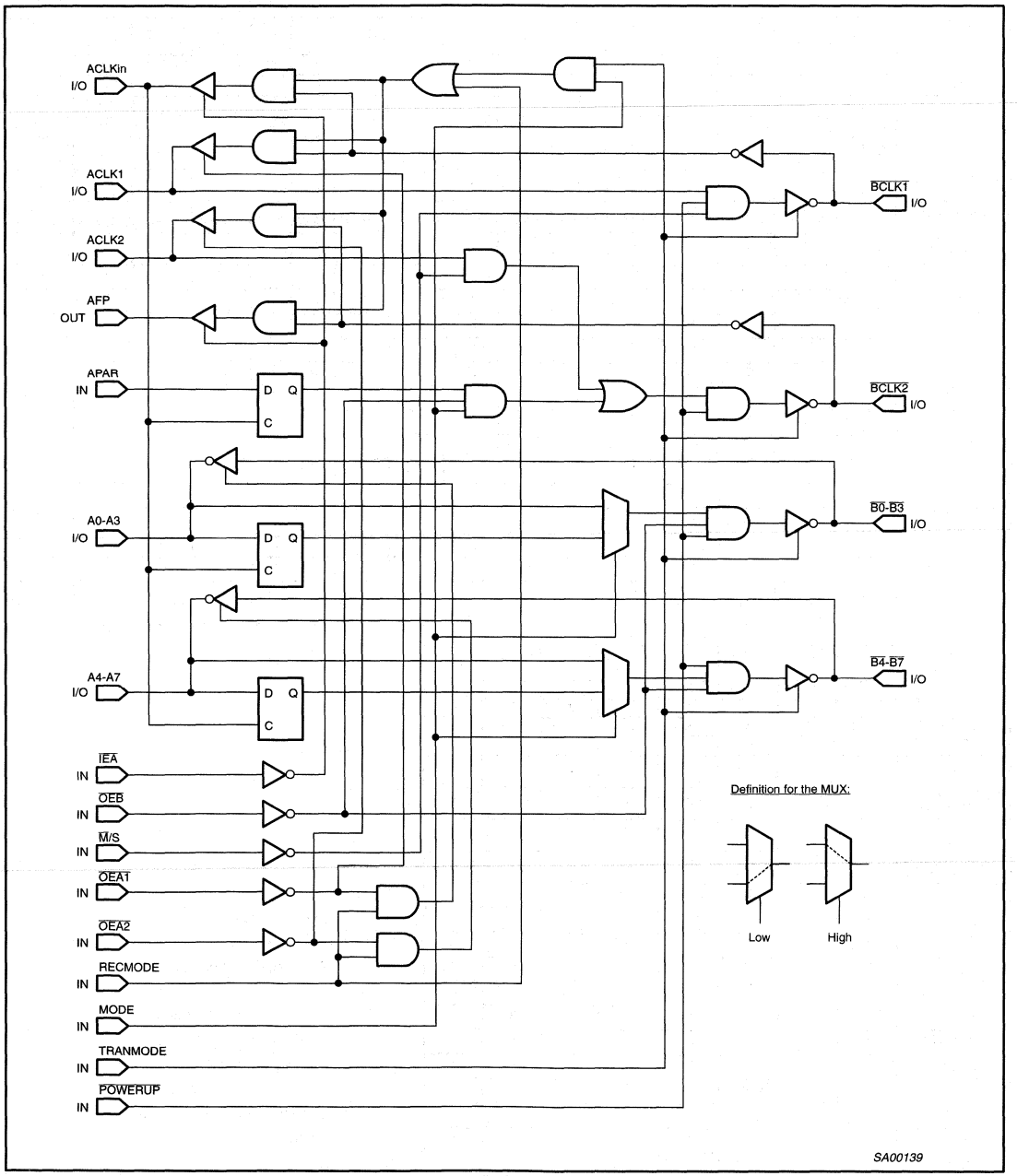
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	FUNCTION	ASSERTION	I/O	LOGIC
OEA1	Output enable data receiver group 1	Low	Input	TTL
OEA2	Output enable data receiver group 2	Low	Input	TTL
OEB	Output enable data transmitter	Low	Input	TTL
IEA	Output enable clock and framepulse receiver	Low	Input	TTL
M/S	Master/Slave select: L: Master, enable clock transmitter H: Slave, disable clock transmitter		Input	TTL
Mode	 Low: Data through mode High: Registered data mode		Input	TTL
Power Up	Power up mode, held low during power up to disable clock and data transmitters	Low	Input	TTL
Recmode	Enables receiver	High	Input	TTL
Tranmode	Enables transmitter	High	Input	TTL
AClk1	Clock or data path		I/O	TTL
AClkIn	 IEA = H → Input for busclock IEA = L → Output for busclock		I/O	TTL
A0..A3	data group 1		I/O	TTL
AClk2	Clock or data path		I/O	TTL
AFPIn	Alternate data path		Output	TTL
APAR	Alternate data path		Input	TTL
A4..A7	data group 2		I/O	TTL
BClk1	Clock or data path		I/O	BTL
B0..B3	data group 1		I/O	BTL
BClk2	Clock or data path		I/O	BTL
B4..B7	data group 2		I/O	BTL

LOGIC DIAGRAM



FUNCTION TABLE

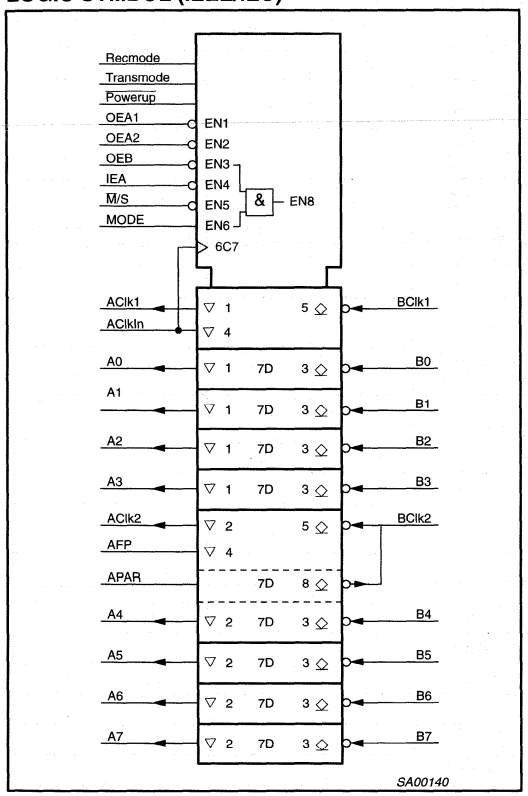
MODE	INPUTS																
	An	$\overline{Bn}$	ACLK in	ACLK 1	ACLK 2	$\overline{BCLK1}$	$\overline{BCLK2}$	$\overline{OEA1}$	$\overline{OEA2}$	$\overline{OEB}$	APAR	$\overline{IEA}$	$\overline{M/S}$	MODE	REC MODE	TRAN MODE	$\overline{POWER\ UP}$
An to Bn (REGISTERED)	l	O	±	X	X	X	X	H	H	L	X	H	X	H	L	H	H
	h	O	±	X	X	X	X	H	H	L	X	H	X	H	L	H	H
AN to Bn (THROUGH)	L	O	X	X	X	X	X	H	H	L	X	X	X	L	L	H	H
	H	O	X	X	X	X	X	H	H	L	X	X	X	L	L	H	H
B0-B3 to A0-A3 (THROUGH)	O	L	X	X	X	X	X	L	X	H	X	X	X	X	H	L	L
	O	H	X	X	X	X	X	L	X	H	X	X	X	X	H	L	L
B4-B7 to A4-A7 (THROUGH)	O	L	X	X	X	X	X	X	L	H	X	X	X	X	H	L	L
	O	H	X	X	X	X	X	X	L	H	X	X	X	X	H	L	L
ACLK1 to BCLK1	X	X	X	L	X	O	X	H	X	X	X	X	L	X	X	H	H
	X	X	X	H	X	O	X	H	X	X	X	X	L	X	X	H	H
ACLK2 to BCLK2	X	X	X	X	L	X	O	X	H	H	X	X	L	L	X	H	H
	X	X	X	X	H	X	O	X	H	H	X	X	L	L	X	H	H
BCLK1 to ACLK1	X	X	X	O	X	L	X	L	X	X	X	X	X	X	H	L	X
	X	X	X	O	X	H	X	L	X	X	X	X	X	X	H	L	X
BCLK2 to ACLK2	X	X	X	X	O	X	L	X	L	X	X	X	X	X	H	L	X
	X	X	X	X	O	X	H	X	L	X	X	X	X	X	H	L	X
APAR to BCLK2	X	X	±	X	X	X	X	X	X	L	l	X	H	H	X	H	H
	X	X	±	X	X	X	X	X	X	L	h	X	H	H	X	H	H
BCLK2 to AFPIn	X	X	X	X	X	X	L	X	X	X	X	L	X	X	H	L	X
	X	X	X	X	X	X	H	X	X	X	X	L	X	X	H	L	X
BCLK1 to ACLKin	X	X	O	X	X	L	X	H	H	L	O	L	H	H	L	H	H
	X	X	O	X	X	H	X	H	H	L	O	L	H	H	L	H	H

MODE	OUTPUTS							
	An	$\overline{Bn}$	ACLK in	ACLK1	ACLK2	$\overline{BCLK1}$	$\overline{BCLK2}$	AF Pin
An to Bn (REGISTERED)	Input	H*	X	X	X	X	X	X
	Input	L	X	X	X	X	X	X
AN to Bn (THROUGH)	Input	H*	X	X	X	X	X	X
	Input	L	X	X	X	X	X	X
B0-B3 to A0-A3 (THROUGH)	H	Input	Input	X	X	X	X	X
	L	Input	Input	X	X	X	X	X
B4-B7 to A4-A7 (THROUGH)	H	Input	Input	X	X	X	X	X
	L	Input	Input	X	X	X	X	X
ACLK1 to BCLK1	X	X	X	Input	X	H*	X	X
	X	X	X	Input	X	L	X	X
ACLK2 to BCLK2	X	X	X	X	Input	X	H*	X
	X	X	X	X	Input	X	L	X
BCLK1 to ACLK1	X	X	X	H	X	Input	X	X
	X	X	X	L	X	Input	X	X
BCLK2 to ACLK2	X	X	X	X	H	X	Input	X
	X	X	X	X	L	X	Input	X
APAR to BCLK2	X	X	Input	X	X	X	H*	X
	X	X	Input	X	X	X	L	X
BCLK2 to AFPIn	X	X	X	X	X	X	Input	H*
	X	X	X	X	X	X	Input	L
BCLK1 to ACLKin	X	X	H	X	X	Input	X	X
	X	X	L	X	X	Input	X	X

NOTES:

H = High voltage level
L = Low voltage level
h = High voltage level one set-up time prior to Low to High ACLKin transition
l = Low voltage level one set-up time prior to Low to High ACLKin transition
± = Low to High transition
Z = High impedance (off) state
H* = Goes to level of pull-up voltage
X = Don't care
O = Output

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage	TTL Signals	–1.2 to +7.0	V
		BTL Signals	–1.2 to +5.5	V
I_{IN}	Input current		–18 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	/v
I_{OUT}	Current applied to output in Low output state	A0 - A8	48	mA
		$\overline{B0}$ - $\overline{B8}$	200	mA
T_{amb}	Operating free-air temperature range		–40 to +85	°C
T_{STG}	Storage temperature		–65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{BTL}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V		0.5	100	µA
I_{OFF}	Power-off output current	$\overline{BTL}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V		10	100	µA
V_{OH}	High-level output voltage	TTL	V_{CC} = MIN, V_{IL} = MAX,[4] V_{IH} = MIN, I_{OH} = –3mA	2.5	2.85	3.4	V
			V_{CC} = MIN to MAX, [4] V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –10µA			V_{CC} – 1.1	V
V_{OL}	Low-level output voltage	TTL	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA		0.35	0.5	V
		$\overline{BTL}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA	0.75	1.0	1.10	V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 4mA	0.5	0.7		V
V_{IK}	Input clamp voltage	TTL	V_{CC} = MIN, I_I = I_{IK}		0.8	–1.2	V
		$\overline{BTL}$	V_{CC} = MIN, I_I = –18mA		0.8	–1.2	V
I_I	Input current at maximum input voltage	TTL	V_{CC} = MAX, V_I = 0.5V or 5.5V		0.1	±50	µA
I_{IH}	High-level input current	$\overline{TTL}$	V_{CC} = MAX, V_I = 2.7V, $\overline{Bn}$ = AIn = 0V		0.1	20	µA
		$\overline{BTL}$	V_{CC} = MAX, V_I = 1.9V		0.1	100	µA
			V_{CC} = MAX, V_I = 3.5V[5]	100			mA
I_{IL}	Low-level input current	TTL	V_{CC} = MAX, V_I = 0.5V		0.1	–20	µA
		$\overline{BTL}$	V_{CC} = MAX, V_I = 0.75V		0.1	–100	µA
I_{OZH}	Off-state output current	TTL	V_{CC} = MAX, V_O = 2.7V		0.1	50	µA
I_{OZL}	Off-state output current	TTL	V_{CC} = MAX, V_O = 0.5V		20	–50	µA
I_{OS}	Short-circuit output current[3]	TTL	V_{CC} = MAX, V_O = 0.0V	–60	130	–150	mA
I_{CC}	Supply current (total)	Recmode Low Tranmode Low	V_{CC} = MAX		1	3	mA
		Recmode Low Tranmode High	V_{CC} = MAX Mode = Low		7	12	mA
		Recmode Low Tranmode High	V_{CC} = MAX Mode = High		13	21	mA
		Recmode High Tranmode Low	V_{CC} = MAX		18	25	mA
		Recmode High Tranmode High	V_{CC} = MAX		29	43	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
5. For B port input voltage between 3 and 5 volts I_{IH} will be greater than 100µA, but the parts will continue to function normally.

TTL signals CLKin, CLK-1/CLK-OUT, CLK-2/FP-OUT, /FP-IN, /PARITY t,A0..A7, OEB, MASTER/SLAVE, MODE, OEA1, OEA2

BTL signals CLK1BTL, CLK2BTL, B0..B7

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{BIASV}	Bias pin DC current	V_{CC} = 0 to 5.25V, $\overline{Bn}$ = 0 to 2.0 V	4.5		5.5	V
I_{BIASV}	Bias pin DC current	V_{CC} = 0 to 4.75 V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			1	mA
		V_{CC} = 4.5 to 5.5V, $\overline{Bn}$ = 0 to 2.0 V, Bias V = 4.5 to 5.5V			10	µA
$\overline{Bn}$	Bus voltage during prebias	$\overline{B0}$ – $\overline{B8}$ = 0V, Bias V = 5.0V	1.62		2.1	V

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, C_L = 500Ω			T_{amb} = –40°C to +85°C, V_{CC} = 5V ± 10%, C_L = 50pF, C_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to An	Waveform 2	2.0 1.8	3.6 3.5	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PLH} t_{PHL}	Propagation delay, BCLK1 to ACLK1	Waveform 2	2.0 1.8	3.8 3.6	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PLH} t_{PHL}	Propagation delay BCLK1 to ACLKin	Waveform 2	2.0 1.8	3.7 3.7	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PLH} t_{PHL}	Propagation delay BCLK2 to ACLK2	Waveform 2	2.0 1.8	3.7 3.9	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PLH} t_{PHL}	Propagation delay BCLK2 to AFP	Waveform 2	2.0 1.8	3.8 3.9	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PZH} t_{PLZ}	Output Enable time $\overline{OEA1}$, $\overline{OEA2}$, $\overline{IEA}$ to An	Waveform 1, 2	2.0 1.8	3.8 2.5	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEA1}$, $\overline{OEA2}$, $\overline{IEA}$ to An	Waveform 4, 5	1.6 2.0	2.5 3.3	5.6 7.8	1.4 1.8	5.7 8.2	ns
t_{TLH} t_{THL}	Output transition time, An Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				3.0 1.7	7.0 4.0	ns
$t_{SK}(p)$	Pulse skew[2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 3		2.0				ns

NOTES:

1. $\lvert t_{PN}$ actual – t_{PM} actual$\rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle. (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_D = 30pF, R_U = 18.5Ω			T_{amb} = –40°C to +85°C V_{CC} = 5V ± 10% C_L = 30pF, R_U = 18.5Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Bn}$	Waveform 2	1.0 1.0	3.3 2.7	4.7 4.5	1.0 1.0	5.7	ns
t_{PLH} t_{PHL}	Propagation delay, ACLKin to $\overline{Bn}$	Waveform 1, 2	2.0 2.0	4.6 4.5	5.9 5.9	2.0 2.0	6.3 6.3	ns
t_{PLH} t_{PHL}	Propagation delay ACLKin to BCLK2	Waveform 1, 2	2.0 2.0	4.6 4.5	7.3 7.3	2.0 2.0	7.6 7.6	ns
t_{PLH} t_{PHL}	Propagation delay ACLK1 to BCLK1	Waveform 2	1.0 1.0	3.2 2.9	4.7 4.5	1.0 1.0	5.1 4.7	ns
t_{PLH} t_{PHL}	Propagation delay ACLK2 to BCLK2	Waveform 2	1.0 1.0	3.1 3.1	5.7 5.5	1.0 1.0	6.0 5.6	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}$ to $\overline{Bn}$ or BCLK2	Waveform 1, 2	1.0 1.0	3.8 3.4	6.8 6.4	1.0 1.0	7.6 6.9	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.6		2.5 2.0	1.0 0.6	3.0 2.5	ns
$t_{SK}(p)$	Pulse skew2 $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 3		2.0				ns

NOTES:

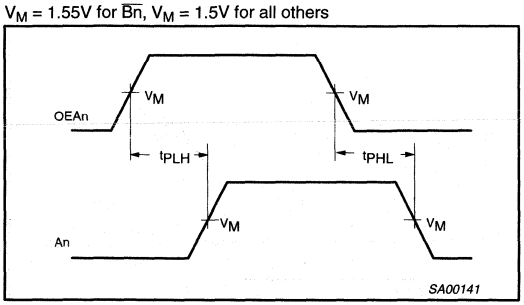
1. $\lvert t_{PN}$ actual – t_{PM} actual$\rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle. (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC SETUP REQUIREMENTS

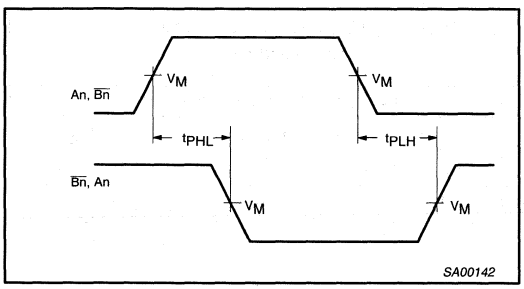
SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT
			T_{amb} = +25°C V_{CC} = 5V		T_{amb} = –40°C to +85°C V_{CC} = 5V ± 10%		
			C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 18.5Ω (B side)				
			MIN	TYP	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time An to ACLKin	Waveform 6	1.9 1.3		2.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time An to ACLKin	Waveform 6	1.8 2.0		2.3 2.0		ns

AC WAVEFORMS

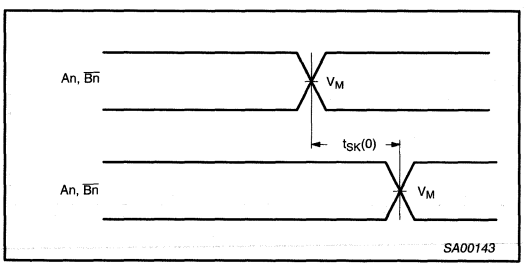
V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others



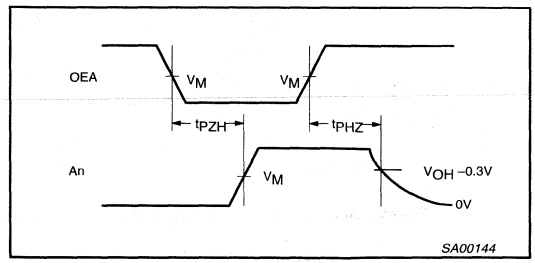
Waveform 1. Propagation Delay for Data or Output Enable to Output



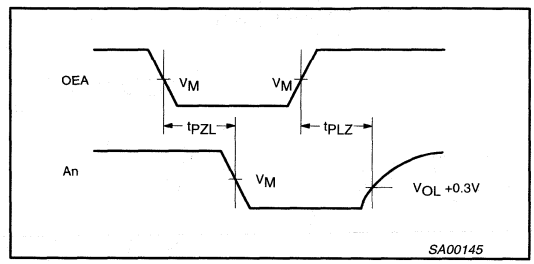
Waveform 2. Propagation Delay for Data to Output



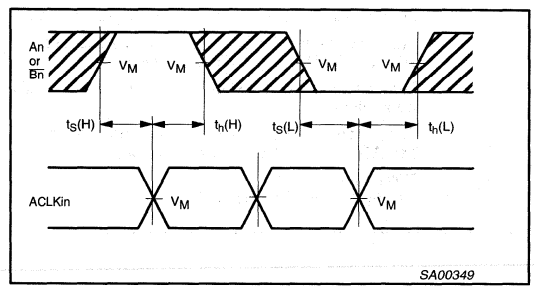
Waveform 3. Output Skews



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

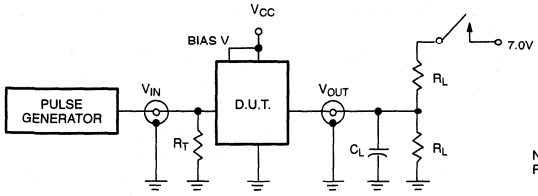


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 6. Data Setup and Hold Times

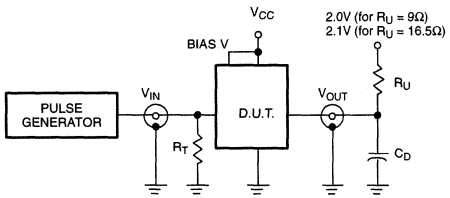
TEST CIRCUIT AND WAVEFORMS



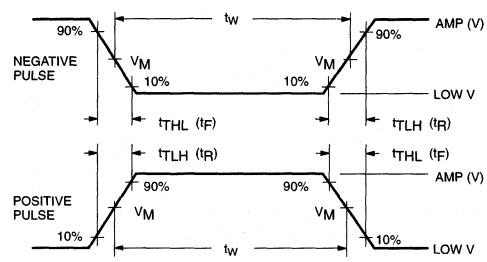
Test Circuit for 3-State Outputs on A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit for Outputs on B Port



V_M = 1.55V for Bn or $\overline{Bn}$, V_M = 1.5V for all others

Input Pulse Definition

ABTL	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

SA00146

9-bit BTL 3.3V latched/registered/pass-thru Futurebus+ transceiver

FBL2031

FEATURES

- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port

DESCRIPTION

The FBL2031 is a 9-bit latched/registered transceiver featuring a latched, registered or pass-thru mode in either the A-to-B or B-to-A direction.

The FBL2031 is intended to provide the electrical interface to a high performance wired-OR bus.

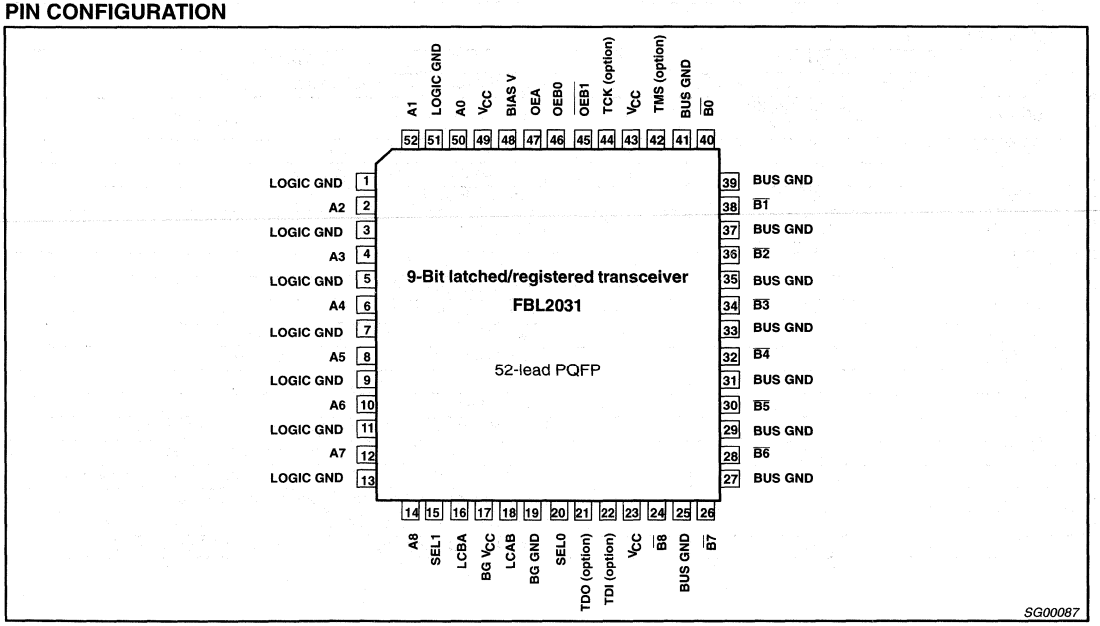
QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Bn}$		2.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to An		4.4 4.2	ns
C_O	Output capacitance ($\overline{B0}$ – $\overline{Bn}$ only)		6	pF
I_{OL}	Output current ($\overline{B0}$ – $\overline{Bn}$ only)		100	mA
I_{CC}	Supply current	AIn to $\overline{Bn}$ (outputs Low or High)	17	mA
		$\overline{Bn}$ to AOn (outputs Low)	50	
		$\overline{Bn}$ to AOn (outputs High)	25	

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 3.3V±10%; T_{amb} = 0°C to +70°C	DWG No.
52-pin Plastic Quad Flat Pack (PQFP)	FBL2031BB	SOT379-1

PIN CONFIGURATION



9-bit BTL 3.3V latched/registered/pass-thru Futurebus+ transceiver

FBL2031

DESCRIPTION

The TTL-level side (A port) has a common I/O. The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two mode select inputs (SEL0 and SEL1). A "00" configures latches in both directions. A "10" configures thru mode in both directions. A "01" configures register mode in both directions. A "11" configures register mode in the A-to-B direction and latch mode in the B-to-A direction.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the register mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-Low latch enables. Regardless of the mode, data is inverted from input to output.

The 3-State A port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and $\overline{OEB1}$. Only when OEB0 is High and $\overline{OEB1}$ is Low is the output enabled.

When either OEB0 is Low or $\overline{OEB1}$ is High, the B port is inactive and is pulled to the level of the pullup voltage. New data can be entered in the register and latched modes or can be retained while the associated outputs are in 3-State (A port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The "V_{OH}" clamp reduces inductive ringing effects during a Low-to-High transition. The "V_{OH}" clamp is always active. The other clamp, the "trapped reflection" clamp, clamps out ringing below the BTL 0.5V V_{OL} level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch-free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be infrequent and impossible to troubleshoot.

As with any high power device, thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.

PACKAGE THERMAL CHARACTERISTICS

PARAMETER	CONDITION	52-PIN PLASTIC QFP
θja	Still air	80°C/W
θja	300 Linear feet per minute air flow	58°C/W
θjc	Thermally mounted on one side to heat sink	20°C/W

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
A0 – A8	50, 52, 2, 4, 6, 8, 10, 12, 14	I/O	BiCMOS data inputs/3-State outputs (TTL)
$\overline{B0}$ – $\overline{B8}$	40, 38, 36, 34, 32, 30, 28, 26, 24	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the B outputs when High
$\overline{OEB1}$	45	Input	Enables the B outputs when Low
OEA	47	Input	Enables the A outputs when High
BUS GND	25, 27, 29, 31, 33, 35, 37, 39, 41	GND	Bus ground (0V)
LOGIC GND	51, 1, 3, 5, 7, 9, 11, 13	GND	Logic ground (0V)
V_{CC}	23, 43, 49	Power	Positive supply voltage
BIAS V	48	Power	Live insertion pre-bias pin
BG V_{CC}	17	Power	Band Gap threshold voltage reference
BG GND	19	GND	Band Gap threshold voltage reference ground
SEL0	20	Input	Mode select
SEL1	15	Input	Mode select
LCAB	18	Input	A to B clock/latch enable (transparent latch when Low)
LCBA	16	Input	B to A clock/latch enable (transparent latch when Low)
TMS	42	Input	Test Mode Select (optional, if not implemented then no connect)
TCK	44	Input	Test Clock (optional, if not implemented then no connect)
TDI	22	Input	Test Data In (optional, if not implemented then no connect)
TDO	21	Output	Test Data Out (optional, if not implemented then shorted to TDI)

9-bit BTL 3.3V latched/registered/pass-thru Futurebus+ transceiver

FBL2031

FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	An	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	OEA	LCAB	LCBA	SEL0	SEL1	An	$\overline{Bn}$
An to $\overline{Bn}$ thru mode	L	—	H	L	L	X	X	H	L	input	H**
	H	—	H	L	L	X	X	H	L	input	L
An to $\overline{Bn}$ transparent latch	L	—	H	L	L	L	X	L	L	input	H**
	H	—	H	L	L	L	X	L	L	input	L
An to $\overline{Bn}$ latch and read	l	—	H	L	L	↑	X	L	L	input	H**
	h	—	H	L	L	↑	X	L	L	input	L
$\overline{Bn}$ outputs latched and read (preconditioned latch)	X	—	H	L	X	H	X	L	L	X	latched data
An to $\overline{Bn}$ register	l	—	H	L	L	↑	X	X	H	input	H**
	h	—	H	L	L	↑	X	X	H	input	L
$\overline{Bn}$ to An thru mode	—	L	Disable		H	X	X	H	L	H	input
	—	H	Disable		H	X	X	H	L	L	input
$\overline{Bn}$ to An transparent latch	—	L	Disable		H	X	L	L	L	H	input
	—	H	Disable		H	X	L	L	L	L	input
	—	L	Disable		H	X	L	H	H	H	input
	—	H	Disable		H	X	L	H	H	L	input
$\overline{Bn}$ to An latch and read	—	l	Disable		H	X	↑	L	L	H	input
	—	h	Disable		H	X	↑	L	L	L	input
	—	l	Disable		H	X	↑	H	H	H	input
	—	h	Disable		H	X	↑	H	H	L	input
An outputs latched and read (preconditioned latch)	—	X	X	X	H	X	H	L	L	latched data	X
	—	X	X	X	H	X	H	H	H	latched data	X
$\overline{Bn}$ to An register	—	l	Disable		H	X	↑	L	H	H	input
	—	h	Disable		H	X	↑	L	H	L	input
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	X	X	X	X	X	X	H**
Disable An outputs	X	X	X	X	L	X	X	X	X	Z	X

FUNCTION SELECT TABLE

MODE SELECTED	SEL0	SEL1
Thru mode	H	L
Register mode (An to Bn)	X	H
Latch mode (An to Bn)	L	L
Register mode (Bn to An)	L	H
Latch mode (Bn to An)	L	L
	H	H

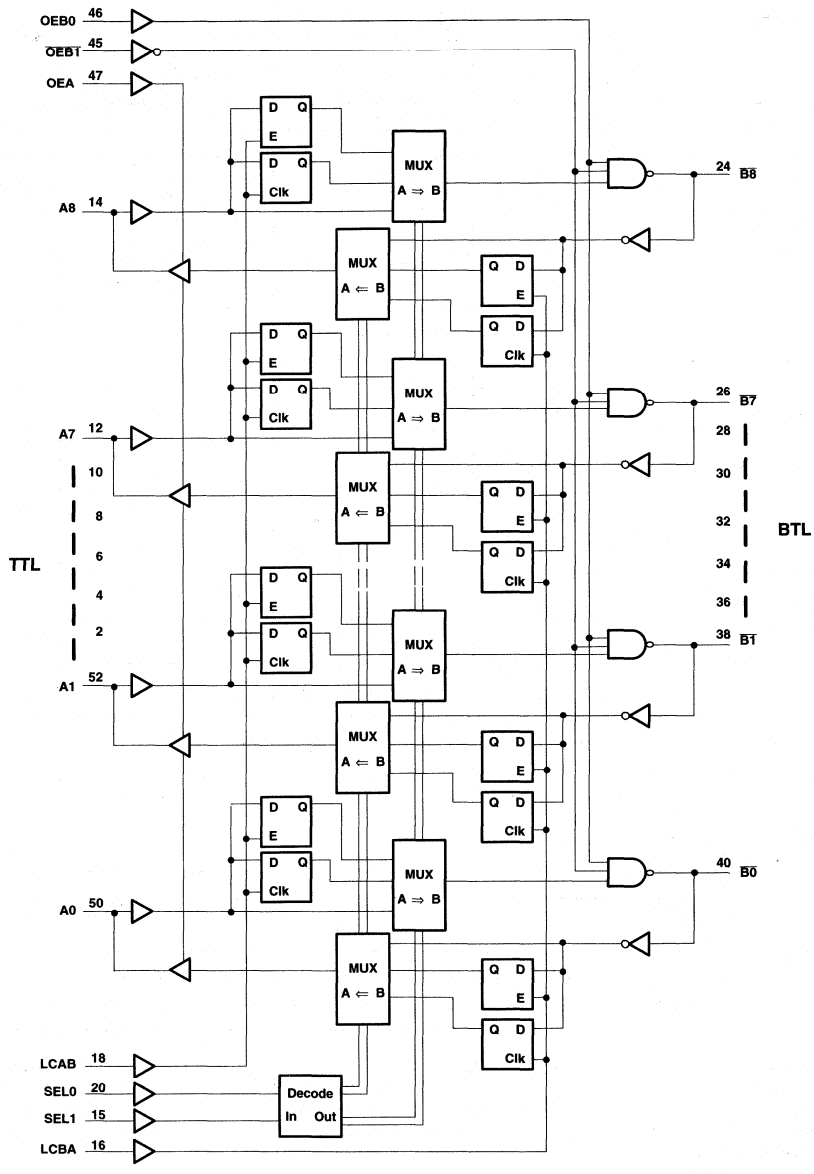
NOTES:

H = High voltage level
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High LCXX transition
h = High voltage level one set-up time prior to the Low-to-High LCXX transition
X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
↑ = Low-to-High transition
H** = Goes to level of pull-up voltage
$\overline{Bn}$* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.
Disable = OEB0 is Low or $\overline{OEB1}$ is High.

9-bit BTL 3.3V latched/registered/pass-thru Futurebus+ transceiver

FBL2031

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +4.6	V
V_{IN}	Input voltage	AI0 – AI6, OEB0, $\overline{OEBn}$, OEAn	-0.5 to +7.0	V
		$\overline{B0} – \overline{B8}$	-0.5 to +3.5	
I_{IN}	Input current	$V_{IN} < 0$	-50	
V_{OUT}	Voltage applied to output in High output state		-0.5 to +7.0	V
I_{OUT}	Current applied to output in	AO0 – AO8	128, –64	mA
	Low output state/High output state	$\overline{B0} – \overline{B8}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		COMMERCIAL LIMITS V_{CC} = 3.3V±10%; T_{amb} = 0 to +70°C			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage	Except $\overline{B0}–\overline{B8}$	2.0			V
		$\overline{B0} – \overline{B8}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}–\overline{B8}$			0.8	V
		$\overline{B0} – \overline{B8}$			1.47	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	AO0 – AO8			-12	mA
I_{OL}	Low-level output current	AO0 – AO8			+12	mA
		$\overline{B0} – \overline{B8}$			100	
C_{OB}	Output capacitance on B port			6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	°C

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
V_{BIASV}	Bias pin voltage	Voltage difference between the Bias voltage and V_{CC} after the PCB is plugged in.	–	–	0.5	V
I_{BIASV}	Bias pin (I_{BIASV}) input DC current	V_{CC} = 0 V, Bias V = 3.6V			1.2	mA
		V_{CC} = 3.3V, Bias V = 3.6V			10	µA
$V_{\overline{Bn}}$	Bus voltage during prebias	$\overline{B0} – \overline{B8}$ = 0V, Bias V = 3.3V	1.62		2.1	V
I_{LM}	Fall current during prebias	$\overline{B0} – \overline{B8}$ = 2V, Bias V = 1.3 to 2.5V			1	µA
I_{HM}	Rise current during prebias	$\overline{B0} – \overline{B8}$ = 1V, Bias V = 3 to 3.6V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 3.3V, $\overline{B0} – \overline{B8}$ = 0 to 2.0V, Bias V = 2.7 to 3.6V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 3.3V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 1.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 3.3V	1.0	1.35		ns

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0} - \overline{B8}$	V_{CC} = MAX, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0} - \overline{B8}$	V_{CC} = 0V, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	AO0 – AO8[3]	V_{CC} = MIN to MAX	V_{CC} –0.2			V
			V_{CC} = MIN; I_{OH} = -8mA	2.4			V
			V_{CC} = MIN; I_{OH} = -32mA	2.0			V
V_{OL}	Low-level output voltage	AO0 – AO8[3]	V_{CC} = MIN; I_{OL} = 16mA			0.4	V
			V_{CC} = MIN; I_{OL} = 32mA			0.5	V
		$\overline{B0} - \overline{B8}$	V_{CC} = MIN, I_{OL} = 4mA	0.5			V
			V_{CC} = MIN, I_{OL} = 100mA	0.75	1.0	1.20	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK} = –18mA		0.85	-1.2	V
I_I	Input leakage current	Control pins	V_{CC} = 3.6V; V_I = V_{CC} or GND			±1.0	µA
		Control/ AI0 – AI8	V_{CC} = 0V or 3.6V; V_I = 5.5V			10	
		AI0 – AI8	V_{CC} = 3.6V; V_I = V_{CC}			1	
		Note 4	V_{CC} = 3.6V; V_I = 0V			–5	
I_{IH}	High-level input current	$\overline{B0} - \overline{B8}$	V_{CC} = MAX, V_I = 1.9V			100	µA
	High-level input current	$\overline{B0} - \overline{B8}$	V_{CC} = MAX, V_I = 3.5V, note 5	100			mA
I_{IL}	Low-level input current	$\overline{B0} - \overline{B8}$	V_{CC} = MAX, V_I = 0.75V			-100	µA
I_{OZH}	Off-state output current	AO0 – AO8	V_{CC} = MAX, V_O =3V			5	µA
I_{OZL}	Off-state output current	AO0 – AO8	V_{CC} = MAX, V_O = 0.5V			-5	µA
I_{CC}	Supply current (total)	I_{CCZ} (standby)	V_{CC} = MAX		1.5	2.0	mA
		I_{CCB}, AIn to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		1.3	1.7	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs Low		10	13	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs High		10	13	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
4. Unused pins are at V_{CC} or GND.
5. For B port input voltage between 3 and 5 volt; I_{IH} will be greater than 100mA but the part will continue to function normally (clamping circuit is active).

AC ELECTRICAL CHARACTERISTICS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to +70°C, V_{CC} = 3.3V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 4	120	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay (thru mode) $\overline{Bn}$ to An	Waveform 1, 2	2.5 2.4	4.4 4.2	5.9 5.5	2.3 2.4	6.6 5.9	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) $\overline{Bn}$ to An	Waveform 1, 2	2.9 2.8	4.6 4.3	6.2 5.9	2.7 2.5	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay LCBA to An	Waveform 1, 2	2.6 2.4	4.1 4.7	5.5 6.1	2.0 2.0	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay SEL0 or SEL1 to An	Waveform 1, 2	1.5 1.7	3.8 3.9	5.2 6.0	1.2 1.5	6.0 6.5	ns
t_{PZH} t_{PZL}	Output enable time from High or Low OEA to An	Waveform 5, 6	2.1 2.0	3.5 3.8	4.8 5.3	1.8 1.7	5.8 6.0	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low OEA to An	Waveform 5, 6	1.9 1.7	3.4 3.2	4.8 4.8	1.6 1.5	5.4 5.4	ns
t_{TLH} t_{THL}	Output transition time, An Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				2.0 1.0	7.5 3.5	ns
$t_{SK(o)}$	Output to output skew for multiple channels[1]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK(p)}$	Pulse skew[2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.5	1.0		1.0	ns

NOTES:
1. $\lvert t_{PN}$actual – t_{PM}actual $\rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC ELECTRICAL CHARACTERISTICS (Commercial)

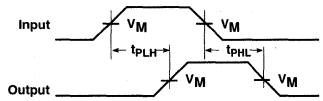
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V, C_D = 30pF, R_U = 16.5Ω			T_{amb} = 0 to +70°C, V_{CC} = 3.3V±10%, C_D = 30pF, R_U = 16.5Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay (thru mode) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.0 2.7	5.0 4.0	1.0 0.5	5.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.2 3.1	5.0 4.2	1.0 0.8	5.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	4.0 4.0	5.5 5.5	1.5 1.0	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay SEL0 or SEL1 to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	3.5 2.3	5.5 4.5	2.0 1.0	6.0 5.0	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.5 1.5	3.0 2.4	5.0 4.5	1.0 0.8	5.5 5.5	ns
t_{TLH} t_{THL}	Output transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.6		2.0 3.0	1.0 0.6	2.3 2.3	ns
$t_{SK(o)}$	Output to output skew for multiple channels[1]	Waveform 3		0.4	1.0		1.6	ns
$t_{SK(p)}$	Pulse skew[2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:
1. $\lvert t_{PN}$actual – t_{PM}actual $\rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

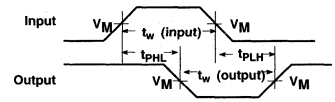
AC SETUP REQUIREMENTS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V,			T_{amb} = 0 to +70°C, V_{CC} = 3.3V±10%,		
			C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 16.5Ω (B side)					
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time An to LCAB	Waveform 4	1.0 1.0			1.5 1.0		ns
t_h(H) t_h(L)	Hold time An to LCAB	Waveform 4	1.0 1.0			2.0 1.0		ns
t_s(H) t_s(L)	Setup time $\overline{Bn}$ to LCBA	Waveform 4	2.0 2.0			3.0 3.0		ns
t_h(H) t_h(L)	Hold time $\overline{Bn}$ to LCBA	Waveform 4	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			3.0 3.0		ns

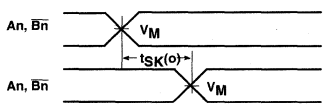
AC WAVEFORMS



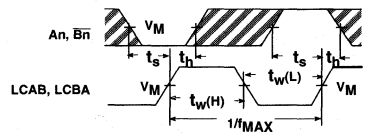
Waveform 1. Propagation Delay for Data or Output Enable to Output



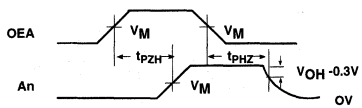
Waveform 2. Propagation Delay for Data or Output Enable to Output



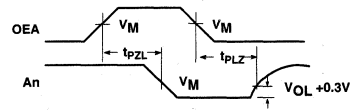
Waveform 3. Output to Output Skew



Waveform 4. Setup and Hold Times, Pulse Widths and Maximum Frequency



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

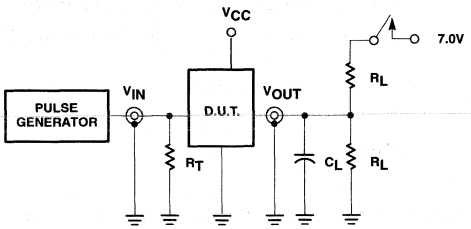


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.
The shaded areas indicate when the input is permitted to change for predictable output performance.

SG00062

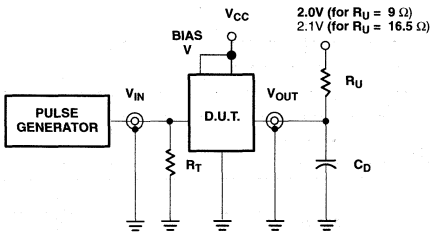
TEST CIRCUIT AND WAVEFORMS



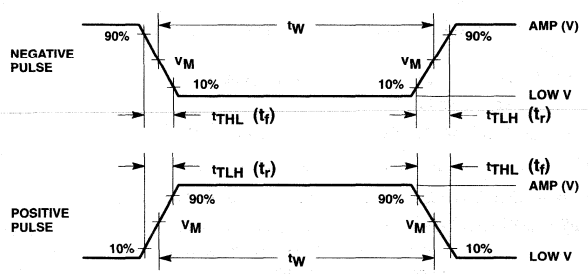
Test Circuit for 3-State Outputs on A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL} All other	closed open



Test Circuit for Outputs on B Port



V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

SG00063

3.3V BTL 8-bit latched/registered/pass-thru Futurebus+ universal interface transceiver

FBL2033

FEATURES

- 8-bit transceivers
- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL Open Collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port

QUICK REFERENCE DATA

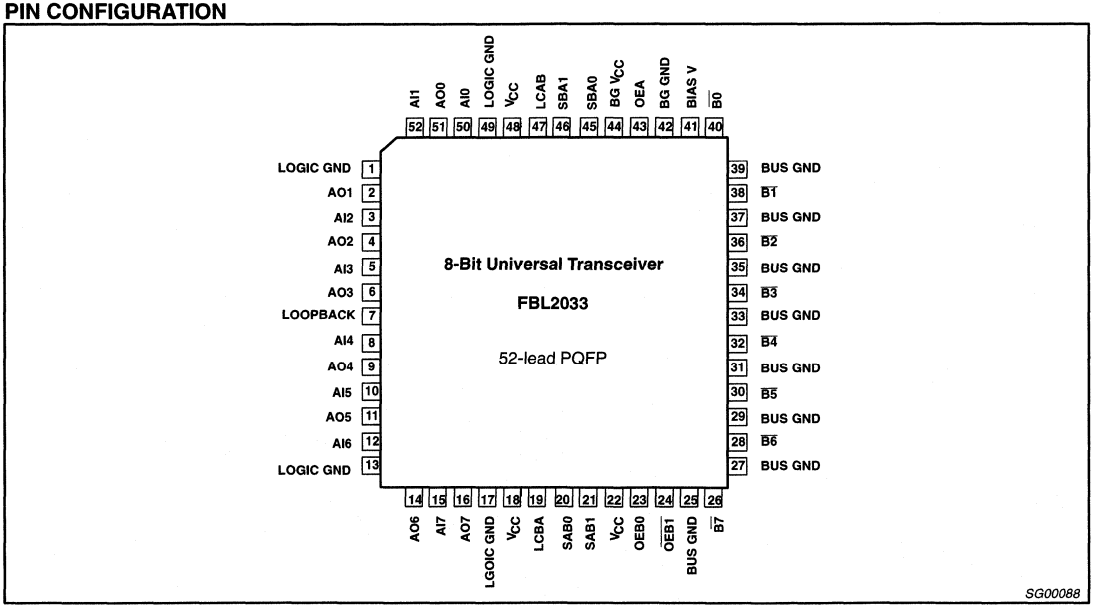
SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		3.0 3.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		4.3 4.1	ns
C_{OB}	Output capacitance ($\overline{B0}$ – $\overline{Bn}$ only)		6	pF
I_{OL}	Output current ($\overline{B0}$ – $\overline{Bn}$ only)		100	mA
I_{CC}	Supply current	AIn to $\overline{Bn}$ (outputs Low or High)	24	mA
		$\overline{Bn}$ to AOn (outputs Low)	45	
		$\overline{Bn}$ to AOn (outputs High)	22	

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 3.3V±10%; T_{amb} = 0°C to +70°C	DWG No.
52-pin Plastic Quad Flat Pack (PQFP)	FBL2033BB	SOT379-1

NOTE: Thermal mounting or forced air is recommended

PIN CONFIGURATION



3.3V BTL 8-bit latched/registered/pass-thru Futurebus+ universal interface transceiver

FBL2033

DESCRIPTION

The FBL2033 is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level side.

The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two pairs of mode select inputs (SBA0 and SBA1 for B-to-A, SAB0 and SAB1 for A-to-B). It can be configured as a buffer, a register, or a D-type latch.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-High latch enables. Regardless of the mode, data is inverted from input to output.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the Loopback input. When the Loopback input is High the output of the selected A-to-B logic element (not inverted) becomes the B-to-A input.

The 3-State AO port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and $\overline{OEB1}$. Only when OEB0 is High and $\overline{OEB1}$ is Low is the output enabled. When either OEB0 is Low or $\overline{OEB1}$ is High, the B-port is inactive and is pulled to the level of the pull-up voltage. New data can be entered in the flip-flop and latched modes or can be retained while the associated outputs are in 3-State (AO port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port ensure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The "V_{OH}" clamp reduces inductive ringing effects during a Low-to-High transition. The "V_{OH}" clamp is always active. The other clamp, the "trapped reflection" clamp, clamps out ringing below the BTL 0.5V V_{OL} level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to ensure glitch- free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble- shoot.

As with any high power device thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI7	50, 52, 3, 5, 8, 10, 12, 15	Input	Data inputs (TTL)
AO0 – AO7	51, 2, 4, 6, 9, 11, 14, 16	Output	3-State outputs (TTL)
$\overline{B0}$ – $\overline{B7}$	40, 38, 36, 34, 32, 30, 28, 26	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	23	Input	Enables the B outputs when High
$\overline{OEB1}$	24	Input	Enables the B outputs when Low
OEA	43	Input	Enables the AO outputs when High
BUS GND	39, 37, 35, 33, 31, 29, 27, 25	GND	Bus ground (0V)
LOGIC GND	1, 13, 17, 49	GND	Logic ground (0V)
V_{CC}	18, 22, 48	Power	Positive supply voltage
BIAS V	41	Power	Live insertion pre-bias pin
BG V_{CC}	44	Power	Band Gap threshold voltage reference
BG GND	42	GND	Band Gap threshold voltage reference ground
SABn	20, 21	Input	Mode select from AI to $\overline{B}$
SBAn	45, 46	Input	Mode select from $\overline{B}$ to AO
LCAB	47	Input	A-to-B clock/latch enable (transparent latch when High)
LCBA	19	Input	B-to-A clock/latch enable (transparent latch when High)
Loopback	7	Input	Enables loopback function when High (from AIn to AOn)

FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	OEA	LCAB	LCBA	$SAB_{1\ 0}$	$SBA_{1\ 0}$	AOn	$\overline{Bn}$
AIn to $\overline{Bn}$ thru mode	L	—	H	L	L	X	X	LL	XX	Z	H**
	H	—	H	L	L	X	X	LL	XX	Z	L
AIn to $\overline{Bn}$ transparent latch	L	—	H	L	L	H	X	HX	XX	Z	H**
	H	—	H	L	L	H	X	HX	XX	Z	L
AIn to $\overline{Bn}$ latch and read	l	—	H	L	L	↓	X	HX	XX	Z	H**
	h	—	H	L	L	↓	X	HX	XX	Z	L
AIn to $\overline{Bn}$ register	L	—	H	L	L	↑	X	LH	XX	Z	H**
	H	—	H	L	L	↑	X	LH	XX	Z	L
$\overline{Bn}$ outputs latched and read (preconditioned latch)	X	—	H	L	L	L	X	HX	XX	Z	latched data
$\overline{Bn}$ to AOn thru mode	X	L	L	H	H	X	X	XX	LL	H	input
	X	H	L	H	H	X	X	XX	LL	L	input
$\overline{Bn}$ to AOn transparent latch	X	L	L	H	H	X	H	XX	HX	H	input
	X	H	L	H	H	X	H	XX	HX	L	input
$\overline{Bn}$ to AOn latch and read	X	l	L	H	H	X	↓	XX	HX	H	input
	X	h	L	H	H	X	↓	XX	HX	L	input
$\overline{Bn}$ to AOn register	X	L	L	H	H	X	↑	XX	LH	H	input
	X	H	L	H	H	X	↑	XX	LH	L	input
AOn outputs latched and read (preconditioned latch)	X	X	L	H	H	X	L	XX	HX	latched data	X
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	X	XX	XX	X	H**
	X	X	X	H	X	X	X	XX	XX	X	H**
Disable AOn outputs	X	X	X	X	L	X	X	XX	XX	Z	X

FUNCTION SELECT TABLE

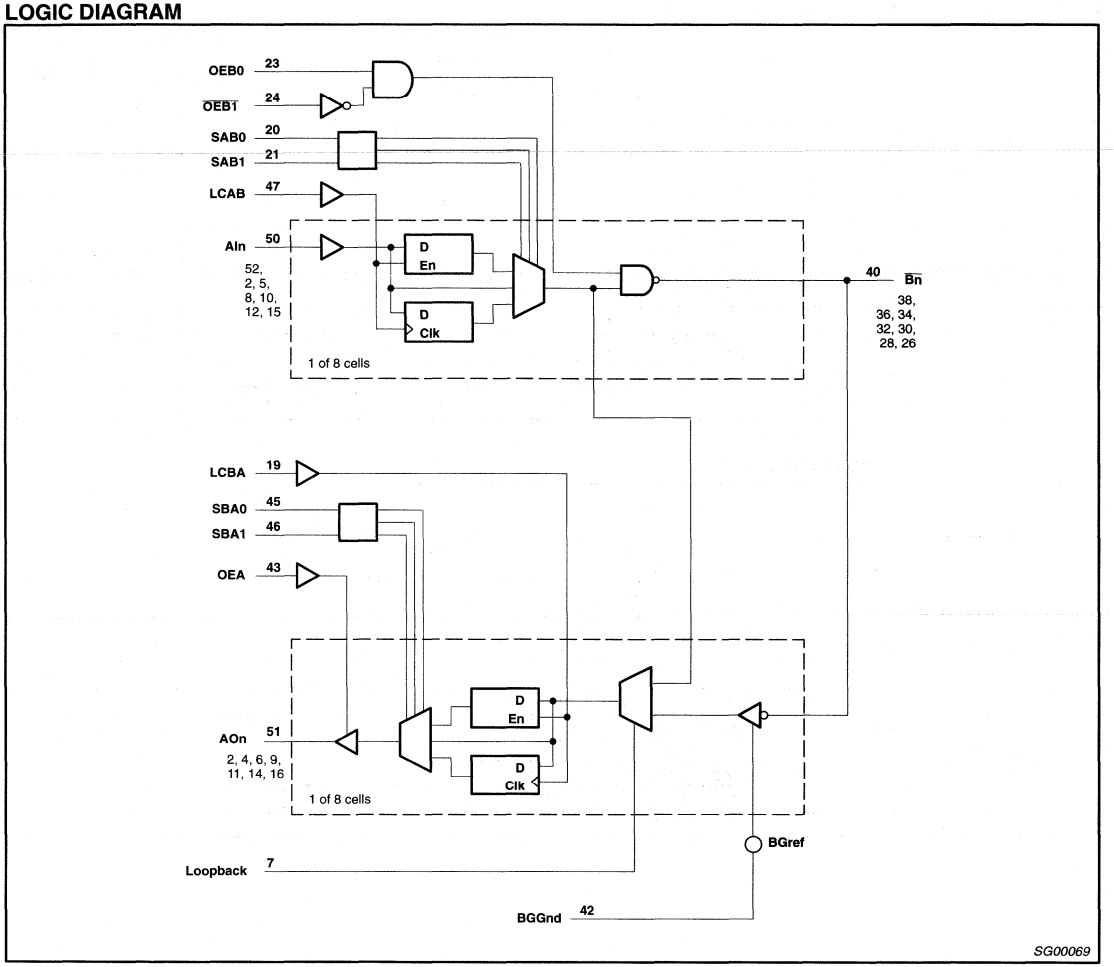
MODE SELECTED	SXX1	SXX0
Thru mode	L	L
Register mode	L	H
Latch mode	H	X

NOTES:

H = High voltage level
L = Low voltage level
h = High voltage level one set-up time prior to the High-to-Low LCXX transition
l = Low voltage level one set-up time prior to the High-to-Low LCXX transition
X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
↑ = Low-to-High transition
↓ = High-to-Low transition
H** = Goes to level of pull-up voltage
$\overline{Bn}$* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

NOTE: In Loopback mode (Loopback = High), AIn inputs are routed to the AOn outputs. The $\overline{Bn}$ inputs are blocked out.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +4.6	V
V_{IN}	Input voltage	AI0 – AI7, OEB0, $\overline{OEBn}$, OEAn	-0.5 to +7.0	V
		$\overline{B0} – \overline{B7}$	-0.5 to +3.5	
I_{IN}	Input current	$V_{IN} < 0$	-50	
V_{OUT}	Voltage applied to output in High output state		-0.5 to +7.0	V
I_{OUT}	Current applied to output in Low output state/High output state	AO0 – AO7	128, –64	mA
		$\overline{B0} – \overline{B7}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		COMMERCIAL LIMITS V_{CC} = 3.3V±10%; T_{amb} = 0 to +70°C			INDUSTRIAL LIMITS V_{CC} = 3.3V±10%; T_{amb} = -40 to +85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		3.0	3.3	3.6	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	Except $\overline{B0}$–$\overline{B7}$	2.0			2.0			V
		$\overline{B0}$ – $\overline{B7}$	1.62	1.55		1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}$–$\overline{B7}$			0.8			0.8	V
		$\overline{B0}$ – $\overline{B7}$			1.47			1.47	
I_{IK}	Input clamp current				-18			-18	mA
I_{OH}	High-level output current	AO0 – AO7			-12			-12	mA
I_{OL}	Low-level output current	AO0 – AO7			+12			+12	mA
		$\overline{B0}$ – $\overline{B7}$			100			100	
C_{OB}	Output capacitance on B port			6	7		6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	-40		+85	°C

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
V_{BIASV}	Bias pin voltage	Voltage difference between the Bias voltage and V_{CC} after the PCB is plugged in.	–	–	0.5	V
I_{BIASV}	Bias pin (I_{BIASV}) input DC current	V_{CC} = 0 V, Bias V = 3.6V			1.2	mA
		V_{CC} = 3.3V, Bias V = 3.6V			10	µA
$V_{\overline{Bn}}$	Bus voltage during prebias	$\overline{B0}$ – $\overline{B7}$ = 0V, Bias V = 3.3V	1.62		2.1	V
I_{LM}	Fall current during prebias	$\overline{B0}$ – $\overline{B7}$ = 2V, Bias V = 1.3 to 2.5V			1	µA
I_{HM}	Rise current during prebias	$\overline{B0}$ – $\overline{B7}$ = 1V, Bias V = 3 to 3.6V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 3.3V, $\overline{B0}$ – $\overline{B7}$ = 0 to 2.0V, Bias V = 2.7 to 3.6V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 3.3V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 1.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 3.3V	1.0	1.35		ns

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	UNIT
I_{OH}	High level output current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = 0V, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	AO0 – AO7[3]	V_{CC} = MIN to MAX; I_{OH} = -100µA	V_{CC} –0.2			V
			V_{CC} = MIN; I_{OH} = -8mA	2.4			V
			V_{CC} = MIN; I_{OH} = -32mA	2.0			V
V_{OL}	Low-level output voltage	AO0 – AO7[3]	V_{CC} = MIN; I_{OL} = 16mA			0.4	V
			V_{CC} = MIN; I_{OL} = 32mA			0.5	V
		$\overline{B0}$ – $\overline{B7}$	V_{CC} = MIN, I_{OL} = 4mA	0.5			V
			V_{CC} = MIN, I_{OL} = 100mA	0.75	1.0	1.20	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK} = –18mA		–0.85	-1.2	V
I_I	Input leakage current	Control pins	V_{CC} = 3.6V; V_I = V_{CC} or GND			±1.0	µA
		Control/ AI0 – AI7	V_{CC} = 0V or 3.6V; V_I = 5.5V			10	
		AI0 – AI7	V_{CC} = 3.6V; V_I = V_{CC}			1	
		Note 4	V_{CC} = 3.6V; V_I = 0V			–5	
I_{IH}	High-level input current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 1.9V			100	µA
I_{IH}	High-level input current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 3.5V, note 5	100			mA
I_{IL}	Low-level input current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 0.75V			-100	µA
I_{OZH}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O =3V			5	µA
I_{OZL}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O = 0.5V			-5	µA
I_{CC}	Supply current (total)	I_{CCZ}	V_{CC} = MAX		5.2	13.5	mA
		I_{CCB}	V_{CC} = MAX, outputs Low or High		3.2	9.0	
		I_{CCL} A3	V_{CC} = MAX, outputs Low		13.5	19.5	
		I_{CCH} A5	V_{CC} = MAX, outputs High		10.7	16.0	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
4. Unused pins are at V_{CC} or GND.
5. For B port input voltage between 3 and 5 volt; I_{IH} will be greater than 100mA but the part will continue to function normally (clamping circuit is active).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 4	100	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay (thru mode) $\overline{Bn}$ to AOn	Waveform 1, 2	2.2 2.0	4.3 4.1	6.0 6.0	2.0 1.8	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) $\overline{Bn}$ to AOn	Waveform 1, 2	1.5 2.4	4.5 4.4	6.5 6.5	1.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay LCBA to AOn	Waveform 1, 2	2.0 2.2	3.8 4.3	5.5 6.0	1.8 1.7	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay SBAn to AOn	Waveform 1, 2	1.4 1.4	2.9 3.1	5.0 5.5	1.0 1.0	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay (Loopback mode) AIn to AOn	Waveform 1, 2	2.0 2.0	3.8 3.9	6.0 6.0	2.8 2.3	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay (Loopback mode) Loopback to AOn	Waveform 1, 2	1.2 1.2	3.4 3.2	5.0 5.5	1.0 1.0	6.0 6.5	ns
t_{PZH} t_{PZL}	Output enable time from High or Low OEA to AOn	Waveform 5, 6	1.0 2.6	3.1 4.0	5.1 5.5	1.0 2.4	5.5 5.8	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low OEA to AOn	Waveform 5, 6	1.0 1.0	3.5 3.3	5.0 4.6	1.7 1.7	5.6 5.2	ns
t_{TLH} t_{THL}	Output transition time, AOn Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				2.0 2.0	5.0 5.0	ns
$t_{SK}(o)$	Output to output skew, A port[2]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK}(p)$	Pulse skew[1] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:

1. $\lvert t_{PN}\text{actual} - t_{PM}\text{actual} \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay (thru mode) AIn to $\overline{Bn}$	Waveform 1, 2	1.2 1.0	2.9 2.9	4.3 4.4	1.0 1.0	4.8 4.6	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) AIn to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.1 3.3	4.5 4.8	1.0 1.0	5.1 5.1	ns
t_{PLH} t_{PHL}	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.7 2.2	4.4 5.1	5.7 6.6	2.4 2.0	6.4 7.1	ns
t_{PLH} t_{PHL}	Propagation delay SABn to $\overline{Bn}$	Waveform 1, 2	1.8 1.0	3.6 3.3	5.0 4.9	1.4 1.0	5.7 5.2	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.0 3.1	4.5 5.0	1.0 1.0	5.0 5.6	ns
$\Delta V/\Delta t$	Output transition rate, $\overline{Bn}$ Port 20% to 80%, 80% to 20%	Test Circuit and Waveforms				0.4	1.2	V/ns
$t_{SK}(o)$	Output to output skew, B port [1]	Waveform 3		0.8	1.5		2.0	ns
$t_{SK}(p)$	Pulse skew 2 $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.5			ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**R_U = 16.5Ω**			**R_U = 16.5Ω**		**UNIT**
t_{PLH} t_{PHL}	Propagation delay (thru mode) AIn to $\overline{Bn}$	Waveform 1, 2	1.2 1.0	3.0 3.0	4.4 4.5	1.0 1.0	4.9 4.7	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) AIn to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.2 3.4	4.6 4.9	1.0 1.0	5.2 5.2	ns
t_{PLH} t_{PHL}	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.7 2.2	4.5 5.2	5.8 6.7	2.4 2.0	6.5 7.2	ns
t_{PLH} t_{PHL}	Propagation delay SABn to $\overline{Bn}$	Waveform 1, 2	1.8 1.0	3.7 3.4	5.1 5.0	1.4 1.0	5.8 5.3	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.1 3.2	4.6 5.1	1.0 1.0	5.1 5.7	ns
$\Delta V/\Delta t$	Output transition rate, $\overline{Bn}$ Port 20% to 80%, 80% to 20%	Test Circuit and Waveforms				0.2	0.6	V/ns
$t_{SK}(o)$	Output to output skew, B port[1]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK}(p)$	Pulse skew[2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

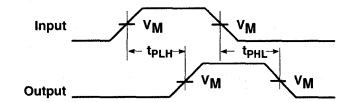
NOTES:

1. $\lvert t_{PN}actual - t_{PM}actual \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

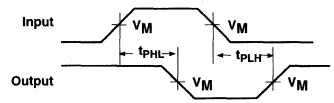
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%		
			C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 9Ω (B side)					
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	1.0 1.0			1.3 1.3		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
SYMBOL	PARAMETER	TEST CONDITION	C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 16.5Ω (B side)					UNIT
$t_s(H)$ $t_s(L)$	Setup time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	1.0 1.0			1.3 1.3		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns

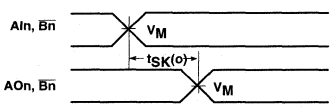
AC WAVEFORMS



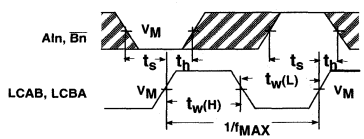
Waveform 1. Propagation Delay for Data or Output Enable to Output



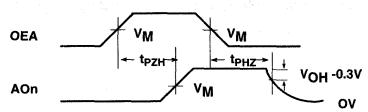
Waveform 2. Propagation Delay for Data or Output Enable to Output



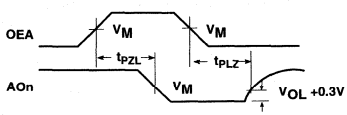
Waveform 3. Output to Output Skew



Waveform 4. Setup and Hold Times, Pulse Widths and Maximum Frequency



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

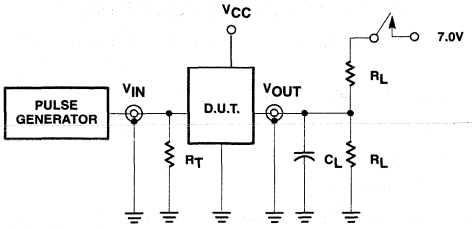


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

SG00070

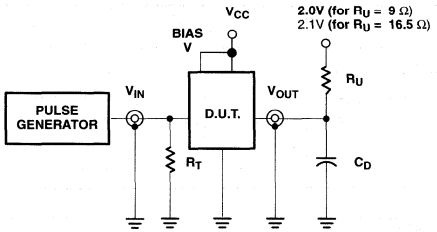
TEST CIRCUIT AND WAVEFORMS



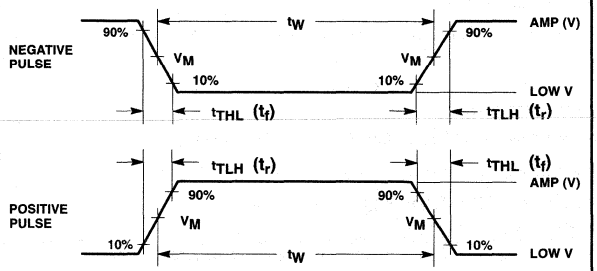
Test Circuit for 3-State Outputs on A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit for Outputs on B Port



V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

SG00063

3.3V BTL 8-bit latched/registered/pass-thru Futurebus+ universal interface transceiver

FBL22033

FEATURES

- 8-bit transceivers
- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL Open Collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port

QUICK REFERENCE DATA

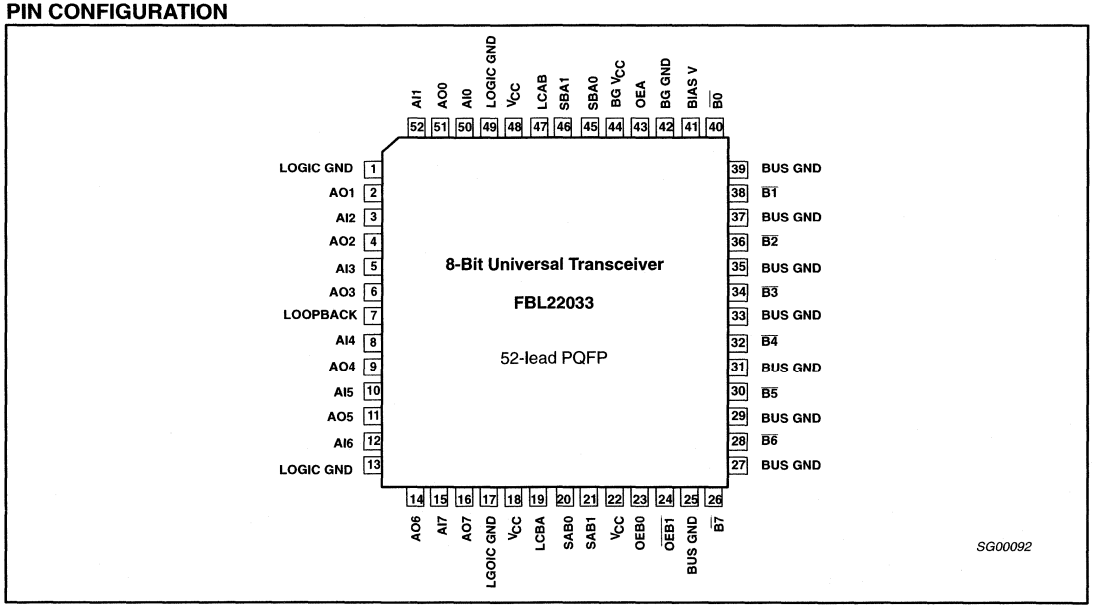
SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		3.0 3.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		4.3 4.1	ns
C_{OB}	Output capacitance ($\overline{B0}$ – $\overline{Bn}$ only)		6	pF
I_{OL}	Output current ($\overline{B0}$ – $\overline{Bn}$ only)		100	mA
I_{CC}	Supply current	AIn to $\overline{Bn}$ (outputs Low or High)	24	mA
		$\overline{Bn}$ to AOn (outputs Low)	45	
		$\overline{Bn}$ to AOn (outputs High)	22	

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 3.3V±10%; T_{amb} = 0°C to +70°C	DWG No.
52-pin Plastic Quad Flat Pack (PQFP)	FBL2033BB	SOT379-1

NOTE: Thermal mounting or forced air is recommended

PIN CONFIGURATION



3.3V BTL 8-bit latched/registered/pass-thru Futurebus+ universal interface transceiver

FBL22033

DESCRIPTION

The FBL22033 is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level side.

The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two pairs of mode select inputs (SBA0 and SBA1 for B-to-A, SAB0 and SAB1 for A-to-B). It can be configured as a buffer, a register, or a D-type latch.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-High latch enables. Regardless of the mode, data is inverted from input to output.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the Loopback input. When the Loopback input is High the output of the selected A-to-B logic element (not inverted) becomes the B-to-A input.

The 3-State AO port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and $\overline{OEB1}$. Only when OEB0 is High and $\overline{OEB1}$ is Low is the output enabled. When either OEB0 is Low or $\overline{OEB1}$ is High, the B-port is inactive and is pulled to the level of the pull-up voltage. New data can be entered in the flip-flop and latched modes or can be retained while the associated outputs are in 3-State (AO port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port ensure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The "V_{OH}" clamp reduces inductive ringing effects during a Low-to-High transition. The "V_{OH}" clamp is always active. The other clamp, the "trapped reflection" clamp, clamps out ringing below the BTL 0.5V V_{OL} level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to ensure glitch- free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble- shoot.

As with any high power device thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI7	50, 52, 3, 5, 8, 10, 12, 15	Input	Data inputs (TTL)
AO0 – AO7	51, 2, 4, 6, 9, 11, 14, 16	Output	3-State outputs (TTL)
$\overline{B0}$ – $\overline{B7}$	40, 38, 36, 34, 32, 30, 28, 26	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	23	Input	Enables the B outputs when High
$\overline{OEB1}$	24	Input	Enables the B outputs when Low
OEA	43	Input	Enables the AO outputs when High
BUS GND	39, 37, 35, 33, 31, 29, 27, 25	GND	Bus ground (0V)
LOGIC GND	1, 13, 17, 49	GND	Logic ground (0V)
V_{CC}	18, 22, 48	Power	Positive supply voltage
BIAS V	41	Power	Live insertion pre-bias pin
BG V_{CC}	44	Power	Band Gap threshold voltage reference
BG GND	42	GND	Band Gap threshold voltage reference ground
SABn	20, 21	Input	Mode select from AI to $\overline{B}$
SBAn	45, 46	Input	Mode select from $\overline{B}$ to AO
LCAB	47	Input	A-to-B clock/latch enable (transparent latch when High)
LCBA	19	Input	B-to-A clock/latch enable (transparent latch when High)
Loopback	7	Input	Enables loopback function when High (from AIn to AOn)

FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	OEA	LCAB	LCBA	$SAB_{1\ 0}$	$SBA_{1\ 0}$	AOn	$\overline{Bn}$
AIn to $\overline{Bn}$ thru mode	L	—	H	L	L	X	X	LL	XX	Z	H**
	H	—	H	L	L	X	X	LL	XX	Z	L
AIn to $\overline{Bn}$ transparent latch	L	—	H	L	L	H	X	HX	XX	Z	H**
	H	—	H	L	L	H	X	HX	XX	Z	L
AIn to $\overline{Bn}$ latch and read	l	—	H	L	L	↓	X	HX	XX	Z	H**
	h	—	H	L	L	↓	X	HX	XX	Z	L
AIn to $\overline{Bn}$ register	L	—	H	L	L	↑	X	LH	XX	Z	H**
	H	—	H	L	L	↑	X	LH	XX	Z	L
$\overline{Bn}$ outputs latched and read (preconditioned latch)	X	—	H	L	L	L	X	HX	XX	Z	latched data
$\overline{Bn}$ to AOn thru mode	X	L	L	H	H	X	X	XX	LL	H	input
	X	H	L	H	H	X	X	XX	LL	L	input
$\overline{Bn}$ to AOn transparent latch	X	L	L	H	H	X	H	XX	HX	H	input
	X	H	L	H	H	X	H	XX	HX	L	input
$\overline{Bn}$ to AOn latch and read	X	l	L	H	H	X	↓	XX	HX	H	input
	X	h	L	H	H	X	↓	XX	HX	L	input
$\overline{Bn}$ to AOn register	X	L	L	H	H	X	↑	XX	LH	H	input
	X	H	L	H	H	X	↑	XX	LH	L	input
AOn outputs latched and read (preconditioned latch)	X	X	L	H	H	X	L	XX	HX	latched data	X
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	X	XX	XX	X	H**
	X	X	X	H	X	X	X	XX	XX	X	H**
Disable AOn outputs	X	X	X	X	L	X	X	XX	XX	Z	X

FUNCTION SELECT TABLE

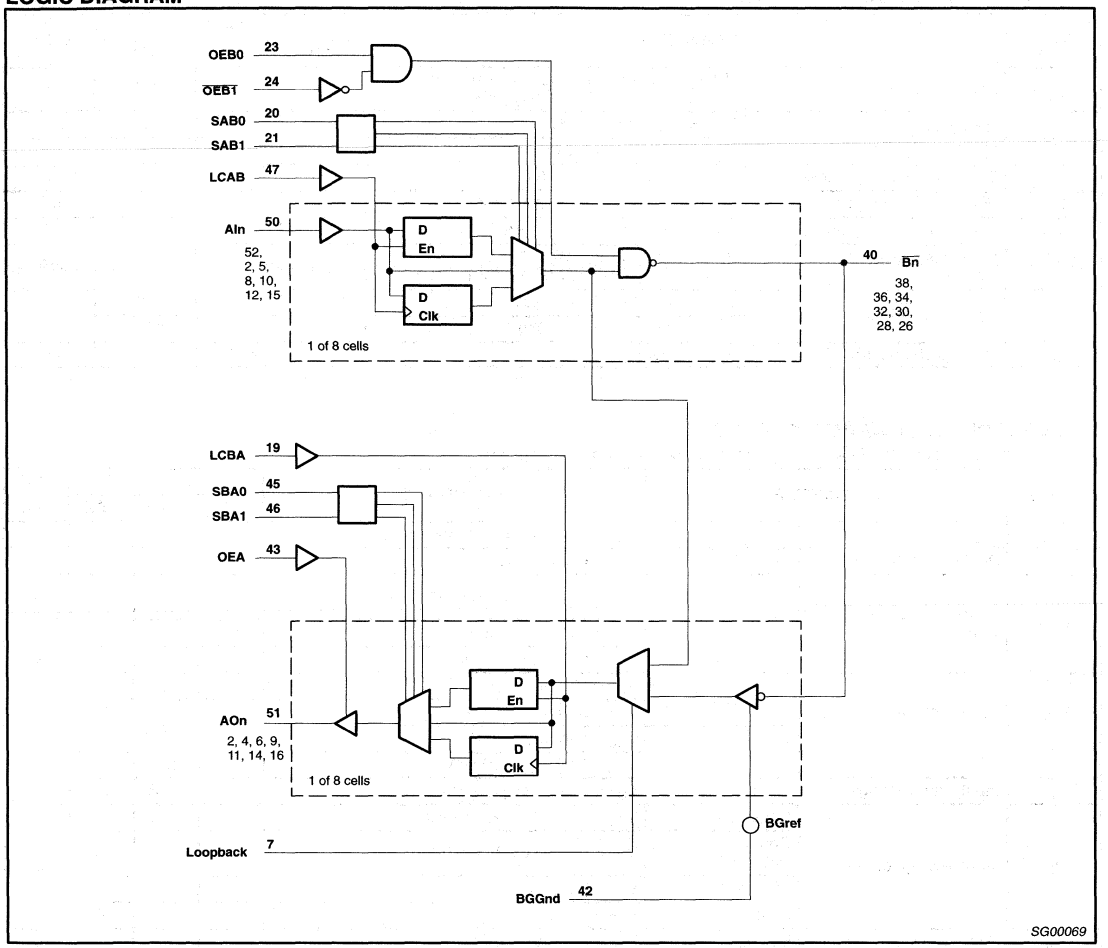
MODE SELECTED	SXX1	SXX0
Thru mode	L	L
Register mode	L	H
Latch mode	H	X

NOTES:

H = High voltage level
L = Low voltage level
h = High voltage level one set-up time prior to the High-to-Low LCXX transition
l = Low voltage level one set-up time prior to the High-to-Low LCXX transition
X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
↑ = Low-to-High transition
↓ = High-to-Low transition
H** = Goes to level of pull-up voltage
$\overline{Bn}$* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

NOTE: In Loopback mode (Loopback = High), AIn inputs are routed to the AOn outputs. The $\overline{Bn}$ inputs are blocked out.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +4.6	V
V_{IN}	Input voltage	AI0 – AI7, OEB0, $\overline{OEBn}$, OEAn	-0.5 to +7.0	V
		$\overline{B0} – \overline{B7}$	-0.5 to +3.5	
I_{IN}	Input current	$V_{IN} < 0$	-50	
V_{OUT}	Voltage applied to output in High output state		-0.5 to +7.0	V
I_{OUT}	Current applied to output in	AO0 – AO7	–48, 48	mA
	Low output state/High output state	$\overline{B0} – \overline{B7}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
V_{BIASV}	Bias pin voltage	Voltage difference between the Bias voltage and V_{CC} after the PCB is plugged in.	–	–	0.5	V
I_{BIASV}	Bias pin (I_{BIASV}) input DC current	V_{CC} = 0 V, Bias V = 3.6V			1.2	mA
		V_{CC} = 3.3V, Bias V = 3.6V			10	µA
$V_{\overline{Bn}}$	Bus voltage during prebias	$\overline{B0}$ – $\overline{B7}$ = 0V, Bias V = 3.3V	1.62		2.1	V
I_{LM}	Fall current during prebias	$\overline{B0}$ – $\overline{B7}$ = 2V, Bias V = 1.3 to 2.5V			1	µA
I_{HM}	Rise current during prebias	$\overline{B0}$ – $\overline{B7}$ = 1V, Bias V = 3 to 3.6V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 3.3V, $\overline{B0}$ – $\overline{B7}$ = 0 to 2.0V, Bias V = 2.7 to 3.6V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 3.3V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 1.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 3.3V	1.0	1.35		ns

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	UNIT
I_{OH}	High level output current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = 0V, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	AO0 – AO7[3]	V_{CC} = MIN to MAX; I_{OH} = -100µA	V_{CC} –0.2			V
			V_{CC} = MIN; I_{OH} = -8mA	2.4			V
			V_{CC} = MIN; I_{OH} = -32mA	2.0			V
V_{OL}	Low-level output voltage	AO0 – AO7[3]	V_{CC} = MIN; I_{OL} = 16mA			0.4	V
			V_{CC} = MIN; I_{OL} = 32mA			0.5	V
		$\overline{B0}$ – $\overline{B7}$	V_{CC} = MIN, I_{OL} = 4mA	0.5			V
			V_{CC} = MIN, I_{OL} = 100mA	0.75	1.0	1.20	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK} = –18mA		–0.85	-1.2	V
I_I	Input leakage current	Control pins	V_{CC} = 3.6V; V_I = V_{CC} or GND			±1.0	µA
		Control/ AI0 – AI7	V_{CC} = 0V or 3.6V; V_I = 5.5V			10	
		AI0 – AI7	V_{CC} = 3.6V; V_I = V_{CC}			1	
		Note 4	V_{CC} = 3.6V; V_I = 0V			–5	
I_{IH}	High-level input current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 1.9V			100	µA
I_{IH}	High-level input current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 3.5V, note 5	100			mA
I_{IL}	Low-level input current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 0.75V			-100	µA
I_{OZH}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O =3V			5	µA
I_{OZL}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O = 0.5V			-5	µA
I_{CC}	Supply current (total)	I_{CCZ}	V_{CC} = MAX		5.2	13.5	mA
		I_{CCB}	V_{CC} = MAX, outputs Low or High		3.2	9.0	
		I_{CCL} A3	V_{CC} = MAX, outputs Low		13.5	19.5	
		I_{CCH} A5	V_{CC} = MAX, outputs High		10.7	16.0	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
4. Unused pins are at V_{CC} or GND.
5. For B port input voltage between 3 and 5 volt; I_{IH} will be greater than 100mA but the part will continue to function normally (clamping circuit is active).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 4	100	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay (thru mode) $\overline{Bn}$ to AOn	Waveform 1, 2	2.2 2.0	4.3 4.1	6.0 6.0	2.0 1.8	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) $\overline{Bn}$ to AOn	Waveform 1, 2	1.5 2.4	4.5 4.4	6.5 6.5	1.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay LCBA to AOn	Waveform 1, 2	2.0 2.2	3.8 4.3	5.5 6.0	1.8 1.7	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay SBAn to AOn	Waveform 1, 2	1.4 1.4	2.9 3.1	5.0 5.5	1.0 1.0	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay (Loopback mode) AIn to AOn	Waveform 1, 2	2.0 2.0	3.8 3.9	6.0 6.0	2.8 2.3	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay (Loopback mode) Loopback to AOn	Waveform 1, 2	1.2 1.2	3.4 3.2	5.0 5.5	1.0 1.0	6.0 6.5	ns
t_{PZH} t_{PZL}	Output enable time from High or Low OEA to AOn	Waveform 5, 6	1.0 2.6	3.1 4.0	5.1 5.5	1.0 2.4	5.5 5.8	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low OEA to AOn	Waveform 5, 6	1.0 1.0	3.5 3.3	5.0 4.6	1.7 1.7	5.6 5.2	ns
t_{TLH} t_{THL}	Output transition time, AOn Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				2.0 2.0	5.0 5.0	ns
$t_{SK}(o)$	Output to output skew, A port[2]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK}(p)$	Pulse skew[1] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:

1. $\lvert t_{PN}\text{actual} - t_{PM}\text{actual} \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay (thru mode) AIn to $\overline{Bn}$	Waveform 1, 2	1.2 1.0	2.9 2.9	4.3 4.4	1.0 1.0	4.8 4.6	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) AIn to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.1 3.3	4.5 4.8	1.0 1.0	5.1 5.1	ns
t_{PLH} t_{PHL}	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.7 2.2	4.4 5.1	5.7 6.6	2.4 2.0	6.4 7.1	ns
t_{PLH} t_{PHL}	Propagation delay SABn to $\overline{Bn}$	Waveform 1, 2	1.8 1.0	3.6 3.3	5.0 4.9	1.4 1.0	5.7 5.2	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.0 3.1	4.5 5.0	1.0 1.0	5.0 5.6	ns
$\Delta V/\Delta t$	Output transition rate, $\overline{Bn}$ Port 20% to 80%, 80% to 20%	Test Circuit and Waveforms				0.4	1.2	V/ns
$t_{SK}(o)$	Output to output skew, B port [1]	Waveform 3		0.8	1.5		2.0	ns
$t_{SK}(p)$	Pulse skew 2 $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.5			ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**R_U = 16.5Ω**			**R_U = 16.5Ω**		**UNIT**
t_{PLH} t_{PHL}	Propagation delay (thru mode) AIn to $\overline{Bn}$	Waveform 1, 2	1.2 1.0	3.0 3.0	4.4 4.5	1.0 1.0	4.9 4.7	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) AIn to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.2 3.4	4.6 4.9	1.0 1.0	5.2 5.2	ns
t_{PLH} t_{PHL}	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.7 2.2	4.5 5.2	5.8 6.7	2.4 2.0	6.5 7.2	ns
t_{PLH} t_{PHL}	Propagation delay SABn to $\overline{Bn}$	Waveform 1, 2	1.8 1.0	3.7 3.4	5.1 5.0	1.4 1.0	5.8 5.3	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.1 3.2	4.6 5.1	1.0 1.0	5.1 5.7	ns
$\Delta V/\Delta t$	Output transition rate, $\overline{Bn}$ Port 20% to 80%, 80% to 20%	Test Circuit and Waveforms				0.2	0.6	V/ns
$t_{SK}(o)$	Output to output skew, B port[1]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK}(p)$	Pulse skew[2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

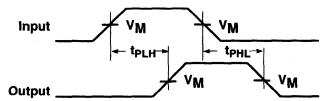
NOTES:

1. $\lvert t_{PN}\text{actual} - t_{PM}\text{actual} \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

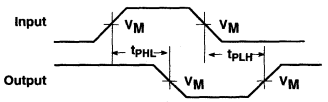
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%		
			C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 9Ω (B side)					
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	1.0 1.0			1.3 1.3		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 16.5Ω (B side)					**UNIT**
$t_s(H)$ $t_s(L)$	Setup time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	1.0 1.0			1.3 1.3		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns

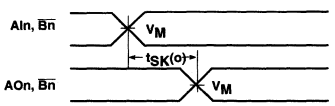
AC WAVEFORMS



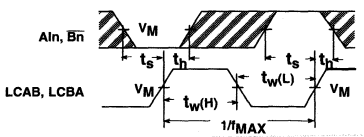
Waveform 1. Propagation Delay for Data or Output Enable to Output



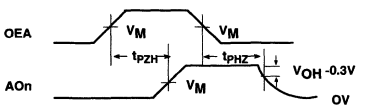
Waveform 2. Propagation Delay for Data or Output Enable to Output



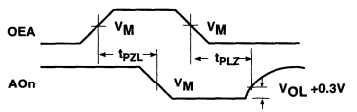
Waveform 3. Output to Output Skew



Waveform 4. Setup and Hold Times, Pulse Widths and Maximum Frequency



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

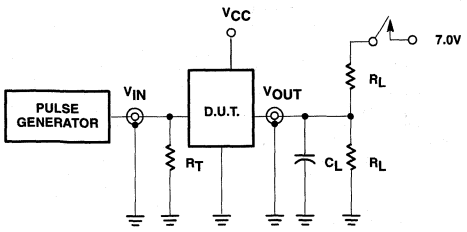


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

SG00070

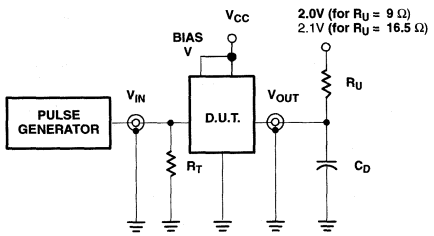
TEST CIRCUIT AND WAVEFORMS



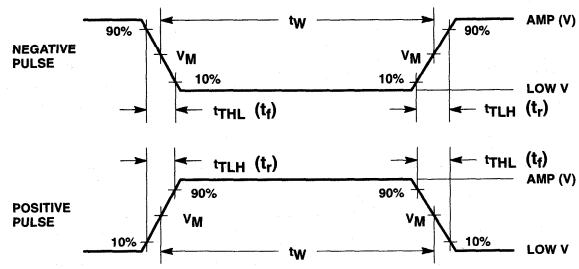
Test Circuit for 3-State Outputs on A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit for Outputs on B Port



V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

SG00063

3.3V BTL 8-bit TTL to BTL transceiver FBL2040

FEATURES

- 3.3V version of FB2040A with 70% power savings
- 8-bit BTL transceivers
- Separate I/O on TTL A-port
- Inverting
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flat Pack

QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		4.4 3.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		3.4 3.2	ns
C_{OB}	Output capacitance ($\overline{B0}$ – $\overline{B7}$ only)		4	pF
I_{OL}	Output current ($\overline{B0}$ – $\overline{B7}$ only)		100	mA
I_{CC}	Supply current	Standby	4	mA
		AIn to $\overline{Bn}$ (outputs Low or High)	4	
		$\overline{Bn}$ to AOn (outputs Low)	22	
		$\overline{Bn}$ to AOn (outputs High)	12	

ORDERING INFORMATION

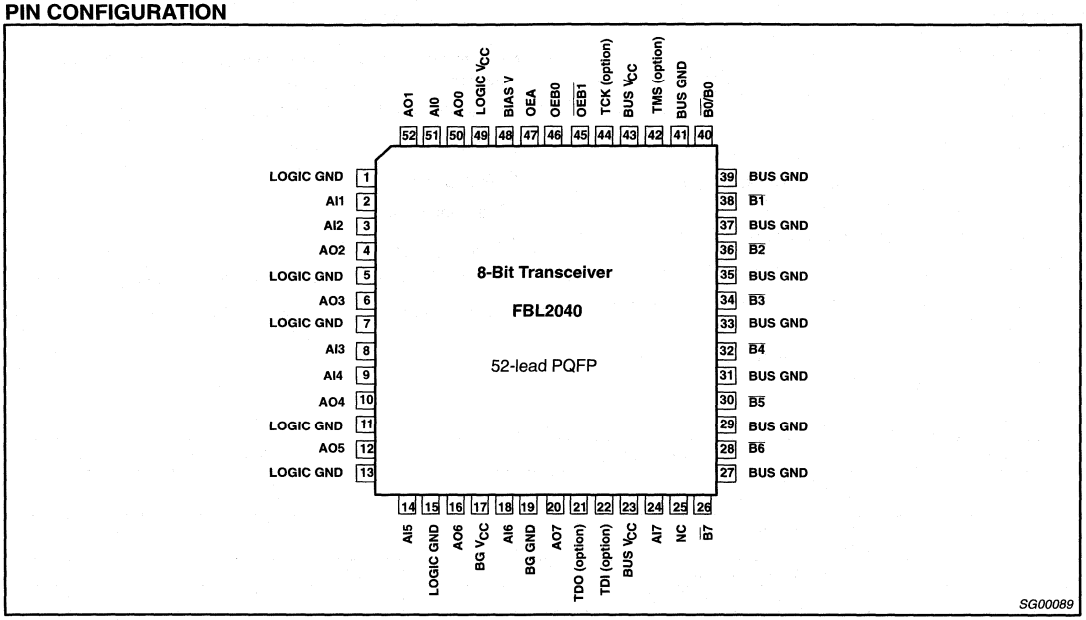
PACKAGES	COMMERCIAL RANGE V_{CC} = 3V±10%; T_{amb} = 0°C to +70°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FBL2040BB	SOT379-1

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +4.6	V
V_{IN}	Input voltage	AI0 – AI7, OEB0, $\overline{OEB1}$, OEA	-0.5 to +7.0	V
		$\overline{B0}$ – $\overline{B7}$	-0.5 to +3.5	
I_{IN}	Input current		-18 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A0 – A7	128	mA
		$\overline{B0}$ – $\overline{B7}$	200	
T_{amb}	Operating free-air temperature range		-40 to ++85	°C
T_{STG}	Storage temperature		-65 to +150	°C

PIN CONFIGURATION



DESCRIPTION

The FBL2040 is an 8-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FBL2040 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEA goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEA goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 1.3V.

The B-port has two output enables, OEB0 and $\overline{OEB1}$. When OEB0 is High and $\overline{OEB1}$ is Low the output is enabled. When OEB0 is Low or if $\overline{OEB1}$ is High, the B-port is inactive and is at the level of the backplane signal.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while V_{CC} is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

The LOGIC V_{CC} and BUS V_{CC} pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

JTAG boundary scan pins are provided with signals TMS, TCK, TDI and TDO. TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally. Boundary scan functionality is not implemented at this time.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI7	51, 2, 3, 8, 9, 14, 18, 24	Input	Data inputs (TTL)
AO0 – AO7	50, 52, 4, 6, 10, 12, 16, 20	Output	3-state outputs (TTL)
$\overline{B0}$ – $\overline{B7}$	40, 38, 36, 34, 32, 30, 28, 26	I/O	Data inputs/Open Collector outputs. High current drive (BTL)
OEB0	46	Input	Enables the B outputs when High
$\overline{OEB1}$	45	Input	Enables the B outputs when Low
OEA	47	Input	Enables the A outputs when High
BUS GND	41, 39, 37, 35, 33, 31, 29, 27	GND	Bus ground (0V)
LOGIC GND	1, 5, 7, 11, 13, 15	GND	Logic ground (0V)
BUS V_{CC}	23, 43	Power	Positive supply voltage
LOGIC V_{CC}	49	Power	Positive supply voltage
BG V_{CC}	17	Power	Band Gap threshold voltage reference
BG GND	19	GND	Band Gap threshold voltage reference ground
BIAS V	48	Power	Live insertion pre-bias pin
TMS	42	Input	Test Mode Select (optional, if not implemented then no-connect)
TCK	44	Input	Test Clock (optional, if not implemented then no-connect)
TDI	22	Input	Test Data In (optional, if not implemented then shorted to TDO)
TDO	21	Output	Test Data Out (optional, if not implemented then shorted to TDI)
NC	25	NC	No Connect

FUNCTION TABLE

MODE	INPUTS					OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	OEA	AOn	$\overline{Bn}$*
AIn to $\overline{Bn}$	L	—	H	L	L	Z	H**
	H	—	H	L	L	Z	L
	L	—	H	L	H	L	H**
	H	—	H	L	H	H	L
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	H**
	X	X	X	H	X	X	H**
$\overline{Bn}$ to AOn	X	L	L	X	H	H	Input
	X	H	X	H	H	L	Input
	X	L	X	H	H	H	Input
	X	H	L	X	H	L	Input
Disable AOn outputs	—	X	X	X	L	Z	X

H** = Goes to level of pull-up voltage

B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

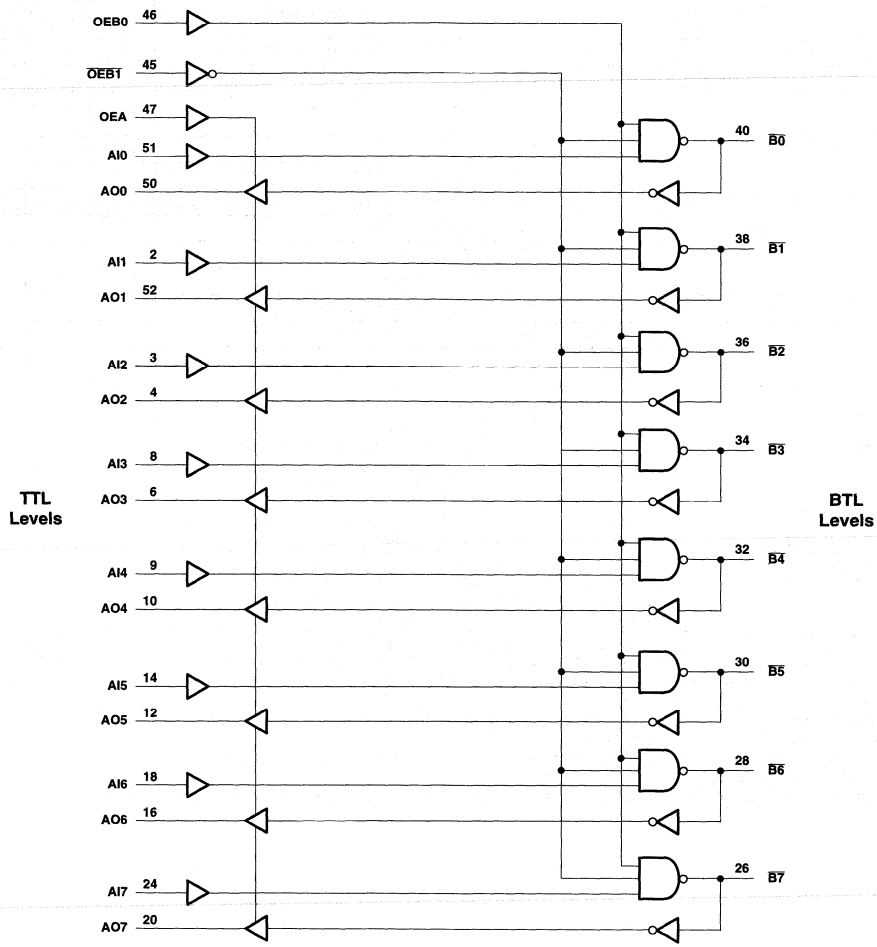
RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage	Except $\overline{B0}$–$\overline{B7}$	2.0			V
		$\overline{B0}$ – $\overline{B7}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}$–$\overline{B7}$			0.8	V
		$\overline{B0}$ – $\overline{B7}$			1.47	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	AO0 – AO7			-33/-12	mA
I_{OL}	Low-level output current	AO0 – AO7			+33/+12	mA
		$\overline{B0}$ – $\overline{B7}$			100	
C_{OB}	Output capacitance on B port			6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	°C

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
V_{BIASV}	Bias pin voltage	Voltage difference between the Bias voltage and V_{CC} after the PCB is plugged in.	–	–	0.5	V
I_{BIASV}	Bias pin (I_{BIASV}) input DC current	V_{CC} = 0 V, Bias V = 3.6V			1.2	mA
		V_{CC} = 3.3V, Bias V = 3.6V			10	µA
$V_{\overline{Bn}}$	Bus voltage during prebias	$\overline{B0}$ – $\overline{B8}$ = 0V, Bias V = 3.3V	1.62		2.1	V
I_{LM}	Fall current during prebias	$\overline{B0}$ – $\overline{B8}$ = 2V, Bias V = 1.3 to 2.5V			1	µA
I_{HM}	Rise current during prebias	$\overline{B0}$ – $\overline{B8}$ = 1V, Bias V = 3 to 3.6V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 3.3V, $\overline{B0}$ – $\overline{B8}$ = 0 to 2.0V, Bias V = 2.7 to 3.6V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 3.3V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 1.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 3.3V	1.0	1.35		ns

LOGIC DIAGRAM FOR FBL2040



NC = 25
LOGIC V_{CC} = 49
LOGIC GND = 1, 5, 7, 11, 13, 15
BUS V_{CC} = 23, 43
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48
BG V_{CC} = 17
BG GND = 19

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0} - \overline{B7}$	V_{CC} = MAX, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0} - \overline{B7}$	V_{CC} = 0V, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	AO0 – AO7[3]	V_{CC} = MIN to MAX; I_{OH} = -100µA	V_{CC} –0.2			V
			V_{CC} = MIN; I_{OH} = -8mA	2.4			V
			V_{CC} = MIN; I_{OH} = -32mA	2.0			V
V_{OL}	Low-level output voltage	AO0 – AO7[3]	V_{CC} = MIN; I_{OL} = 16mA			0.4	V
			V_{CC} = MIN; I_{OL} = 32mA			0.5	V
		$\overline{B0} - \overline{B7}$	V_{CC} = MIN, I_{OL} = 4mA	0.5			V
			V_{CC} = MIN, I_{OL} = 100mA	0.75	1.0	1.20	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK} = –18mA		–0.85	-1.2	V
I_I	Input leakage current	Control pins	V_{CC} = 3.6V; V_I = V_{CC} or GND			±1.0	µA
		Control/ AI0 – AI7	V_{CC} = 0V or 3.6V; V_I = 5.5V			10	
		AI0 – AI7	V_{CC} = 3.6V; V_I = V_{CC}			1	
		Note 4	V_{CC} = 3.6V; V_I = 0V			–5	
I_{IH}	High-level input current	$\overline{B0} - \overline{B7}$	V_{CC} = MAX, V_I = 1.9V			100	µA
			V_{CC} = MAX, V_I = 3.5V, note 5	100			
I_{IL}	Low-level input current	$\overline{B0} - \overline{B7}$	V_{CC} = MAX, V_I = 0.75V			-100	µA
I_{OZH}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O =3V			5	µA
I_{OZL}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O = 0.5V			-5	µA
I_{CC}	Supply current (total)	I_{CCZ} (standby)	V_{CC} = MAX		1.5	2.0	mA
		I_{CCB}, AIn to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		1.3	1.7	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs Low		10	13	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs High		10	13	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
4. Unused pins are at V_{CC} or GND.
5. For B port input voltage between 3 and 5 volt; I_{IH} will be greater than 100µA bu the part will continue to function normally.

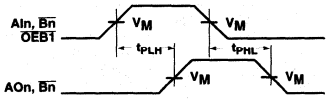
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, $\overline{Bn}$ to AOn	Waveform 1, 2	1.8 1.6	3.4 3.2	5.0 4.9	1.6 1.6	5.6 5.3	ns
t_{PZH} t_{PZL}	Output enable time, OEA to AOn	Waveform 4, 5	1.0 1.0		5.0 5.0	1.5 1.5	5.5 5.5	ns
t_{PHZ} t_{PLZ}	Output disable time, OEA to AOn	Waveform 4, 5	1.5 1.5	3.3 3.3	4.8 5.4	1.2 1.3	5.0 5.9	ns
t_{TLH} t_{THL}	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	1.5 1.5	2.2 2.4	3.5 3.5	1.0 1.0	4.5 4.5	ns
$t_{SK(o)}$	Output skew between receivers in same package[1]	Waveform 3		0.4	1.0		1.0	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**B PORT LIMITS**					**UNIT**
			T_{amb} = +25°C, V_{CC} = 3.3V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_D = 30pF, R_U = 9Ω		
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	2.9 1.6	4.4 3.3	5.0 4.8	2.3 1.5	5.5 5.1	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	2.9 1.9	4.7 3.5	5.9 5.1	2.6 1.8	7.8 5.7	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	3.0 1.7	5.3 3.2	6.3 4.8	2.7 1.5	8.0 5.7	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.4 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**R_U = 16.5Ω**			**R_U = 16.5Ω**		**UNIT**
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	3.0 1.7	4.5 3.3	6.4 4.8	2.3 1.6	6.9 5.1	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	3.0 2.0	4.8 3.5	6.0 5.2	2.7 1.9	7.9 5.7	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	3.1 1.8	5.4 3.3	6.4 4.9	2.8 1.6	8.1 5.7	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.5 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns

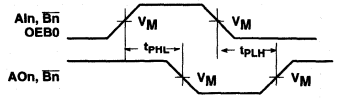
NOTES:

1. $|t_{PN}actual - t_{PM}actual|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).

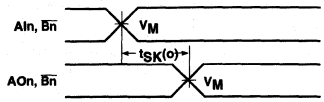
AC WAVEFORMS



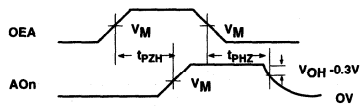
Waveform 1. Propagation Delay for Data or Output Enable to Output



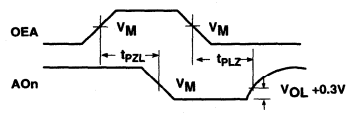
Waveform 2. Propagation Delay for Data or Output Enable to Output



Waveform 3. Output Skews



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

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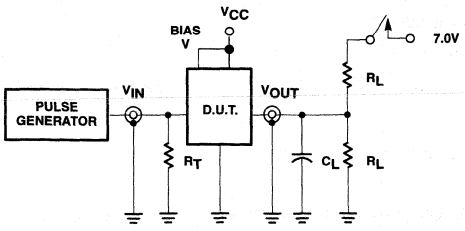
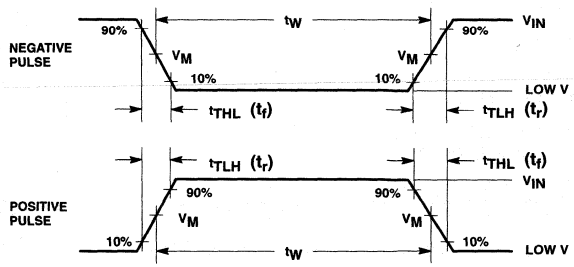
TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port



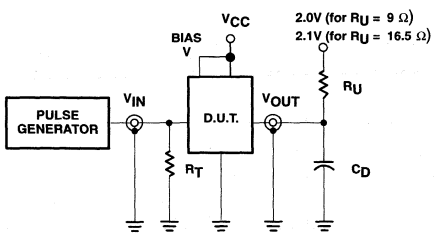
V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns



Test Circuit for Outputs on B Port

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

SG00059

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port) FBL2041

FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port

DESCRIPTION

The FBL2041 is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FBL2041 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The FBL2041 is pin and function compatible with FB2041 but operates at a 3.3V supply voltage, greatly reducing power consumption.

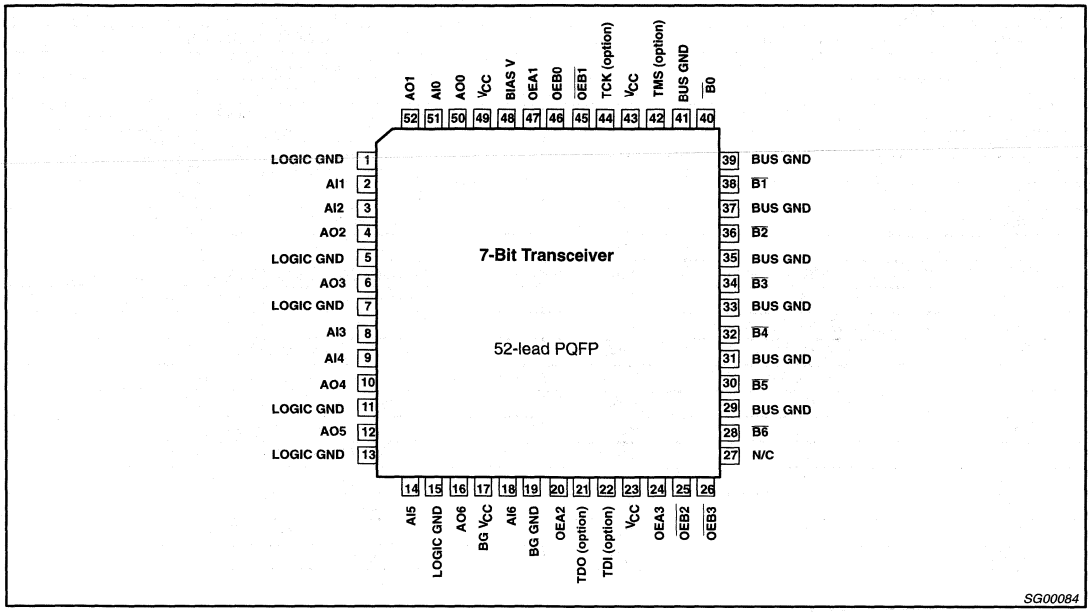
QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		4.2 3.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		4.8 4.9	ns
C_{OB}	Output capacitance ($\overline{B0}$ - $\overline{B6}$ only)		6	pF
I_{OL}	Output current ($\overline{B0}$ - $\overline{B6}$ only)		100	mA
I_{CC}	Supply Current	Standby	5.2	mA
		AIn to $\overline{Bn}$ (outputs Low or High)	3.2	
		$\overline{Bn}$ to AOn (outputs Low)	13.5	
		$\overline{Bn}$ to AOn (outputs High)	10.7	

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 3.3V±10%; T_{amb} = 0 to +70°C	DWG No.
52-pin Plastic Quad Flatpack	FBL2041BB	SOT379-1

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port) FBL2041



The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

There are three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement. The TTL/BTL output drivers for bit 0 are enabled with OEA1/$\overline{\text{OEB1}}$, output drivers for bits 1–2–3 are enabled with OEA2/$\overline{\text{OEB2}}$ and output drivers for bits 4–5–6 are enabled with OEA3/$\overline{\text{OEB3}}$.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEAn goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEAn goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 1.3V.

The B-port has an output enable, $\overline{\text{OEB0}}$, which affects all seven drivers. When OEB0 is High and $\overline{\text{OEBn}}$ is Low the output driver will be enabled. When OEB0 is Low or if $\overline{\text{OEBn}}$ is High, the B-port drivers will be inactive and at the level of the backplane signal.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while V_{CC} is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

JTAG boundary scan functionality is provided as an option with signals TMS, TCK, TDI and TDO. When this option is not present, TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
ai0 – ai6	51, 2, 3, 8, 9, 14, 18	Input	Data inputs (TTL)
aO0 – aO6	50, 52, 4, 6, 10, 12, 16	Output	3-state outputs (TTL)
$\overline{b0}$ – $\overline{b6}$	40, 38, 36, 34, 32, 30, 28	i/o	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the Bn outputs when High
OEB1	45	Input	Enables the B0 output when Low
OEB2	25	Input	Enables the B1 – B3 outputs when Low
OEB3	26	Input	Enables the B4 – B6 outputs when Low
OEA1	47	Input	Enables the A0 outputs when High
OEA2	20	Input	Enables the A1 – A3 outputs when High
OEA3	24	Input	Enables the A4 – A6 outputs when High
bus gnd	41, 39, 37, 35, 33, 31, 29	GND	Bus ground (0V)
LOGIC gnd	1, 5, 7, 11, 13, 15	GND	Logic ground (0V)
LOGIC/bus V_{CC}	23, 43, 49	Power	Positive supply voltage
BG V_{CC}	17	Power	Positive supply voltage BAND GAP
BIAS V	48	Power	Positive supply voltage
TMS	42	Input	Test Mode Select (no-connect)
Tck	44	Input	Test Clock (no-connect)
Tdi	22	Input	Test Data In (shorted to TDO)
Tdo	21	Output	Test Data Out (TDI)
BG GND	19	GND	BAND GAP GROUND (0V)

FUNCTION TABLE

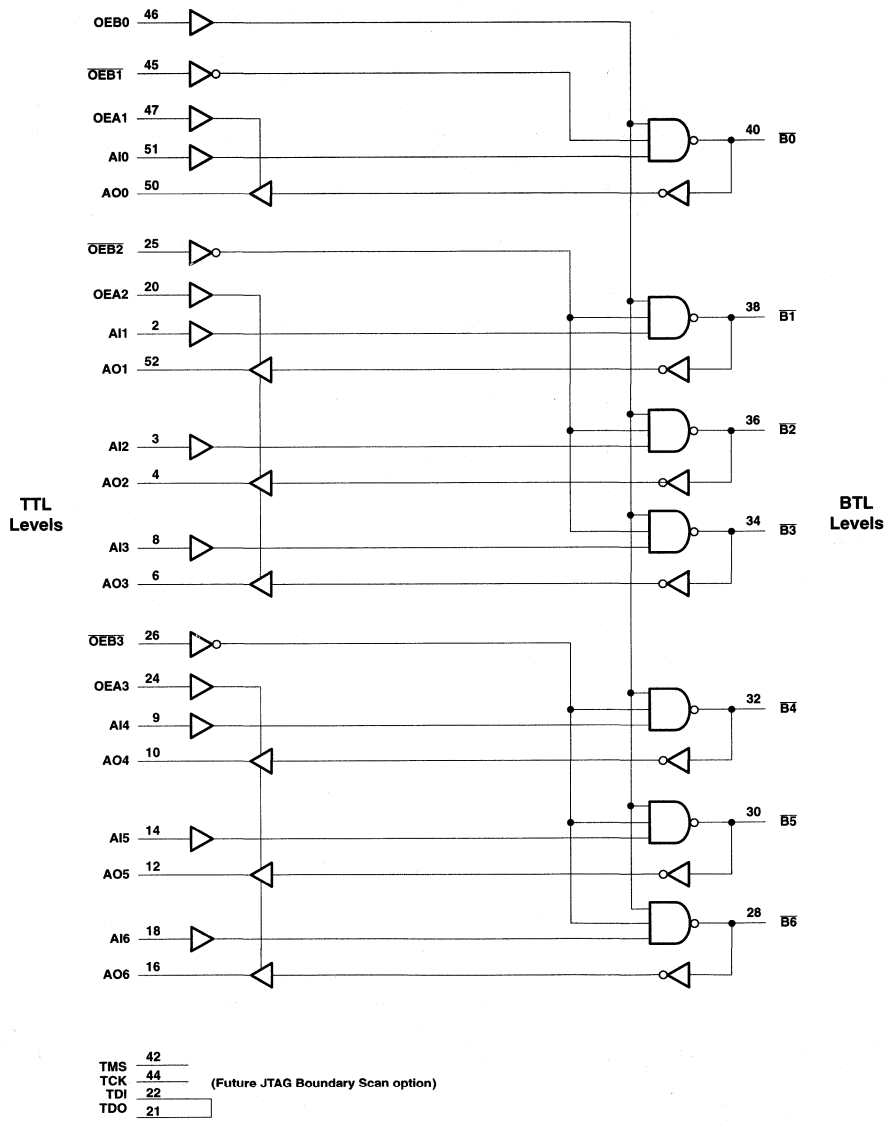
MODE	INPUTS									OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	$\overline{OEB2}$	$\overline{OEB3}$	OEA1	OEA2	OEA3	AOn	$\overline{Bn}$*
AIn to $\overline{Bn}$	L	—	H	L	L	L	L	L	L	Z	H**
	H	—	H	L	L	L	L	L	L	Z	L
	L	—	H	L	L	L	H	H	H	L	H**
	H	—	H	L	L	L	H	H	H	H	L
AI0 to $\overline{B0}$	L	—	H	L	X	X	L	L	L	Z	H**
	H	—	H	L	X	X	L	L	L	Z	L
	L	—	H	L	X	X	H	H	H	L	H**
	H	—	H	L	X	X	H	H	H	H	L
AI1 – AI3 to $\overline{B1}$ – $\overline{B3}$	L	—	H	X	L	X	L	L	L	Z	H**
	H	—	H	X	L	X	L	L	L	Z	L
	L	—	H	X	L	X	H	H	H	L	H**
	H	—	H	X	L	X	H	H	H	H	L
AI4 – AI6 to $\overline{B4}$ – $\overline{B6}$	L	—	H	X	X	L	L	L	L	Z	H**
	H	—	H	X	X	L	L	L	L	Z	L
	L	—	H	X	X	L	H	H	H	L	H**
	H	—	H	X	X	L	H	H	H	H	L
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	H	H	X	X	X	X	H**
Disable $\overline{B0}$ outputs	X	X	H	H	X	X	X	X	X	X	H**
Disable $\overline{B1}$ – $\overline{B3}$ outputs	X	X	H	X	H	X	X	X	X	X	H**
Disable $\overline{B4}$ – $\overline{B6}$ outputs	X	X	H	X	X	H	X	X	X	X	H**
$\overline{Bn}$ to AOn	X	L	L	X	X	X	H	H	H	H	Input
	X	H	L	X	X	X	H	H	H	L	Input
	X	L	X	H	H	H	H	H	H	H	Input
	X	H	X	H	H	H	H	H	H	L	Input
$\overline{B0}$ to AO0	X	L	L	X	X	X	H	X	X	H	Input
	X	H	L	X	X	X	H	X	X	L	Input
	X	L	X	H	H	H	H	X	X	H	Input
	X	H	X	H	H	H	H	X	X	L	Input
$\overline{B1}$ – $\overline{B3}$ to AO1 – AO3	X	L	L	X	X	X	X	H	X	H	Input
	X	H	L	X	X	X	X	H	X	L	Input
	X	L	X	H	H	H	X	H	X	H	Input
	X	H	X	H	H	H	X	H	X	L	Input
$\overline{B4}$ – $\overline{B6}$ to AO4 – AO6	X	L	L	X	X	X	X	X	H	H	Input
	X	H	L	X	X	X	X	X	H	L	Input
	X	L	X	H	H	H	X	X	H	H	Input
	X	H	X	H	H	H	X	X	H	L	Input
Disable AOn outputs	X	X	X	X	X	X	L	L	L	Z	X
Disable AO0 outputs	X	X	X	X	X	X	L	X	X	Z	X
Disable AO1 – AO3 outputs	X	X	X	X	X	X	X	L	X	Z	X
Disable AO4 – AO6 outputs	X	X	X	X	X	X	X	X	L	Z	X

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
H** = Goes to level of pull-up voltage
B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

Z = High-impedance (OFF) state
— = Input not externally driven
H** = Goes to level of pull-up voltage
B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

LOGIC DIAGRAM



LOGIC V_{CC} = 17, 49
LOGIC GND = 1, 5, 7, 11, 13, 15, 19
BUS V_{CC} = 23, 43
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48

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ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +4.6	V
V_{IN}	Input voltage	AI0 – AI6, OEB0, $\overline{OEBn}$, OEAn	-0.5 to +7.0	V
		$\overline{B0} – \overline{B6}$	-0.5 to +3.5	
I_{IN}	Input current	$V_{IN} < 0$	-50	
V_{OUT}	Voltage applied to output in High output state		-0.5 to +7.0	V
I_{OUT}	Current applied to output in	AO0 – AO6	64, –64	mA
	Low output state/High output state	$\overline{B0} – \overline{B6}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		COMMERCIAL LIMITS V_{CC} = 3.3V±10%; T_{amb} = 0 to +70°C			INDUSTRIAL LIMITS V_{CC} = 3.3V±10%; T_{amb} = -40 to +85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		3.0	3.3	3.6	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	Except $\overline{B0}–\overline{B6}$	2.0			2.0			V
		$\overline{B0} – \overline{B6}$	1.62	1.55		1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}–\overline{B6}$			0.8			0.8	V
		$\overline{B0} – \overline{B6}$			1.47			1.47	
I_{IK}	Input clamp current				-18			-18	mA
I_{OH}	High-level output current	AO0 – AO6			-32			-32	mA
I_{OL}	Low-level output current	AO0 – AO6			+32			+32	mA
		$\overline{B0} – \overline{B6}$			100			100	
C_{OB}	Output capacitance on B port			6	7		6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	-40		+85	°C

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
V_{BIASV}	Bias pin voltage	Voltage difference between the Bias voltage and V_{CC} after the PCB is plugged in.	–	–	0.5	V
I_{BIASV}	Bias pin (I_{BIASV}) input DC current	V_{CC} = 0 V, Bias V = 3.6V			1.2	mA
		V_{CC} = 3.3V, Bias V = 3.6V			10	µA
$V_{\overline{Bn}}$	Bus voltage during prebias	$\overline{B0} - \overline{B8}$ = 0V, Bias V = 3.3V	1.62		2.1	V
I_{LM}	Fall current during prebias	$\overline{B0} - \overline{B8}$ = 2V, Bias V = 1.3 to 2.5V			1	µA
I_{HM}	Rise current during prebias	$\overline{B0} - \overline{B8}$ = 1V, Bias V = 3 to 3.6V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 3.3V, $\overline{B0} - \overline{B8}$ = 0 to 2.0V, Bias V = 2.7 to 3.6V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 3.3V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 1.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 3.3V	1.0	1.35		ns

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0} - \overline{B6}$	V_{CC} = MAX, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0} - \overline{B6}$	V_{CC} = 0V, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	AO0 – AO6[3]	V_{CC} = MIN to MAX; I_{OH} = -100µA	V_{CC} –0.2			V
			V_{CC} = MIN; I_{OH} = -8mA	2.4			V
			V_{CC} = MIN; I_{OH} = -32mA	2.0			V
V_{OL}	Low-level output voltage	AO0 – AO6[3]	V_{CC} = MIN; I_{OL} = 16mA			0.4	V
			V_{CC} = MIN; I_{OL} = 32mA			0.5	V
		$\overline{B0} - \overline{B6}$	V_{CC} = MIN, I_{OL} = 4mA	0.5			V
			V_{CC} = MIN, I_{OL} = 100mA	0.75	1.0	1.20	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK} = –18mA		–0.85	-1.2	V
I_I	Input leakage current	Control pins	V_{CC} = 3.6V; V_I = V_{CC} or GND			±1.0	µA
		Control/ AI0 – AI6	V_{CC} = 0V or 3.6V; V_I = 5.5V			10	
		AI0 – AI6	V_{CC} = 3.6V; V_I = V_{CC}			1	
		Note 4	V_{CC} = 3.6V; V_I = 0V			–5	
I_{IH}	High-level input current	$\overline{B0} - \overline{B6}$	V_{CC} = MAX, V_I = 1.9V			100	µA
I_{IH}	High-level input current	$\overline{B0} - \overline{B6}$	V_{CC} = MAX, V_I = 3.5V, note 5	100			mA
I_{IL}	Low-level input current	$\overline{B0} - \overline{B6}$	V_{CC} = MAX, V_I = 0.75V			-100	µA
I_{OZH}	Off-state output current	AO0 – AO6	V_{CC} = MAX, V_O =3V			5	µA
I_{OZL}	Off-state output current	AO0 – AO6	V_{CC} = MAX, V_O = 0.5V			-5	µA
I_{CC}	Supply current (total)	I_{CCZ}	V_{CC} = MAX		5.2	13.5	mA
		I_{CCB}	V_{CC} = MAX, outputs Low or High		3.2	9.0	
		I_{CCL} A3	V_{CC} = MAX, outputs Low		13.5	19.5	
		I_{CCH} A5	V_{CC} = MAX, outputs High		10.7	16.0	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
4. Unused pins are at V_{CC} or GND.
5. For B port input voltage between 3 and 5 volt; I_{IH} will be greater than 100mA but the part will continue to function normally (clamping circuit is active).

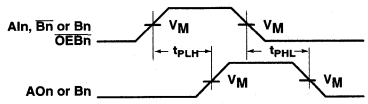
AC ELECTRICAL CHARACTERISTICS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, $\overline{Bn}$ to AOn	Waveform 1, 2	3.9 4.0	4.8 4.9	5.8 6.0	3.7 3.8	6.4 6.7	ns
t_{PZH} t_{PZL}	Output enable time, OEA to AOn	Waveform 4, 5	5.3 2.4	6.6 4.4	8.0 8.0	5.0 2.1	8.6 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time, OEA to AOn	Waveform 4, 5	3.5 2.3	4.8 3.1	6.0 3.9	3.4 2.2	6.5 4.3	ns
t_{TLH} t_{THL}	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	0.8 0.6	1.6 1.1	2.8 1.7	0.7 0.5	3.0 2.0	ns
$t_{SK}(o)$	Output skew between receivers in same package[1]	Waveform 3		0.4	1.5		1.5	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**B PORT LIMITS**					**UNIT**
			T_{amb} = +25°C, V_{CC} = 3.3V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_D = 30pF, R_U = 9Ω		
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	3.3 2.7	4.2 3.5	5.2 4.5	2.9 2.5	6.0 5.0	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	4.0 3.4	4.9 4.3	5.8 5.3	3.6 3.1	6.6 6.0	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	4.2 2.9	5.1 3.8	6.1 4.7	3.9 2.6	6.9 5.5	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.3 0.4	1.9 0.8	2.8 1.4	1.2 0.4	3.0 1.5	ns
$t_{SK}(o)$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.4		1.4	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	R_U = 16.5Ω			R_U = 16.5Ω		**UNIT**
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	3.3 2.7	4.2 3.6	5.1 4.5	3.0 2.5	6.0 5.0	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	4.0 3.4	4.9 4.3	5.8 5.3	3.6 3.1	6.6 6.0	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	4.2 2.9	5.1 3.8	6.1 4.7	3.9 2.6	6.8 5.5	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.3 0.4	1.9 0.8	2.8 1.4	1.2 0.4	3.0 1.5	ns
$t_{SK}(o)$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.4		1.4	ns

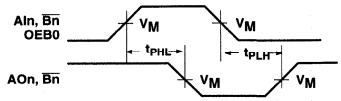
NOTES:

1. $|t_{PN}actual - t_{PM}actual|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).

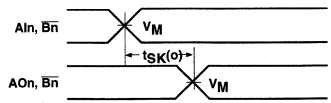
AC WAVEFORMS



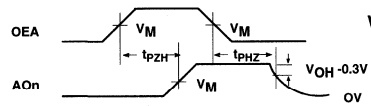
Waveform 1. Propagation Delay for Data or Output Enable to Output



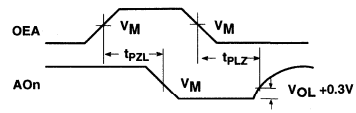
Waveform 2. Propagation Delay for Data or Output Enable to Output



Waveform 3. Output Skews



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

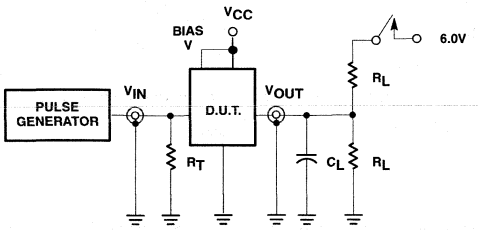


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

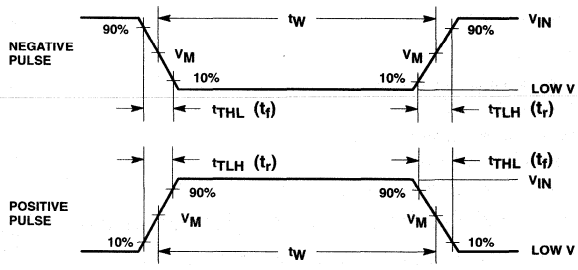
NOTE: V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

SG00086

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port



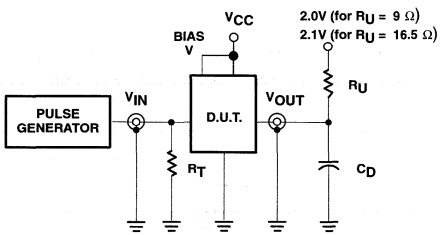
V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

SWITCH POSITION FOR ALL A-PORTS

TEST	SWITCH
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	CLOSED
t_{PHZ}, t_{PZH}	GND

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns



Test Circuit for Outputs on B Port

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

SG00090

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port) FBL22041

FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port

DESCRIPTION

The FBL22041 is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FBL22041 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The FBL22041 is pin and function compatible with FB2041 but operates at a 3.3V supply voltage, greatly reducing power consumption.

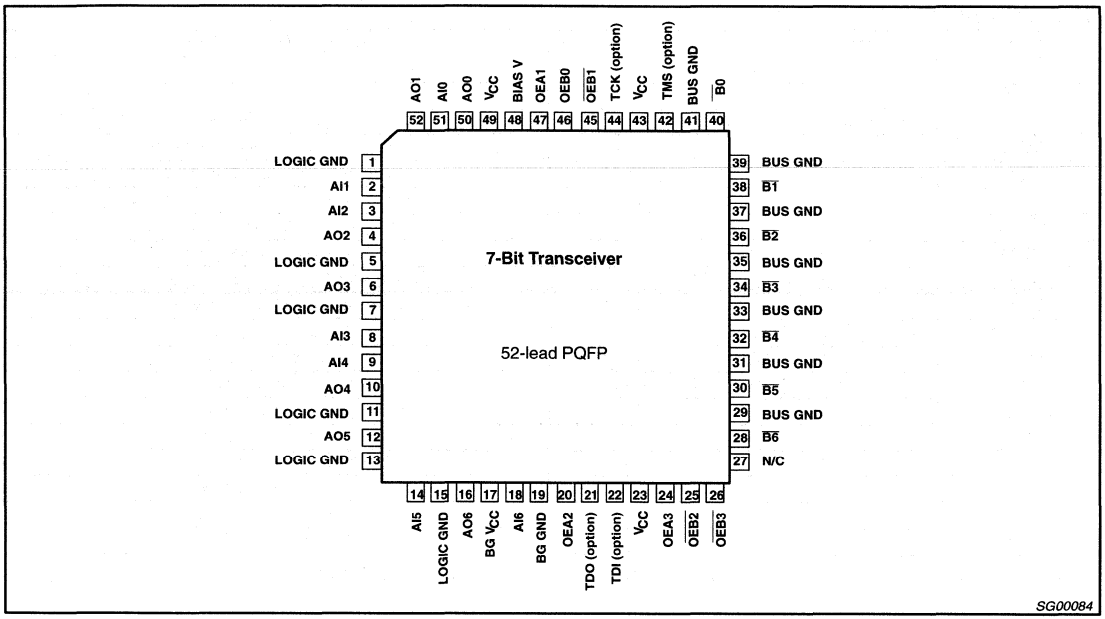
QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		4.1 3.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		5.2 5.1	ns
C_{OB}	Output capacitance ($\overline{B0}$ - $\overline{B6}$ only)		6	pF
I_{OL}	Output current ($\overline{B0}$ - $\overline{B6}$ only)		100	mA
I_{CC}	Supply Current	Standby	6.0	mA
		AIn to $\overline{Bn}$ (outputs Low or High)	5.1	
		$\overline{Bn}$ to AOn (outputs Low)	13.4	
		$\overline{Bn}$ to AOn (outputs High)	10.6	

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 3.3V±10%; T_{amb} = 0 to +70°C	DWG No.
52-pin Plastic Quad Flatpack	FBL22041BB	SOT379-1

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port) FBL22041



The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

There are three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement. The TTL/BTL output drivers for bit 0 are enabled with OEA1/$\overline{\text{OEB1}}$, output drivers for bits 1–2–3 are enabled with OEA2/$\overline{\text{OEB2}}$ and output drivers for bits 4–5–6 are enabled with OEA3/$\overline{\text{OEB3}}$.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEAn goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEAn goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 1.3V.

The B-port has an output enable, OEB0, which affects all seven drivers. When OEB0 is High and $\overline{\text{OEBn}}$ is Low the output driver will be enabled. When OEB0 is Low or if $\overline{\text{OEBn}}$ is High, the B-port drivers will be inactive and at the level of the backplane signal.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
ai0 – ai6	51, 2, 3, 8, 9, 14, 18	Input	Data inputs (TTL)
aO0 – aO6	50, 52, 4, 6, 10, 12, 16	Output	3-state outputs (TTL)
$\overline{b0}$ – $\overline{b6}$	40, 38, 36, 34, 32, 30, 28	i/o	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the Bn outputs when High
OEB1	45	Input	Enables the B0 output when Low
OEB2	25	Input	Enables the B1 – B3 outputs when Low
OEB3	26	Input	Enables the B4 – B6 outputs when Low
OEA1	47	Input	Enables the A0 outputs when High
OEA2	20	Input	Enables the A1 – A3 outputs when High
OEA3	24	Input	Enables the A4 – A6 outputs when High
bus gnd	41, 39, 37, 35, 33, 31, 29	GND	Bus ground (0V)
LOGIC gnd	1, 5, 7, 11, 13, 15	GND	Logic ground (0V)
LOGIC/bus V_{CC}	23, 43, 49	Power	Positive supply voltage
BG V_{CC}	17	Power	Positive supply voltage BAND GAP
BIAS V	48	Power	Positive supply voltage
TMS	42	Input	Test Mode Select (no-connect)
Tck	44	Input	Test Clock (no-connect)
Tdi	22	Input	Test Data In (shorted to TDO)
Tdo	21	Output	Test Data Out (TDI)
BG GND	19	GND	BAND GAP GROUND (0V)

FUNCTION TABLE

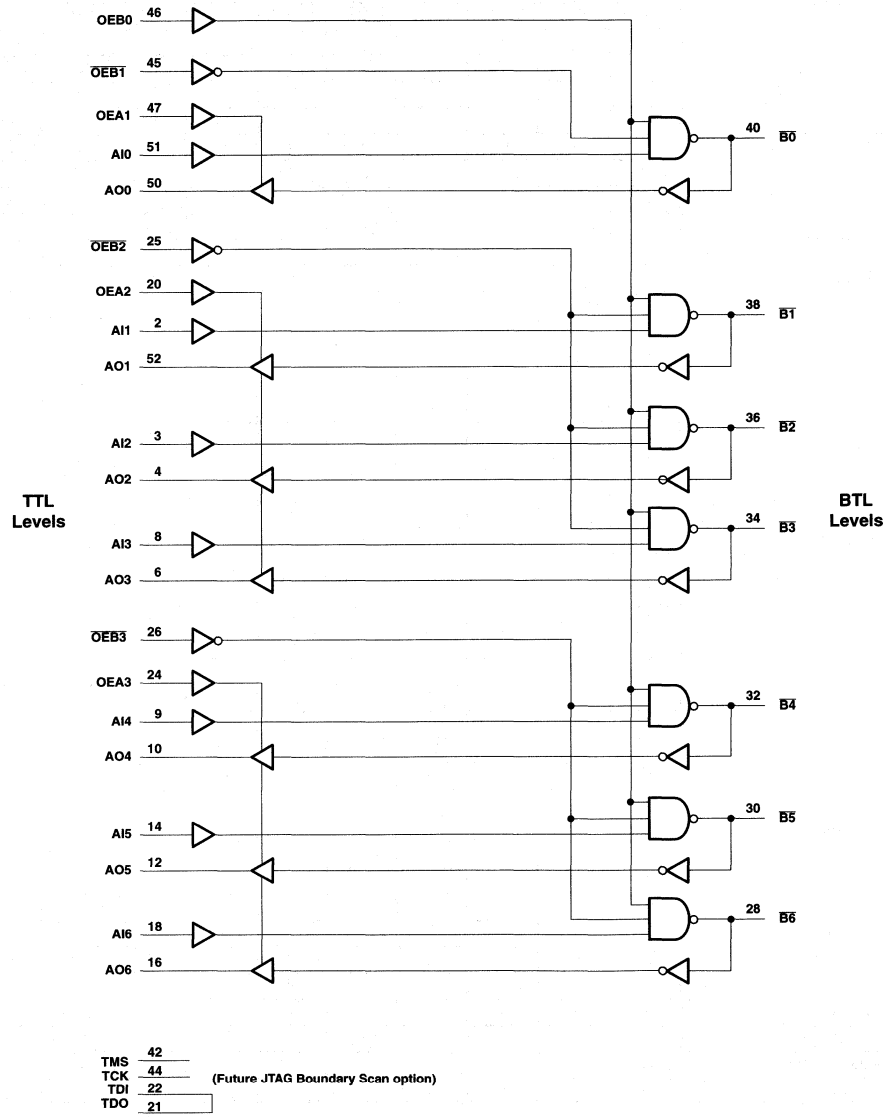
MODE	INPUTS									OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	$\overline{OEB2}$	$\overline{OEB3}$	OEA1	OEA2	OEA3	AOn	$\overline{Bn}$*
AIn to $\overline{Bn}$	L	—	H	L	L	L	L	L	L	Z	H**
	H	—	H	L	L	L	L	L	L	Z	L
	L	—	H	L	L	L	H	H	H	L	H**
	H	—	H	L	L	L	H	H	H	H	L
AI0 to $\overline{B0}$	L	—	H	L	X	X	L	L	L	Z	H**
	H	—	H	L	X	X	L	L	L	Z	L
	L	—	H	L	X	X	H	H	H	L	H**
	H	—	H	L	X	X	H	H	H	H	L
AI1 – AI3 to $\overline{B1}$ – $\overline{B3}$	L	—	H	X	L	X	L	L	L	Z	H**
	H	—	H	X	L	X	L	L	L	Z	L
	L	—	H	X	L	X	H	H	H	L	H**
	H	—	H	X	L	X	H	H	H	H	L
AI4 – AI6 to $\overline{B4}$ – $\overline{B6}$	L	—	H	X	X	L	L	L	L	Z	H**
	H	—	H	X	X	L	L	L	L	Z	L
	L	—	H	X	X	L	H	H	H	L	H**
	H	—	H	X	X	L	H	H	H	H	L
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	H	H	X	X	X	X	H**
Disable $\overline{B0}$ outputs	X	X	H	H	X	X	X	X	X	X	H**
Disable $\overline{B1}$ – $\overline{B3}$ outputs	X	X	H	X	H	X	X	X	X	X	H**
Disable $\overline{B4}$ – $\overline{B6}$ outputs	X	X	H	X	X	H	X	X	X	X	H**
$\overline{Bn}$ to AOn	X	L	L	X	X	X	H	H	H	H	Input
	X	H	L	X	X	X	H	H	H	L	Input
	X	L	X	H	H	H	H	H	H	H	Input
	X	H	X	H	H	H	H	H	H	L	Input
$\overline{B0}$ to AO0	X	L	L	X	X	X	H	X	X	H	Input
	X	H	L	X	X	X	H	X	X	L	Input
	X	L	X	H	H	H	H	X	X	H	Input
	X	H	X	H	H	H	H	X	X	L	Input
$\overline{B1}$ – $\overline{B3}$ to AO1 – AO3	X	L	L	X	X	X	X	H	X	H	Input
	X	H	L	X	X	X	X	H	X	L	Input
	X	L	X	H	H	H	X	H	X	H	Input
	X	H	X	H	H	H	X	H	X	L	Input
$\overline{B4}$ – $\overline{B6}$ to AO4 – AO6	X	L	L	X	X	X	X	X	H	H	Input
	X	H	L	X	X	X	X	X	H	L	Input
	X	L	X	H	H	H	X	X	H	H	Input
	X	H	X	H	H	H	X	X	H	L	Input
Disable AOn outputs	X	X	X	X	X	X	L	L	L	Z	X
Disable AO0 outputs	X	X	X	X	X	X	L	X	X	Z	X
Disable AO1 – AO3 outputs	X	X	X	X	X	X	X	L	X	Z	X
Disable AO4 – AO6 outputs	X	X	X	X	X	X	X	X	L	Z	X

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
H** = Goes to level of pull-up voltage
B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

Z = High-impedance (OFF) state
— = Input not externally driven
H** = Goes to level of pull-up voltage
B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

LOGIC DIAGRAM



LOGIC V_{CC} = 17, 49
LOGIC GND = 1, 5, 7, 11, 13, 15, 19
BUS V_{CC} = 23, 43
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48

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ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +4.6	V
V_{IN}	Input voltage	AI0 – AI6, OEB0, $\overline{OEBn}$, OEAn	-0.5 to +7.0	V
		$\overline{B0} – \overline{B6}$	-0.5 to +3.5	
I_{IN}	Input current	$V_{IN} < 0$	-50	
V_{OUT}	Voltage applied to output in High output state		-0.5 to +7.0	V
I_{OUT}	Current applied to output in	AO0 – AO6	48, –24	mA
	Low output state/High output state	$\overline{B0} – \overline{B6}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		COMMERCIAL LIMITS V_{CC} = 3.3V±10%; T_{amb} = 0 to +70°C			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage	Except $\overline{B0}$–$\overline{B6}$	2.0			V
		$\overline{B0} – \overline{B6}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}$–$\overline{B6}$			0.8	V
		$\overline{B0} – \overline{B6}$			1.47	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	AO0 – AO6			-12	mA
I_{OL}	Low-level output current	AO0 – AO6			12	mA
		$\overline{B0} – \overline{B6}$			100	
C_{OB}	Output capacitance on B port			6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	°C

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
V_{BIASV}	Bias pin voltage	Voltage difference between the Bias voltage and V_{CC} after the PCB is plugged in.	–	–	0.5	V
I_{BIASV}	Bias pin (I_{BIASV}) input DC current	V_{CC} = 0 V, Bias V = 3.6V			1.2	mA
		V_{CC} = 3.3V, Bias V = 3.6V			10	µA
$V_{\overline{Bn}}$	Bus voltage during prebias	$\overline{B0}$ – $\overline{B8}$ = 0V, Bias V = 3.3V	1.62		2.1	V
I_{LM}	Fall current during prebias	$\overline{B0}$ – $\overline{B8}$ = 2V, Bias V = 1.3 to 2.5V			1	µA
I_{HM}	Rise current during prebias	$\overline{B0}$ – $\overline{B8}$ = 1V, Bias V = 3 to 3.6V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 3.3V, $\overline{B0}$ – $\overline{B8}$ = 0 to 2.0V, Bias V = 2.7 to 3.6V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 3.3V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 1.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 3.3V	1.0	1.35		ns

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0}$ – $\overline{B6}$	V_{CC} = MAX, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0}$ – $\overline{B6}$	V_{CC} = 0V, V_{IL} = MAX, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	AO0 – AO6 [3]	V_{CC} = MIN to MAX; I_{OH} = -100µA	V_{CC} –0.2			V
			V_{CC} = MIN; I_{OH} = -4mA	2.4			V
			V_{CC} = MIN; I_{OH} = -12mA	2.0			V
V_{OL}	Low-level output voltage	AO0 – AO6 [3]	V_{CC} = MIN; I_{OL} = 4mA			0.4	V
			V_{CC} = MIN; I_{OL} = 12mA			0.8	V
		$\overline{B0}$ – $\overline{B6}$	V_{CC} = MIN, I_{OL} = 4mA	0.5			V
			V_{CC} = MIN, I_{OL} = 100mA	0.75	1.0	1.20	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK} = –18mA		–0.85	-1.2	V
I_I	Input leakage current	Control pins	V_{CC} = 3.6V; V_I = V_{CC} or GND			±1.0	µA
		Control/ AI0 – AI6	V_{CC} = 0V or 3.6V; V_I = 5.5V			10	
		AI0 – AI6	V_{CC} = 3.6V; V_I = V_{CC}			1	
		Note 4	V_{CC} = 3.6V; V_I = 0V			–5	
I_{IH}	High-level input current	$\overline{B0}$ – $\overline{B6}$	V_{CC} = MAX, V_I = 1.9V			100	µA
I_{IH}	High-level input current	$\overline{B0}$ – $\overline{B6}$	V_{CC} = MAX, V_I = 3.5V, note 5	100			mA
I_{IL}	Low-level input current	$\overline{B0}$ – $\overline{B6}$	V_{CC} = MAX, V_I = 0.75V			-100	µA
I_{OZH}	Off-state output current	AO0 – AO6	V_{CC} = MAX, V_O =3V			5	µA
I_{OZL}	Off-state output current	AO0 – AO6	V_{CC} = MAX, V_O = 0.5V			-5	µA
I_{CC}	Supply current (total)	I_{CCZ} (standby)	V_{CC} = MAX		6.0	13.0	mA
		I_{CCB}, AIn to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		5.1	10.0	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs Low		13.4	19.5	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs High		10.6	16.0	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
4. Unused pins are at V_{CC} or GND.
5. For B port input voltage between 3 and 5 volt; I_{IH} will be greater than 100mA but the part will continue to function normally (clamping circuit is active).

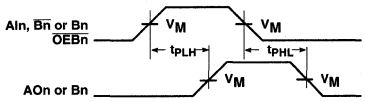
AC ELECTRICAL CHARACTERISTICS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 3.3V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, $\overline{Bn}$ to AOn	Waveform 1, 2	4.2 4.1	5.2 5.1	6.2 6.1	3.9 3.9	7.0 6.8	ns
t_{PZH} t_{PZL}	Output enable time, OEA to AOn	Waveform 4, 5	5.8 2.7	7.1 4.5	8.5 8.0	5.4 2.5	9.4 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time, OEA to AOn	Waveform 4, 5	3.9 3.7	5.2 4.8	6.5 6.0	3.6 3.3	7.0 7.3	ns
t_{TLH} t_{THL}	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	0.8 0.6	1.6 1.1	2.8 1.7	0.7 0.5	3.0 2.0	ns
$t_{SK(o)}$	Output skew between receivers in same package[1]	Waveform 3		0.4	1.5		1.5	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**B PORT LIMITS**					**UNIT**
			T_{amb} = +25°C, V_{CC} = 3.3V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 3.3V±10%, C_D = 30pF, R_U = 9Ω		
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	3.2 2.9	4.1 3.6	5.0 4.4	2.9 2.7	5.8 4.9	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	3.9 3.5	4.7 4.4	5.5 5.4	3.5 3.2	6.4 5.9	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	4.1 3.0	5.0 3.9	5.9 4.8	3.8 2.6	6.6 5.5	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.3 0.4	1.9 0.8	2.8 1.4	1.2 0.4	3.0 1.5	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.4		1.4	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	R_U = 16.5Ω			R_U = 16.5Ω		**UNIT**
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	3.2 2.9	4.1 3.6	5.0 4.9	2.9 2.6	5.8 4.9	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	3.9 3.5	4.7 4.4	5.5 5.4	3.5 3.2	6.4 5.9	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	4.1 3.0	5.0 3.9	5.9 4.8	3.8 2.6	6.6 5.5	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.3 0.4	1.9 0.8	2.8 1.4	1.2 0.4	3.0 1.5	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.4		1.4	ns

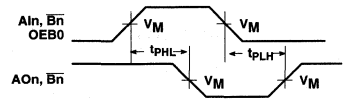
NOTES:

1. $|t_{PN}actual - t_{PM}actual|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).

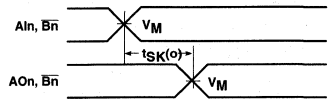
AC WAVEFORMS



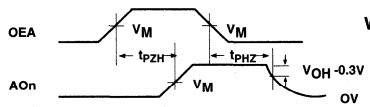
Waveform 1. Propagation Delay for Data or Output Enable to Output



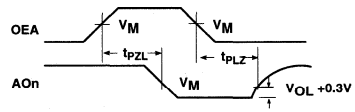
Waveform 2. Propagation Delay for Data or Output Enable to Output



Waveform 3. Output Skews



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

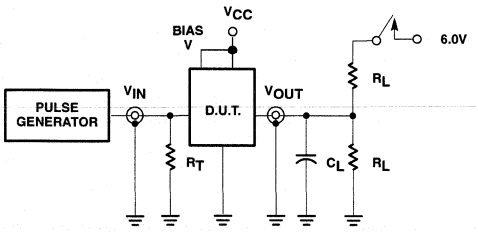


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

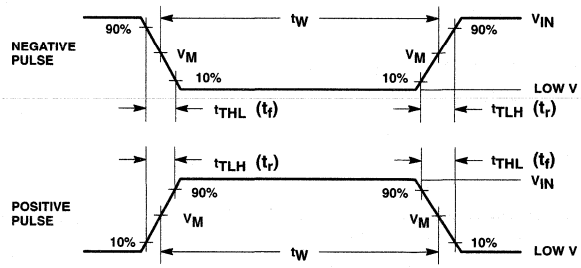
NOTE: V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

SG00086

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port



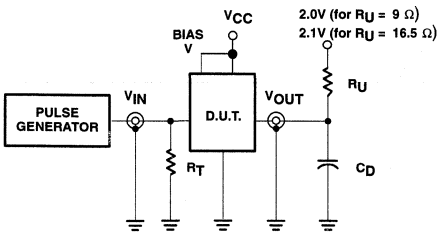
V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

SWITCH POSITION FOR ALL A-PORTS

TEST	SWITCH
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	CLOSED
t_{PHZ}, t_{PZH}	GND

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns



Test Circuit for Outputs on B Port

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

SG00090

18-bit universal GTL to ALVT/LVT translating bus transceiver (3-State)

74GTL16612

FEATURES

- 18-bit bidirectional bus interface
- Translates between GTL logic levels (B ports) and ALVT logic levels (A ports)
- 5V I/O compatible on the ALVT side (A ports)
- 3-State buffers
- Output capability: +64mA/-32mA on the ALVT side (A ports); +40mA on the GTL side (B ports)
- TTL input levels on control pins
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when ALVT output is tied to 5V bus
- Positive edge triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74GTL16612 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V and 3.3V with I/O compatibility up to 5V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When $\overline{OEAB}$ is Low, the outputs are active. When $\overline{OEAB}$ is High, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs ($\overline{CEBA}$/$\overline{CEAB}$).

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and CPBA.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Except for the GTL logic levels on the B-port, the functionality of the 74GTL16612 is the same as for the 74ALVT16601.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF	2.5	1.9	ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or V_{CC}	4	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or V_{CC}	8	8	pF
I_{CCZ}	Total supply current	Outputs disabled	40	60	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74GTL16612 DL	GTL16612 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74GTL16612 DGG	GTL16612 DGG	SOT364-1

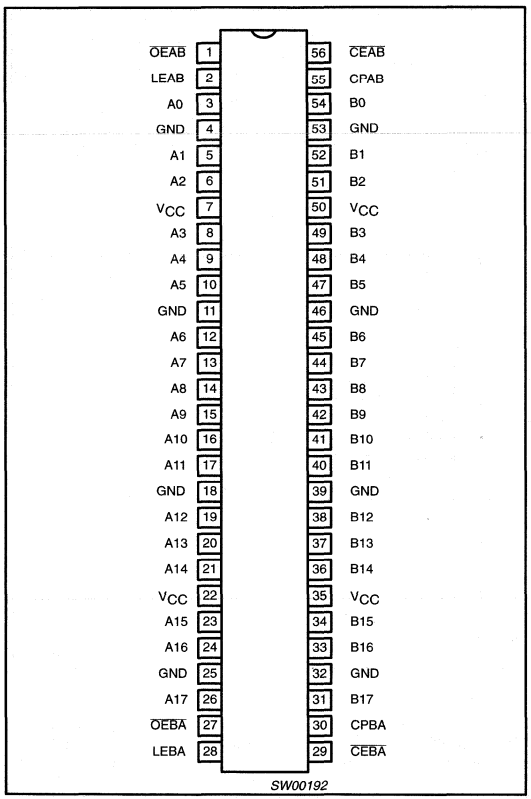
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 27	$\overline{OEAB}$/$\overline{OEBA}$	A-to-B/ B-to-A Output enable input (active Low)
29, 56	$\overline{CEBA}$/$\overline{CEAB}$	B-to-A/A-to-B clock enable
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

18-bit universal GTL to ALVT/LVT translating bus transceiver (3-State)

74GTL16612

PIN CONFIGURATION

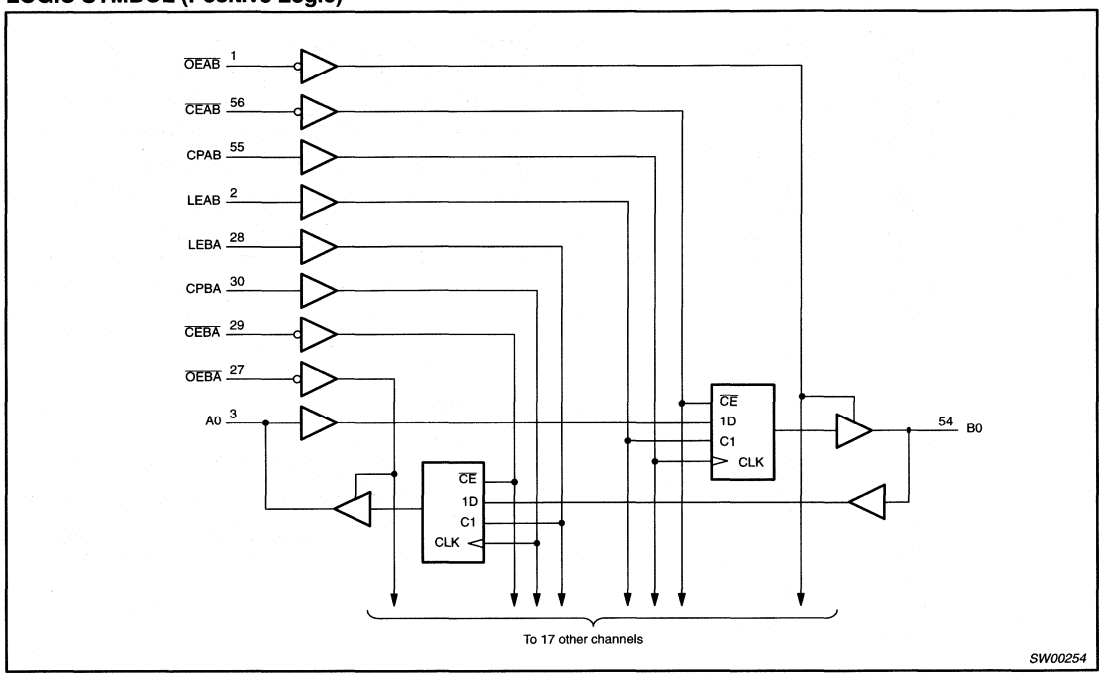


FUNCTION TABLE

INPUTS					OUTPUT
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CPAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	$B_O^{\pm}$
H	L	L	X	X	$B_O^{\pm}$
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	H	X	$B_O^{\pm}$
L	L	L	L	X	$B_O^{\S}$

X = Don't care
H = High voltage level
L = Low voltage level
↑ = Low to High
Z = High impedance "off" state
† = A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CPBA, and $\overline{CEBA}$.
$^{\pm}$ = Output level before the indicated steady-state input conditions were established.
§ = Output level before the indicated steady-state input conditions were established, provided that CPAB was Low before LEAB went Low.

LOGIC SYMBOL (Positive Logic)



ABSOLUTE MAXIMUM RATINGS [1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state – A port	128	mA
		Output in Low state – B port	80	mA
		Output in High state – A Port	–64	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage		2.3	2.7	3.0	3.6	V
V_I	Input voltage	A port	0	5.5	0	5.5	V
		B port		3.3		3.3	V
V_{IH}	High-level input voltage	A port	1.7		2.0		V
		B port	V_{REF}+50mV		V_{REF}+50mV		V
V_{IL}	Input voltage	A port		0.7		0.8	V
		B port		V_{REF}–50mV		V_{REF}–50mV	V
I_{OH}	High-level output current	A port		–8		–32	mA
I_{OL}	Low-level output current			8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz	A port		24		64	mA
		B port		15		40	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled			10		10	ns/V
T_{amb}	Operating free-air temperature range		–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0 to 3.6V; I_{OH} = –100µA	A port	V_{CC}–0.2	V_{CC}		V
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA	A port		0.07	0.2	V
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
		V_{CC} = 3.15V; I_{OL} = 40mA	B port		0.5	0.4	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins4 A port		0.1	20	µA
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
			B port				µA
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current, A outputs	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V	A port		10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$ = Don't care			1.0	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.06	0.09	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.06	0.09	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.2	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1				MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.5 1.9	2.3 2.9	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	1.5 1.5	2.2 2.6	3.5 3.9	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.5 1.5	2.2 2.9	3.3 4.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.0 1.0	2.3 1.6	3.9 2.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	2.9 2.4	4.1 3.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low An to CPAB or Bn to CPBA	4	1.5 1.5	0.4 0.6	ns
th(H) th(L)	Hold time, High or Low An to CPAB or Bn to CPBA	4	1.0 1.0	–0.5 –0.3	ns
ts(H) ts(L)	Setup time, High or Low Clock Low An to LEAB or Bn to LEBA	4	1.0 1.0	–0.5 –0.1	ns
th(H) th(L)	Hold time, High or Low Clock High An to LEAB or Bn to LEBA	4	1.5 1.5	0.1 0.5	ns
ts(H) ts(L)	Setup time $\overline{CEAB}$ before CPAB or $\overline{CEBA}$ before CPBA	4	1.5 1.0	0.3 –0.4	ns
th(H) th(L)	Hold time $\overline{CEAB}$ after CPAB or $\overline{CEBA}$ after CPBA	4	1.5 1.0	0.7 –0.3	ns
tw(H) tw(L)	Pulse width, High or Low CPAB or CPBA	1	2.0 2.0		ns
tw(H)	LEAB or LEBA pulse width, High	3	1.5		ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
		V_{CC} = 2.3V; I_{OH} = –8mA		1.7			
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.3V; I_{OL} = 24mA			0.3	0.5	
I_I	Input leakage current	V_{CC} = 2.7V; V_I = GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = 5.5V	I/O Data pins[4]		0.1	20	µA
		V_{CC} = 2.7V; V_I = V_{CC}			0.1	10	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}[6]	Bus Hold current A or B outputs	V_{CC} = 2.5V; V_I = 0.8V			90		µA
		V_{CC} = 2.5V; V_I = 2.0V			75		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			1	100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.09	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2.5	4.5	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.09	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.01	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
f_{MAX}	Maximum clock frequency	1				MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.9 2.5	3.0 3.7	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	2.0 2.0	3.1 3.5	4.6 5.2	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.0 2.0	3.4 4.0	5.0 5.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	2.0 1.0	3.3 2.1	4.8 3.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.0	2.6 1.9	4.2 3.4	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

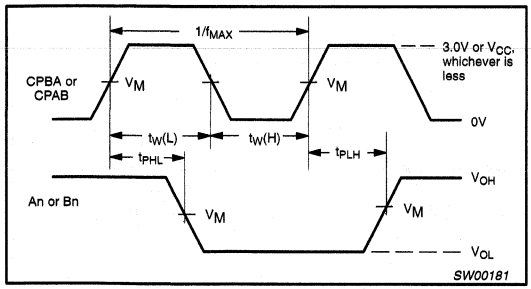
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low An to CPAB or Bn to CPBA	4	2.0 2.0	0.4 1.2	ns
th(H) th(L)	Hold time, High or Low An to CPAB or Bn to CPBA	4	0.0 0.0	–1.1 –0.3	ns
ts(H) ts(L)	Setup time, High or Low Clock Low or High An to LEAB or Bn to LEBA	4	0.0 1.5	–1.0 0.4	ns
th(H) th(L)	Hold time, High or Low Clock Low or High An to LEAB or Bn to LEBA	4	1.5 1.9	0.4 1.0	ns
ts(H) ts(L)	Setup time $\overline{CEAB}$ before CPAB or $\overline{CEBA}$ before CPBA	4	1.0 0.3	0.3 –0.4	ns
th(H) th(L)	Hold time $\overline{CEAB}$ after CPAB or $\overline{CEBA}$ after CPBA	4	2.0 0.5	0.4 –0.1	ns
tw(H) tw(L)	Pulse width, High or Low CPAB or CPBA	1	3.0 3.0		ns
tw(H)	LEAB or LEBA pulse width, High	3	1.5		ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

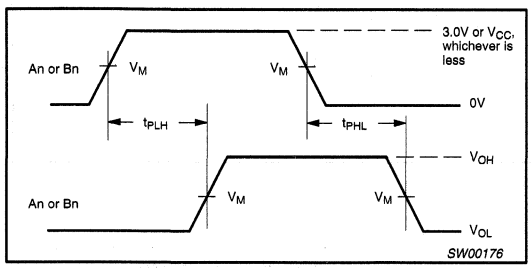
AC WAVEFORMS

NOTES:

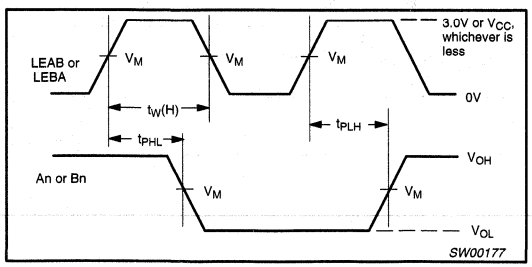
1. $V_M = 1.5V$ at $V_{CC} \geq 3.0V$, $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7V$. $V_M = 1.5V$ for A ports and control pins.; $V_M = 0.8V$ for B ports.
2. $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 3.0V$, $V_X = V_{OL} + 0.150V \cdot V_{CC}$ at $V_{CC} \leq 2.7V$
3. $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 3.0V$, $V_Y = V_{OH} - 0.150V \cdot V_{CC}$ at $V_{CC} \leq 2.7V$



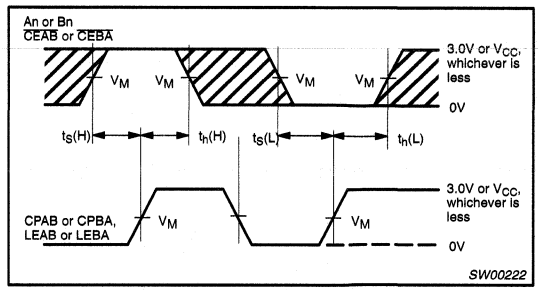
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



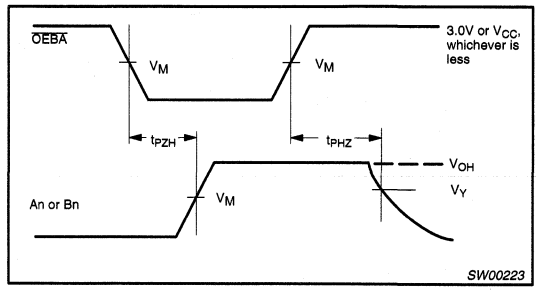
Waveform 2. Propagation Delay, Transparent Mode



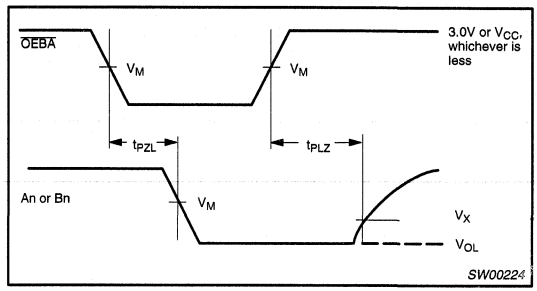
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 4. Data Setup and Hold Times

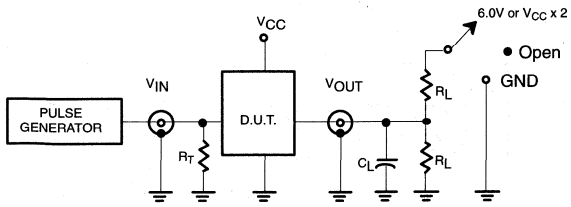


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

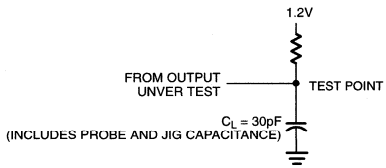


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

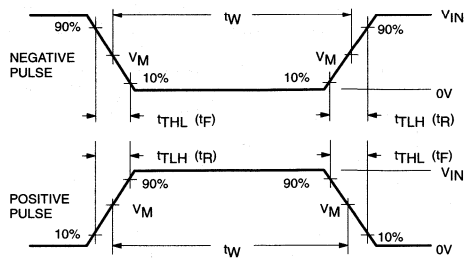
TEST CIRCUIT



Test Circuit for A Outputs



Load Circuit for B Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74GTL16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SW00255

18-bit LVTTL-to-GTL and transceivers 74GTL16622

FEATURES

- Translates between GTL/GTL + signal levels and LVTTL.
- Supports GTL/GTL + signal operation on B port.
- D-type flip-flops with qualified storage enable.
- Bus-hold data inputs eliminate the need for external pullup or pulldown resistors on A port.
- Flow-through architecture facilitates printed-circuit-board layout
- Low quiescent supply current

DESCRIPTION

These 18-bit registered bus transceivers contain two sets of D-type flip-flops for temporary storage of data flowing in either direction.

The B port operates at GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) and GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) levels, while the A port and control inputs are compatible with LVTTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock(CLKAB and CLKBA) inputs. The clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs are designed to control each 9-bit transceiver independently, which makes the device more versatile.

For A-to-B data flow, the devices operate on the Low-to-High transition of CLKAB if $\overline{CEAB}$ is low. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B, but uses $\overline{OEBA}$, CLKBA and $\overline{CEBA}$.

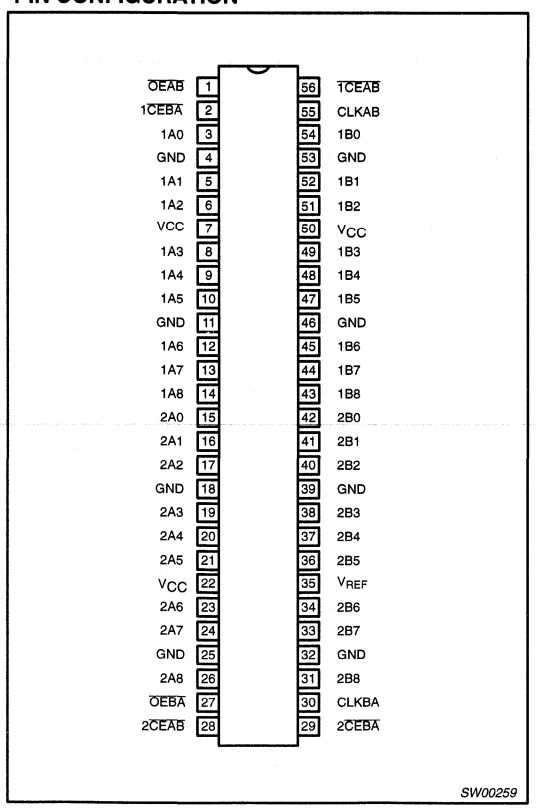
Active bus hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by current-sinking capability of the driver.

ORDERING INFORMATION

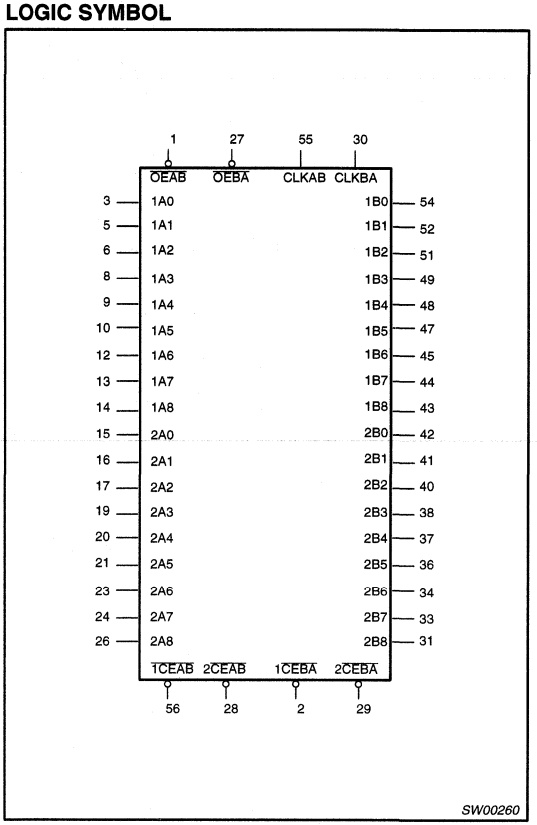
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74GTL16622	GTL16622 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74GTL16622	GTL16622 DGG	SOT364-1

PIN CONFIGURATION



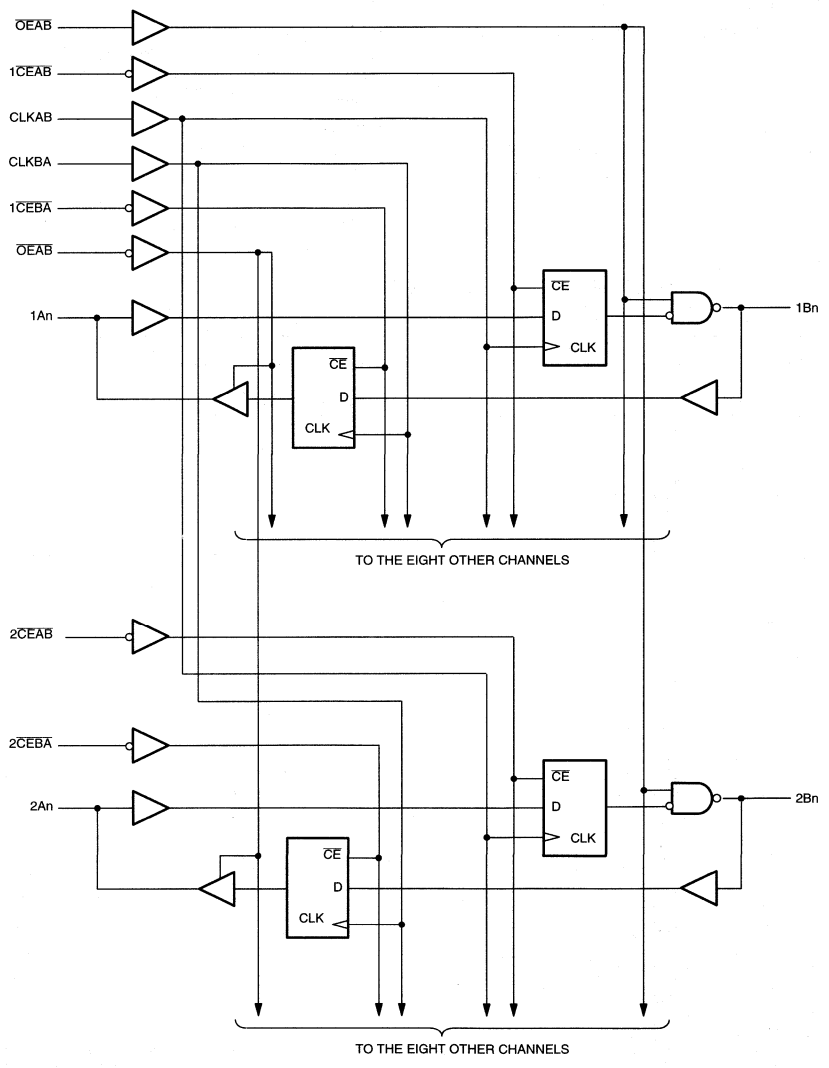
SW00259

LOGIC SYMBOL



SW00260

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT	MODE
$\overline{CEAB}$	$\overline{OEAB}$	CLKAB	A	B	
X	H	X	X	Z	
H X	L L	X H or L	X X	B_O[2] B_O[2]	Latched storage of A data
L L	L L	↑ ↑	L H	L H	Clocked storage of A data

NOTES:
1. A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, CLKBA and $\overline{CEBA}$.
2. Output level before the indicated steady-state input conditions are established.

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low to High

ABSOLUTE MAXIMUM RATINGS [1]

In accordance with the Absolute Maximum Rating System (IEC 134). See Note 1; voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
V_I	Input voltage range, A port[3]		−0.5 to +V_{CC} + 0.5	V
V_I	Input voltage range, B port[3]		−0.5 to +5.5	V
V_O	Voltage range applied to any output in the high or power-off state, A port/B port[3]		−0.5 to +V_{CC} + 0.5	V
I_{OH}	Current into any output in the high state	A port	−50	mA
I_{OL}	Current into any output in the low state	A port	50	mA
		B port	100	
I_{IK}	Input clamp current	V_I < 0	−50	mA
I_{OK}	Output clamp current	V_O < 0	−50	mA
P_{tot}	Power dissipation per package	for temperature range: −40 to +125 °C		mW
	plastic medium-shrink (SSOP)	above +55 °C derate linearly with 11.3 mW/K	850	
	plastic thin-medium-shrink (TSSOP)	above +55 °C derate linearly with 8 mW/K	600	
T_{stg}	Storage temperature range		−60 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER		MIN	MAX	MAX	UNIT
V_{CC}	DC supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1.0	1.10	
V_I	Input voltage	B port	0		V_{TT}	V
		Except B port	0		5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50mV	V
		Except B port			0.8	
I_{OH}	High-level output current	A port			–50	mA
I_{OL}	Low-level output current	A and B port			50	mA
T_{amb}	Operating free-air temperature		–40		+85	°C

NOTES:
1. Unused control inputs must be held high or low to prevent them from floating.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{OH}	High-level output voltage	V_{CC} = 3.15V; I_{OH} = –100µA	A port	V_{CC}–0.2	–	–	V
		V_{CC} = 3.15V; I_{OH} = –12mA		V_{CC}–0.5	–	–	
		V_{CC} = 3.15V; I_{OH} = –24mA		V_{CC}–0.8	–	–	
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 100µA	A port	–	–	0.2	V
		V_{CC} = 3.0V; I_{OL} = 12mA		–	–	0.4	
		V_{CC} = 3.0V; I_{OL} = 24mA		–	–	0.5	
V_{OL}	Low–level output voltage	V_{CC} = 3.15V; I_{OL} = 10mA	B port	–	–	0.2	V
		V_{CC} = 3.15V; I_{OL} = 40mA		–	–	0.4	
		V_{CC} = 3.15V; I_{OL} = 50mA		–	–	0.55	
I_I	Input leakage current	V_{CC} = 3.45V; V_I = V_{CC} or GND	Control pins	–	–	±5	µA
		V_{CC} = 3.45V; V_I = V_{TT} or GND	B port	–	–	±5	
$I_{I(HOLD)}$	Bus Hold current, A outputs	V_{CC} = 3.15V; V_I = 0.8V	A port	75	–	–	µA
		V_{CC} = 3.15V; V_I = 2.0V		–75	–	–	
		V_{CC} = 3.45V[2]; V_I =0.8 to 2.0V		–	–	±500	
I_{OZH}		V_{CC} = 3.45V; V_O = 1.5V	B port	–	–	10	µA
I_{OZ}[4]		V_{CC} = 3.45V; V_O = V_{CC} or GND	A port	–	–	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.45V; V_I = V_{CC} or GND; I_O = 0	A or B port	–	–	20	mA
ΔI_{CC}[4]	Additional supply current per input pin	V_{CC} = 3.45V; V_I = V_{CC} – 0.6	A port or control inputs	–	–	500	µA
C_I		V_I = 3.15V or 0	Control inputs	–	3		pF
C_{IO}		V_O = 3.15V or 0	A port	–	10		pF
		Per IEEE 1194.1	B port	–	8.5		

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the bus hold maximum dynamic current required to switch the input from one state to another.
3. For I/O ports, the parameter I_{OZ} includes the input leakage current.
4. This is the increase in supply current for each input that is at the specified TLL voltage level rather than V_{CC} or GND.

AC CHARACTERISTICS FOR GTL

Over recommended ranges of supply voltage[1]

SYMBOL	PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency		0	200	MHz
t_W	Pulse duration, CLK high or low		2.5		ns
t_{SU}	Setup time	Data before CLK ↑	2.0		ns
		$\overline{CE}$ before CLK ↑	1.0		
t_h	Hold time	Data after CLK ↑	0		ns
		$\overline{CE}$ after CLK ↑	0		

SYMBOL	FROM (INPUT)	TO (OUTPUT)	MIN	TYP[2]	MAX	UNIT
f_{MAX}			200			MHz
t_{PLH}	CLKAB	B		1.7	2.7	ns
t_{PHL}				1.7	2.7	
t_{PLH}	$\overline{OEAB}$	B		1.5	2.4	ns
t_{PHL}				1.5	2.4	
Slew rate	Both transitions			0.7		V/ns
t_r	Transition time, B outputs (0.6 V to 1 V)		0.7	0.8	1.2	ns
t_f	Transition time, B outputs (1 V to 0.6 V)		0.4	0.5	0.6	ns
t_{PLH}	CLKAB	A		2.7	3.8	ns
t_{PHL}				2.7	3.8	
t_{enable}	$\overline{OEAB}$	A		2.5	4.0	ns
$t_{disable}$				2.5	4.0	

NOTES:

1. These parameters are warranted but not production tested.
2. All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR GTL+

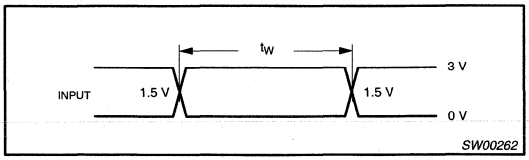
Over recommended ranges of supply voltage[1]

SYMBOL	PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency		0	200	MHz
t_W	Pulse duration, CLK high or low		2.5		ns
t_{SU}	Setup time	Data before CLK ↑	2.0		ns
		$\overline{CE}$ before CLK ↑	1.0		
t_h	Hold time	Data after CLK ↑	0		ns
		$\overline{CE}$ after CLK ↑	0		

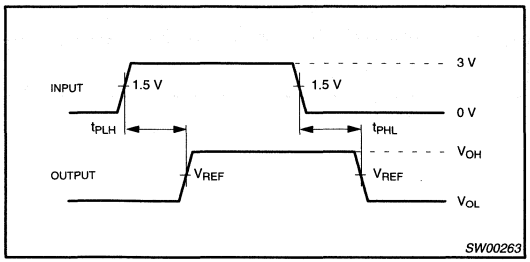
SYMBOL	FROM (INPUT)	TO (OUTPUT)	MIN	TYP[2]	MAX	UNIT
f_{MAX}			200			MHz
t_{PLH}	CLKAB	B		1.8	2.8	ns
t_{PHL}				1.8	2.8	
t_{PLH}	$\overline{OEAB}$	B		1.5	2.5	ns
t_{PHL}				1.5	2.5	
Slew rate	Both transitions			0.8		V/ns
t_r	Transition time, B outputs (0.6 V to 1.3V)		0.8	1.2	2.2	ns
t_f	Transition time, B outputs (1 V to 0.6 V)		0.5	0.7	1.0	ns
t_{PLH}	CLKAB	A		2.7	3.8	ns
t_{PHL}				2.7	3.8	
t_{enable}	$\overline{OEAB}$	A		2.5	4.0	ns
$t_{disable}$				2.5	4.0	

NOTES:
1. These parameters are warranted but not production tested.
2. All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25°C.

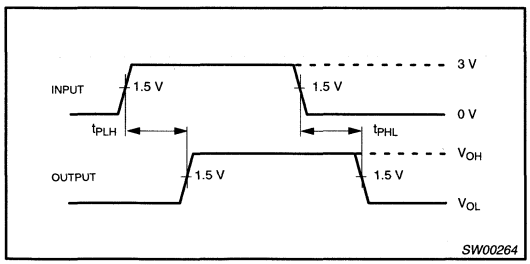
AC WAVEFORMS



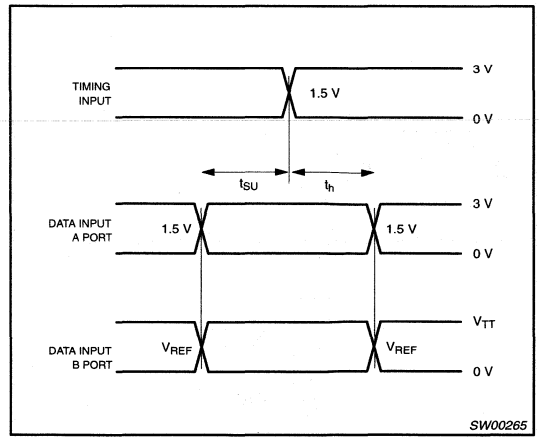
Waveform 1. Voltage waveforms pulse duration



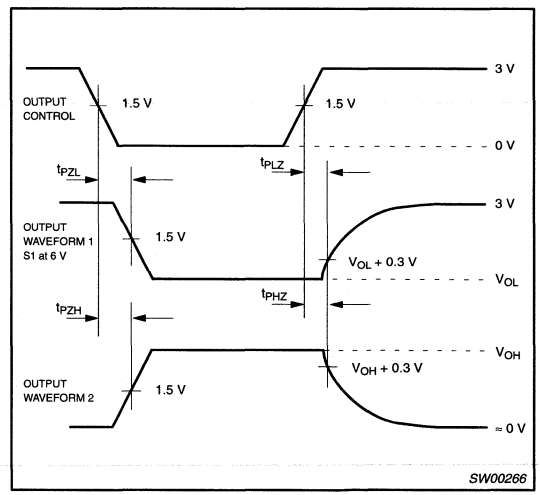
Waveform 2. Voltatage waveforms propagation times. (CLKAB to B port)



Waveform 3. Voltage waveforms propagation delay times (CLKBA to A port)

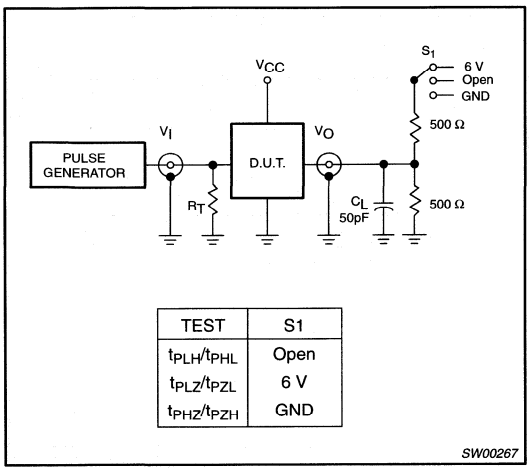


Waveform 4. Voltage waveforms setup and hold times



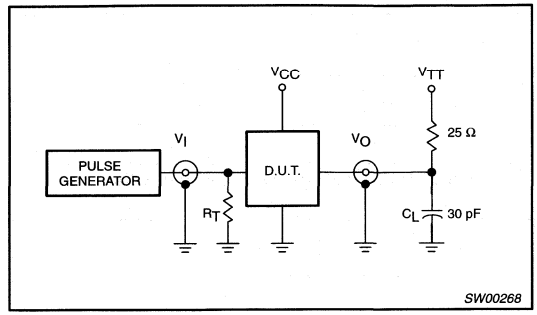
Waveform 5. Voltages waveforms enable and disable times (A port)

LOAD CIRCUIT FOR A OUTPUTS



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR B OUTPUTS



Section 6
3.3V/5V Devices
PLD

BiCMOS Bus Interface Logic

CONTENTS

5V high-speed universal PLD device with live insertion capability

ABT22V10A5, A7

DESCRIPTION

The ABT22V10A is a versatile PAL® device fabricated on Philips BiCMOS process known as QUBiC.

The QUBiC process produces very high speed, 5 volt devices (5.0ns) which have excellent noise immunity. The ground bounce of an output held low while the 9 remaining outputs are switching is less than 1.0V (typical).

The ABT22V10A outputs are designed to support Live Insertion/Extraction into powered-up systems. The output is specially designed so that during V_{CC} ramp, the output remains 3-Stated until $V_{CC} \approx 2.1V$. At that time, the outputs become fully functional, depending upon device inputs. (See DC Electrical Characteristics, Symbol $I_{PU/PD}$, Page 1303).

The ABT family of devices have virtually no ground bounce— less than 1.0 volts V_{OLP}, measured on an unswitched output (9 remaining outputs switching, each with a 50pF load tied to ground).

The ABT family of devices has been designed with high drive outputs (48mA sink and 16mA source currents), which allow for direct connection to a backplane bus. This feature eliminates the need for additional, standalone bus drivers, which are traditionally required to boost the drive of a standard 16/–4mA PLDs.

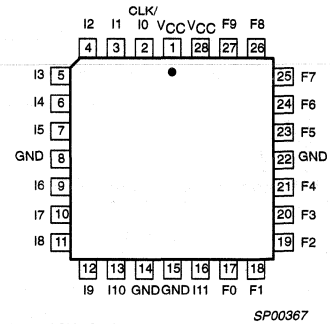
Philips has developed a new means of testing the integrity of fuses, both blown and intact fuses, which insures that all the fuses have been correctly programmed and that each and every fuse—whether "blown" or "intact"—is at the appropriate and optimal fuse resistance. This dual verify scheme represents a significant improvement over single reference voltage comparison schemes that have been used for bipolar devices since the late 1980's.

The ABT22V10A uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-products equations.

This device has a programmable AND array, which drives a fixed OR array. The OR sum-of-products feeds an "Output Macro Cell" (OMC) that can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback.

PIN CONFIGURATIONS

A Package



A = Plastic Leaded Chip Carrier

PIN LABEL DESCRIPTIONS

SYMBOL	FUNCTION
I1 – I11	Dedicated Input
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground

FEATURES

- Fastest 5V 22V10
- Low ground bounce (<1.0V typical)
- Live insertion/extraction permitted
- High output drive capability: 48mA/–16mA
- Varied product term distribution with up to 16 product terms per output for complex functions
- Metastable hardened flip-flops
- Programmable output polarity
- Design support provided for third party CAD development and programming hardware
- Improved fuse verification circuitry increases reliability

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
28-Pin Plastic Leaded Chip Carrier	ABT22V10A5A (5ns device) ABT22V10A7A (7.5ns device)	SOT261-3

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage[2]	–0.5	+7.0	V_{DC}
V_{IN}	Input voltage[2]	–1.2	V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	–0.5	V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Except in programming mode.

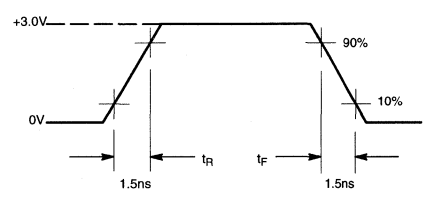
OPERATING RANGES

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

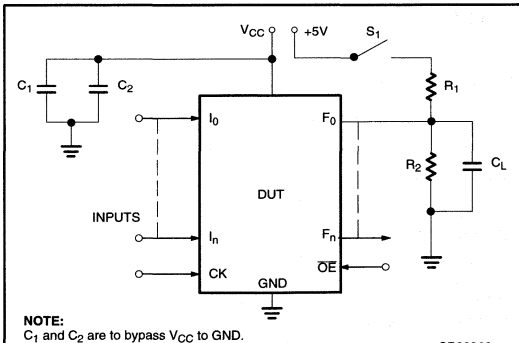
VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

DC ELECTRICAL CHARACTERISTICS

Over operating ranges.

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS MIN	LIMITS MAX	UNIT
Input voltage						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V
V_I	Clamp	V_{CC} = MIN, I_{IN} = −18mA			−1.2	V
Output voltage						
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = V_{IH} or V_{IL}	I_{OH} = −32mA	2.0		V
			I_{OH} = −16mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = V_{IH} or V_{IL}	I_{OL} = 48mA		0.5	V
Input current						
I_{IL}	Low	V_{CC} = MAX, V_{IN} = 0.4V			−10	µA
I_{IH}	High	V_{CC} = MAX, V_{IN} = 2.7V			10	µA
I_I	Max input current	V_{CC} = MAX, V_{IN} = 5.5V			20	µA
Output current						
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} <2.1V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; OE/$\overline{OE}$ = X			50	µA
		V_{CC} = MAX				
I_{OZH}	Output leakage[2]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 2.7V			20	µA
I_{OZL}	Output leakage[2]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} =0.4V			−20	µA
I_{SC}	Short circuit[3]	V_{OUT} = 0.5V		−30	−220	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX, Outputs enabled, V_I = V_{CC} or GND; I_O = 0			200	mA
Ground Bounce				**TYP**	**MAX**	**UNIT**
V_{OLP}	Minimum dynamic V_{OH} [5]	V_{CC} = MAX, 25°C, C_L = 50pF (including jig capacitance)		1.0	1.2	V

NOTES:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
3. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. This parameter is valid for any V_{CC} between 0V and 1.2 V with a transition time up to 10 mS. From V_{CC} = 1.2 to V_{CC} = 5.0V ±0.25V a transition time of 100 µS is permitted. X = Don't care.
5. Guaranteed by design, but not tested. Measured holding one output (the output under test) Low and simultaneously switching all remianing output from a High to a Low state. Switch S1 is closed; 50pF load.

AC ELECTRICAL CHARACTERISTICS[1]

$4.75V \leq V_{CC} \leq 5.25V$; $0°C \leq T_{amb} \leq +75°C$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				ABT22V10A5			ABT22V10A7			
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to non-registered output[2]	Active-LOW		2.0	4.5	5.0	2.0	6.0	7.5	ns
		Active-HIGH		2.0	4.5	5.0	2.0	6.0	7.5	ns
t_S	Setup time from input or SP to Clock			2.0	1.3		3.5	3.0		ns
t_{SIO}	Setup time from feedback to Clock			2.25	1.5		3.5	3.0		ns
t_H	Hold time			0			0			ns
t_{SKEWR}	Skew between registered outputs [4, 7]					1.0			1.0	ns
t_{CO}	Clock to output			2.0	3.5	4.0	2.0	4.5	5.5	ns
t_{CF}	Clock to feedback[3]				2.0	4.0		3.0	5.0	ns
t_{AR}	Asynchronous Reset to registered output					10.0			10.0	ns
t_{ARW}	Asynchronous Reset width			6.0			7.5			ns
t_{ARR}	Asynchronous Reset recovery time			4.0			5.5			ns
t_{SPR}	Synchronous Preset recovery time			4.5			5.0			ns
t_{WL}	Width of Clock LOW			2.0			3.0			ns
t_{WH}	Width of Clock HIGH			2.0			3.0			ns
f_{MAX}	Maximum frequency; External feedback $1/(t_S + t_{CO})$[4]			167	208		111	133		MHz
	Maximum frequency; Internal feedback $1/(t_S + t_{CF})$[4]			167	303		125	166		MHz
t_{EA}	Input to Output Enable[5]					8.0			8.0	ns
t_{ER}	Input to Output Disable[5]					7.5			7.5	ns
Capacitance[6]										
C_{IN}	Input Capacitance (Pin 2)	V_{IN} = 2.0V	V_{CC} = 5.0V, T_{amb} = 25°C, f = 1MHz		8			8		pF
	Input Capacitance (Others)	V_{IN} = 2.0V			4			4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V			8			8		pF

NOTES:

1. Test Conditions: $R_1 = 300\Omega$, $R_2 = 390\Omega$
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$ (including jig capacitance). $V_{IH} = 3V$, $V_{IL} = 0V$, $V_T = 1.5V$.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
7. Skew is measured with all outputs switching in the same direction.

5V high-speed universal PLD device with live insertion capability

ABT22V10A5, A7

PRODUCT FEATURES

Low Ground Bounce

The Philips Semiconductors BiCMOS QUBiC process produces exceptional noise immunity. The typical ground bounce, with 9 outputs simultaneously switching and the 10th output held low, is less than 1.0V. V_{OLP} is tested by holding one output (the output uncer test) in the Low state and then simultaneously switching all remaining outputs from a High to a Low state (each output is loaded with 50pF). The maximum peak voltage on the output under test is guaranteed to be less than 1.2 Volts.

Live Insertion/Extraction Capability

There are some inherent problems associated with inserting or extracting an unpowered module from a powered-up, active system. The ABT22V10A outputs have been designed such that any chance of bus contention, glitching or clamping is eliminated.

Detailed information on this feature is provided in an application note AN051: *Philips PLDs Support Live Insertion Applications.*

Improved Fuse Verification Circuitry Increases Reliability

Philips has developed a new means of testing the integrity of fuses, both blown and intact fuses, which insures that all the fuses have been correctly programmed and that each and every fuse – whether "blown" or "intact" – is at the appropriate and optimal fuse resistance. This dual verify scheme represents a significant improvement over single reference voltage comparisons schemes that have been used for bipolar devices since the late 1980s. Detailed information on this feature is provided in an application note entitled *Dual Verify Technique Increases Reliability of PLDs.*

Programmable 3-stage Outputs

Each output has a 3-Stage output buffer with 3-State control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macro cell output can be Active-HIGH or Active-LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the Output Macro Cell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be Active-HIGH ($S_0 = 1$).

Preset/Reset

For initialization, the ABT22V10A has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW, independent of the clock.

Note that Preset and Reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the ABT22V10A will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1–10µs maximum.

Security Fuse

After programming and verification, ABT22V10A designs can be secured by programming the security fuse link. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The ABT22V10A offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies programmability and functionality of the device to provide the highest programming and post-programming functional yields.

Technology

The BiCMOS ABT22V10A is fabricated with the Philips Semiconductors process known as QUBiC. QUBiC combines an advanced, state-of-the-art 1.0µm (drawn feature size) CMOS process with an ultra fast bipolar process to achieve superior speed and drive capabilities. QUBiC incorporates three layers of Al/Cu interconnects for reduced chip size, and our proven Ti-W fuse technology ensures highest programming yields.

Programming

The ABT22V10A is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ CUPL™ and PALASM® 90 design software packages also support the ABT22V10A architecture.

All packages allow Boolean and state equation entry formats, SNAP, ABEL and CUPL also accept, as input, schematic capture format.

Output Register Preload

The register on the ABT22V10A can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. The procedure for preloading follows:

1. Raise V_{CC} to 5.0V ± 0.25V.
2. Set pin 2 or 3 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock Pin 1 from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower pin 2 or 3 to V_{ILP}.
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

Metastable Characteristics

Philips provides complete data on the ABT22V10A5's metastable characteristics. While the ABT22V10A5 **does not** employ Philips patented metastable immune flip-flop, its metastabel characteristics are still quite favorable relative to competitive devices. For information on metastable immune PLDs, refer to the datasheets for the ABT22V10-7 for 5V applications or the LVT22V10-7 for 3.3V designs.

Design Example

Suppose a designer wants to use the ABT22V10A5 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), in a 5V system that has a clock frequency of 50MHz, at an ambient temperature of 25°C. The next device in the sytem samples the output fo the ABT22V10A5 5.5ns after the clock edge to ensure that any metastable conditions that occur have time to resolve to the correct state. The MTBF for this situatio can be calcuclated by using the equation below:

$$MTBF = e(t'/\tau)/T_0F_CF_1$$

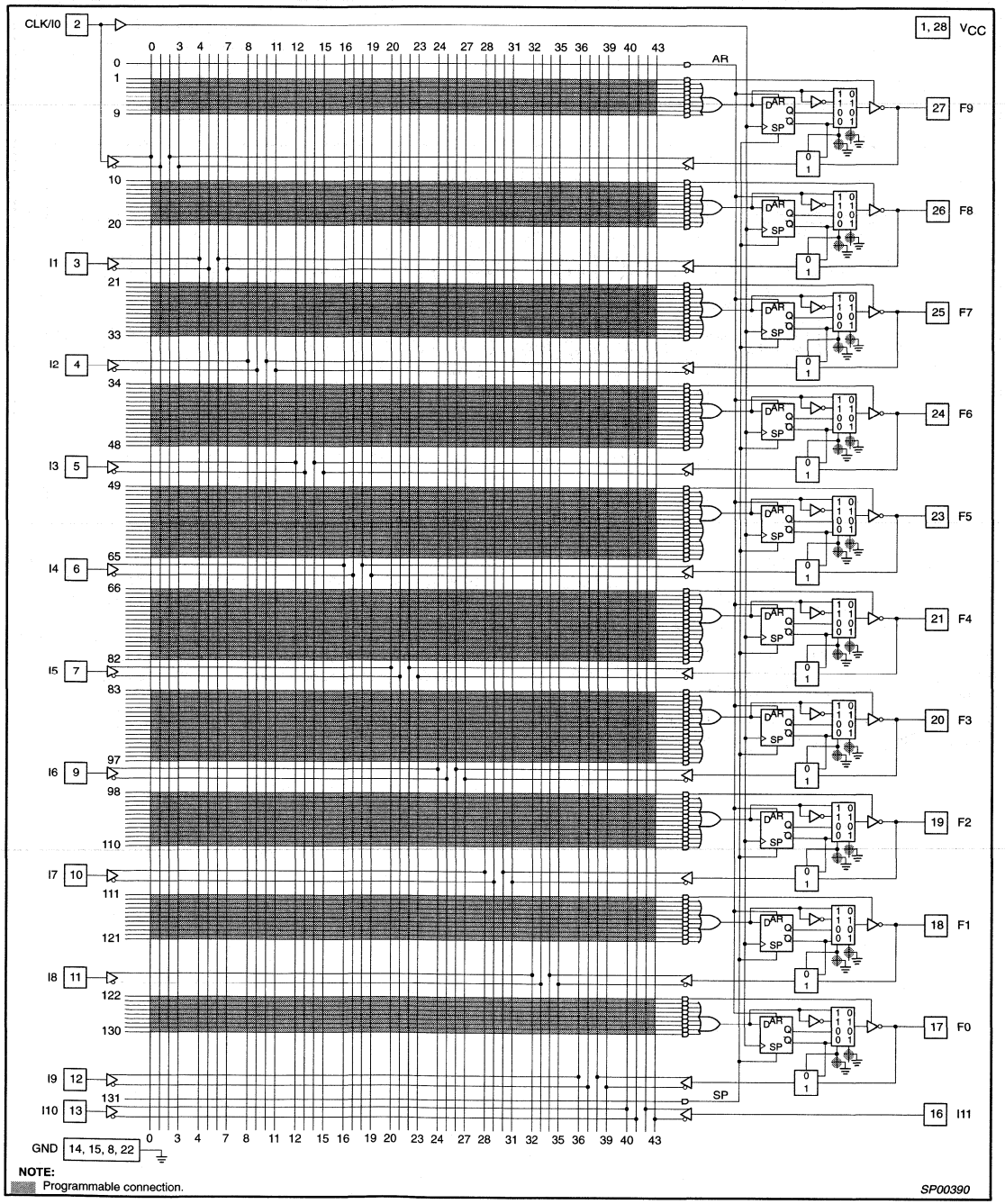
In this formula, F_C is the frequency of the clock, F_1 is the average input event frequency, and t′ is the time after the clock pulse that the output is sampled ($t' > T_{CO}$). T_0 and τ are device parameters provided by the semiconductor manufacturer (refer to Table 1 for the ABT22V10A5 metastability specifications). T_0 and τ are derived from tests and can be most nearly be defined as follows: τ is a function of the rate at which a latch in a metastable state resolves that condition. T_0 is a function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a normalization constant which is a very strong function of the normal propagation dely of the device.

In this situation, the F_1 will be twice that data frequency, or 20MHz, because input events consist of both low and high transitions. Thus in this case F_C is 50MHz, F_1 is 20MHz, τ is 85.6ps, t′ is 5.5ns, and T_0 is 4.55 seconds. Using the above formula, the actual MTBF for this situation is 1.76×10^{12} seconds, or 55,889 years for the ABT22V10A5.

Table 1. Typical Values for τ and T_0 at various V_{CC}'s and Temperatures

	0°C		+25°C		+75°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.25V	72.00ps	7.20E+01	96.70ps	4.59E–01	105.00ps	1.43E–01
5.00V	72.80ps	2.06E+02	85.60ps	4.55E+00	100.00ps	8.37E–01
4.75V	68.70ps	9.97E+03	81.70ps	4.85E+01	99.80ps	1.29E+00

LOGIC DIAGRAM



FUNCTIONAL DIAGRAM

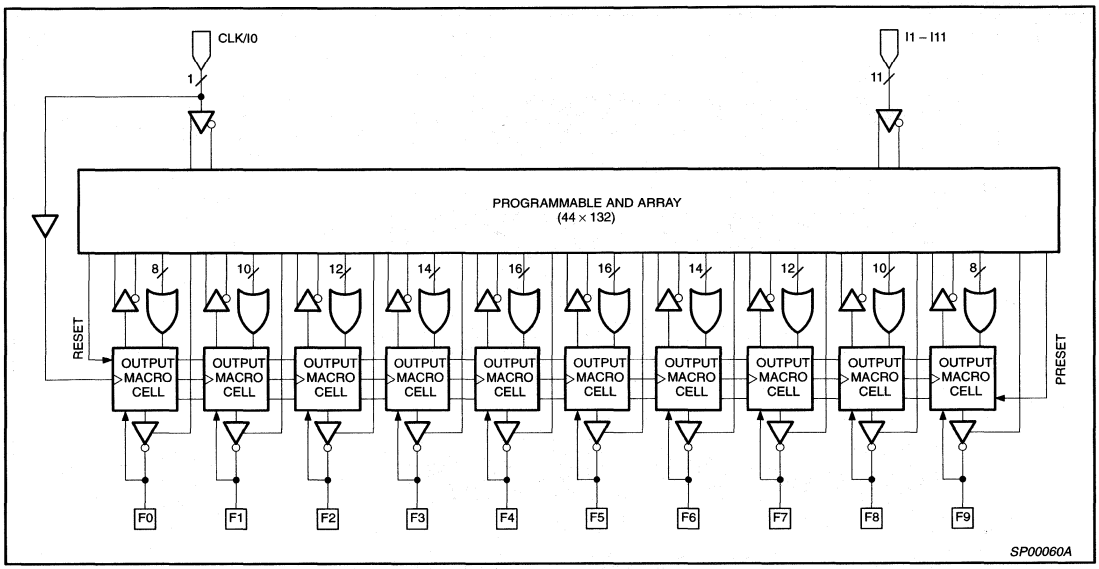


Figure 1. Functional Diagram

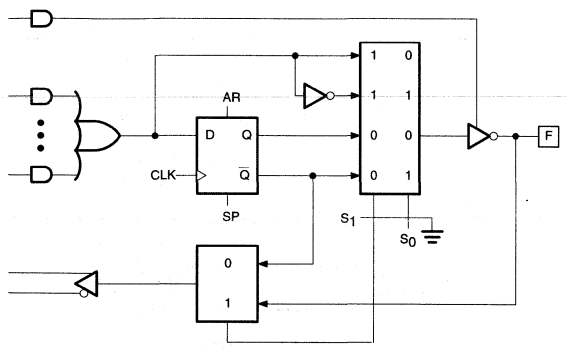
FUNCTIONAL DESCRIPTION

The ABT22V10A allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both True and Complement of any single input assume the logical LOW state.

The ABT22V10A has 12 inputs and 10 I/O Macro Cells (Figure 1). The Macro Cell allows one of four potential output configurations, registered output or combinatorial I/O, Active-HIGH or Active-LOW (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0–S_1. Multiplexer controls are connected to ground (0) through a programmable fuse link, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

OUTPUT MACRO CELL

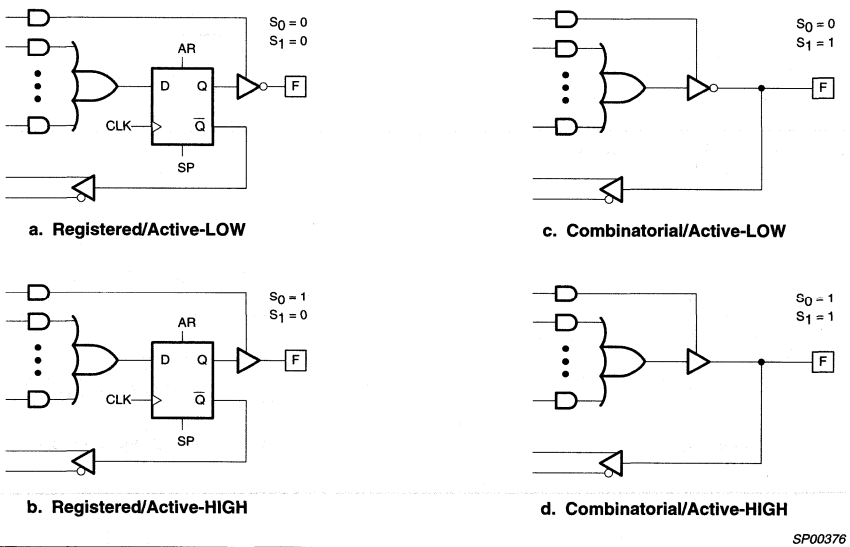


S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed fuse
1 = Programmed fuse

SP00375

Figure 2. Output Macro Cell Logic Diagram



SP00376

Figure 3. Output Macro Cell Configurations

Registered Output Configuration

Each Macro Cell of the ABT22V10A includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

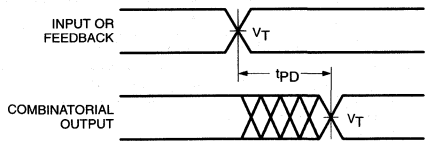
Any Macro Cell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration, the feedback is from the pin.

Variable Input/Output Pin Ratio

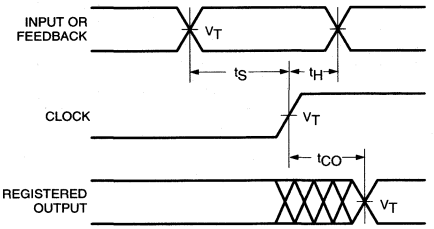
The ABT22V10A has twelve dedicated input lines, and each Macro Cell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity.

SWITCHING WAVEFORMS

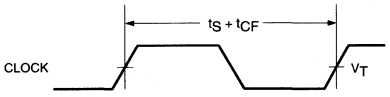
V_T = 1.5V.
Input pulse amplitude 0V to 3.0V.
Input rise and fall times 1.5ns max.



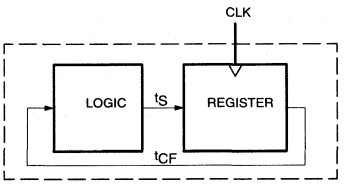
Combinatorial Output



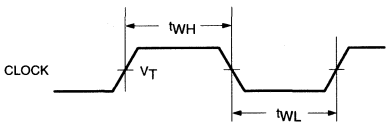
Registered Output



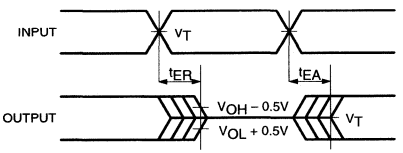
Clock to Feedback (f_{MAX} Internal) (See Path at Right)



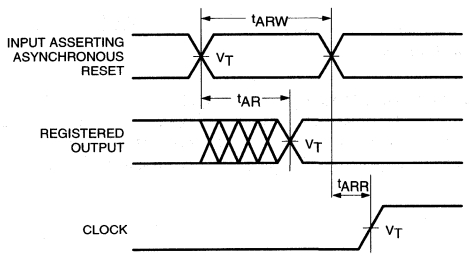
Clock to Feedback



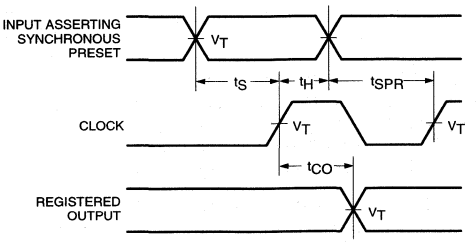
Clock Width



Input to Output Disable/Enable



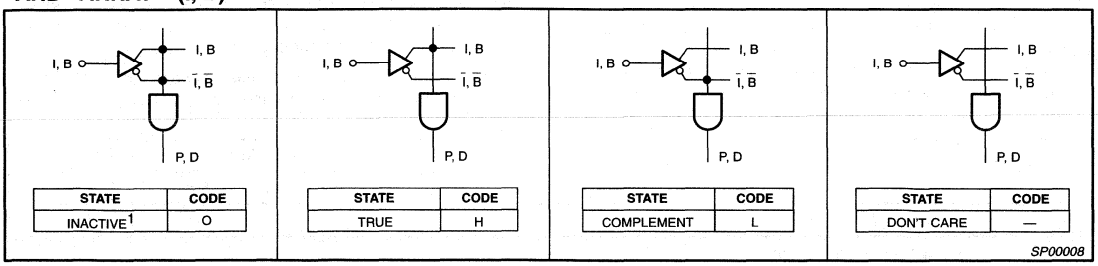
Asynchronous Reset



Synchronous Preset

SP00377

"AND" ARRAY – (I, B)



STATE	CODE
INACTIVE[1]	O

STATE	CODE
TRUE	H

STATE	CODE
COMPLEMENT	L

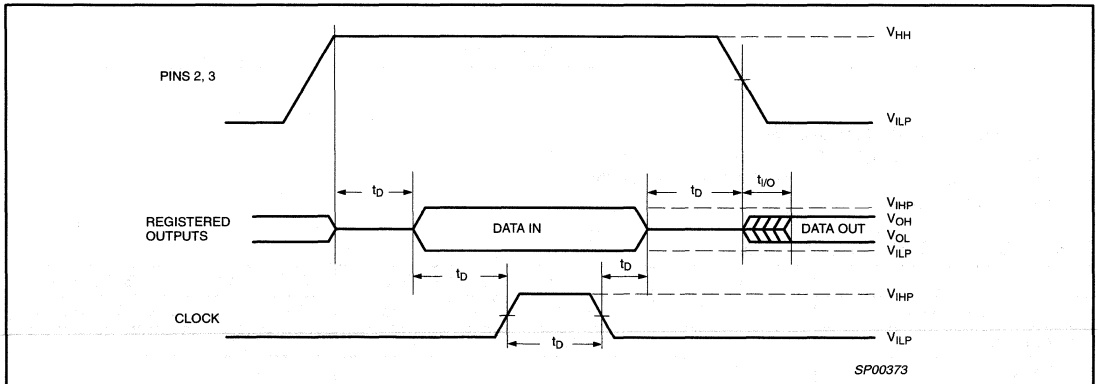
STATE	CODE
DON'T CARE	—

SP00008

NOTE:
1. This is the initial state.

PRELOAD SET-UP

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	REC	MAX	
V_{HH}	Super-level input voltage	9.5	9.5	10	V
V_{ILH}	Low-level input voltage	0	0	0.8	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	100	200	1000	ns
$t_{I/O}$	I/O valid after Pin 2 or 3 drops from V_{HH} to V_{ILP}	100			ns



SP00373

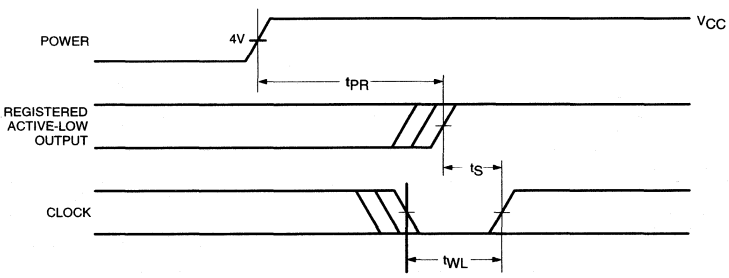
Output Register Preload Waveform

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{PR}	Power-up Reset Time		1	µs
t_S	Input or Feedback Setup Time	See AC Electrical Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveform SP00066

OTHER PHILIPS 22V10 DEVICES

Philips offers a complete family of 22V10 devices, addressing a wide variety of design applications. This Features Matrix summarizes the basic features of each specific device.

PHILIPS 22V10 FEATURES MATRIX

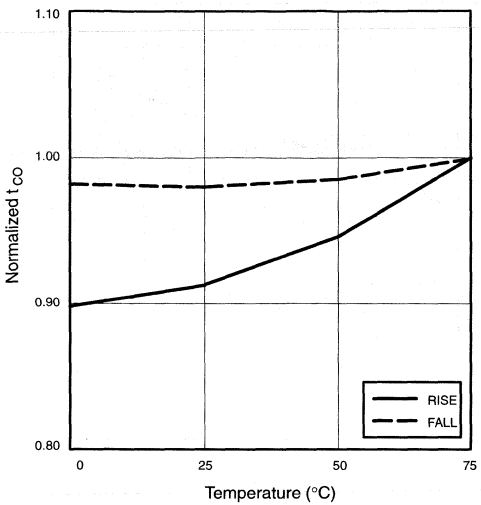
	PL22V10-10/-15	LVT22V10-7	ABT22V10-7	ABT22V10A5	ABT22V10A7
Operating supply voltage	+4.75 to +5.25V	+3.0 to +3.6V [1]	+4.75 to +5.25V	+4.75 to +5.25V	+4.75 to +5.25V
Live Insertion	No	Yes	No	Yes	Yes
Dual Verify	No	Yes	No	Yes	Yes
Metastability	No	Hardened	Immune	No	No
Source Drive Capability	4mA (V_{OH} = 2.4V)	16mA (V_{OH} = 2.0V)	16mA (V_{OH} = 2.4V)	16mA (V_{OH} = 2.4V)	16mA (V_{OH} = 2.4V)
Sink Drive Capability	16mA (V_{OL} = 0.5V)	32mA (V_{OL} = 0.5V)	48mA (V_{OL} = 0.5V)	48mA (V_{OL} = 0.5V)	48mA (V_{OL} = 0.5V)
Low Ground Bounce	No	Yes	Yes	Yes	Yes
Package Availability:					
Plastic Dual In-Line (N)	24-Pin	24-Pin	24-Pin	not available	not available
Plastic Leaded Chip Carrier (A)	24-Pin	28-Pin	28-Pin	28-Pin	28-Pin
Plastic Small Outline Large (D)	24-Pin	24-Pin	not available	not available	not available

NOTE:

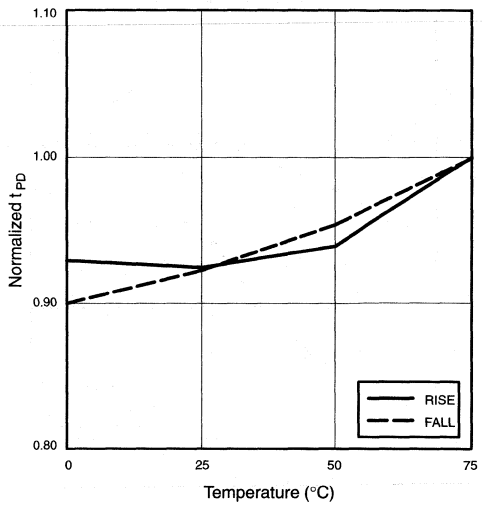
1. 5 volt compatible I/O. Inputs are capable of handling 7V and the outputs can also be pulled up to 7 volts.

ABT22V10A5 TIMING CHARACTERIZATION

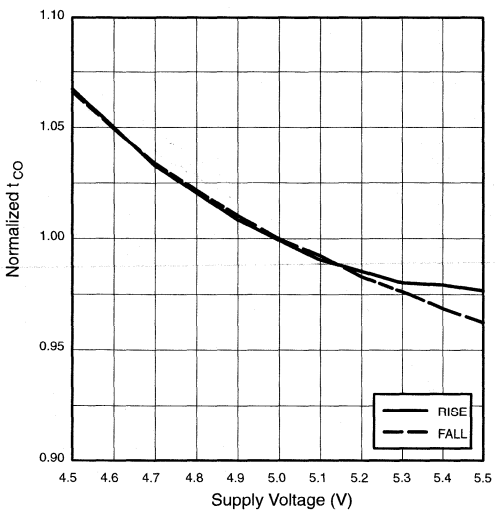
Normalized t_{CO} vs Temperature
(V_{CC} = 5.0V, output capacitance = 50pF, 5 outputs switching)



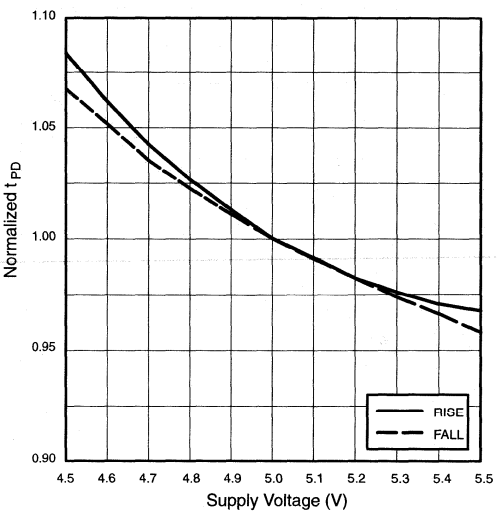
Normalized t_{PD} vs Temperature
(V_{CC} = 5.0V, output capacitance = 50pF, 5 outputs switching)



Normalized tCO vs VCC
(temp = 25°C, output capacitance = 50pF, 5 outputs switching)



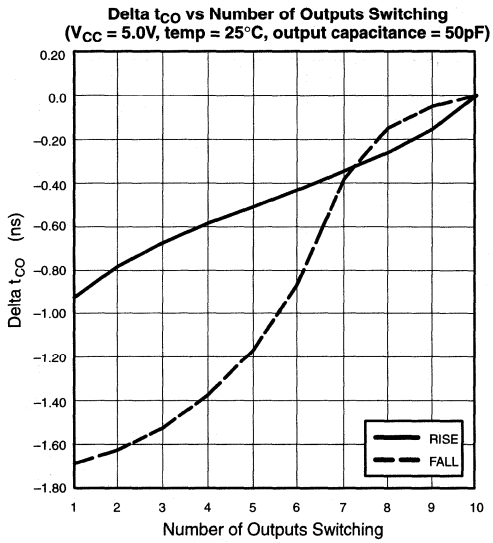
Normalized tPD vs VCC
(temp = 25°C, output capacitance = 50pF, 5 outputs switching)

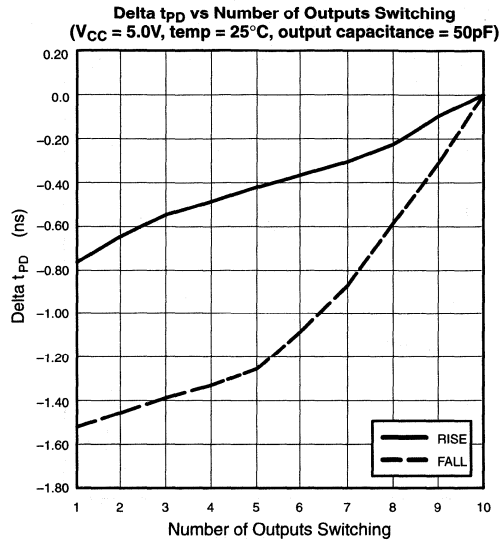


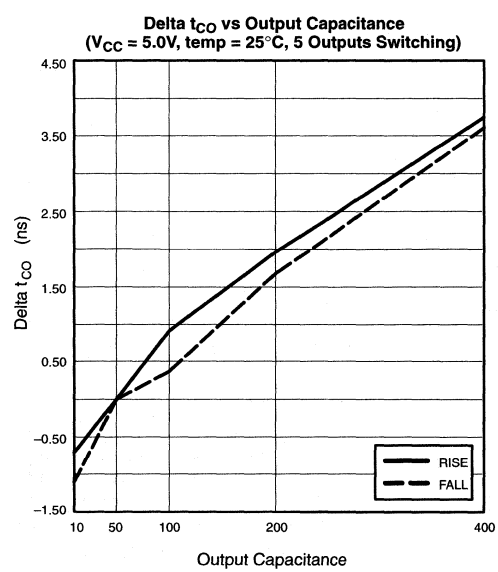
The timing characterization represents the average values of a representative sample for each parameter.
The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design.
Philips guarantees the MAX AC CHARACTERIZATION specifications.

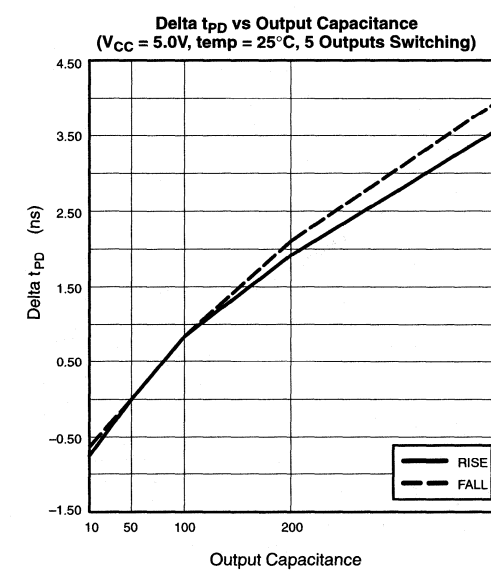
SP00370

ABT22V10A5 TIMING CHARACTERIZATION









The timing characterization represents the average values of a representative sample for each parameter.
The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design.
Philips guarantees the MAX AC CHARACTERIZATION specifications.

SP00371

3V high speed, universal PLD device — LVT22V10

FEATURES

- Fastest 3V PLD
- Supports 3/5V mixed systems
- Low ground bounce (<1.1V worst case)
- Live insertion/extraction permitted
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Metastable hardened device
- High output drive capability: 32mA/–16mA
- Varied product term distribution with up to 16 product terms per output for complex functions
- Programmable output polarity
- Available in 300 mil-wide 24-pin Plastic Small Outline Package
- Design support provided for third party CAD development and programming hardware

DESCRIPTION

The LVT22V10 is a versatile PAL® device fabricated on the Philips BiCMOS QUBiC process.

The QUBiC process produces very high speed 3V devices (7.5ns) which have excellent noise characteristics. Ground bounce of an output held low while the remaining 9 outputs switch from high to low is typically less than 0.7V. V_{CC} bounce of an output held high while the remaining 9 outputs switch from low to high is typically less than 1.0V.

The LVT22V10 was designed to support mixed 3/5V systems. The inputs are capable of handling 7V while the outputs can be pulled up to 7V.

The designer can interface directly from 5V outputs (CMOS full rail or totem pole) to a 3V LVT input. A 3V LVT output can drive a 5V TTL input directly, or in the case of a CMOS input, the LVT output can interface with the use of an external pull-up resistor. Finally, no external pull-up resistors are needed on unused input pins due to a bus-hold data structure designed into the LVT input.

The LVT22V10 has been designed with high drive outputs (32mA sink and 16mA source currents), which allows for direct connection to a backplane bus. This feature eliminates the need for additional, standalone bus drivers, which are traditionally required to boost the drive of a standard PLDs.

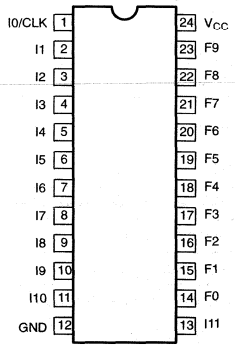
The LVT22V10 outputs are designed to support Live Insertion/Extraction into powered up systems. The output is specially designed so that during V_{CC} ramp, the output remains 3-Stated until $V_{CC} \approx 2.1V$. At that time the outputs become fully functional depending upon device inputs. (See DC Electrical Characteristics, Symbol $I_{PU/PD}$, Page 1318). In addition when an LVT22V10 output is tied to a 5V bus, no bus current is loaded.

The LVT22V10 uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-products equations.

This device has a programmable AND array which drives a fixed OR array. The OR sum of products feeds an "Output Macro Cell" (OMC) which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback.

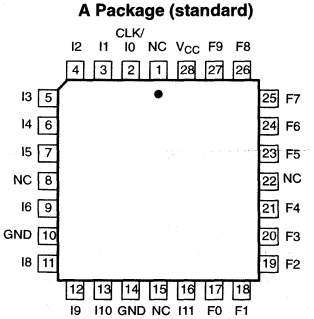
PIN CONFIGURATIONS

D and N Packages



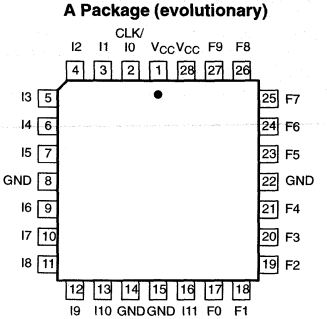
N = Plastic Dual In-Line Package (300mil-wide)
D = Plastic Small Outline Large (300mil-wide) Package

A Package (standard)



A = Plastic Leaded Chip Carrier

A Package (evolutionary)



A = Plastic Leaded Chip Carrier

SP00436

®PAL is a registered trademark of Advanced Micro Devices, Inc.

ORDERING INFORMATION

PACKAGES	ORDER CODE	DWG NUMBER
24-Pin Plastic DIP (300mil)	LVT22V10-7N (8.0ns device)	SOT222-1
28-Pin PLCC (standard pinout)	LVT22V10B7A (7.5ns device)	SOT261-3
28-Pin PLCC (evolutionary pinout)	LVT22V10-7A (7.5ns device)	SOT261-3
24-Pin Plastic SOL	LVT22V10-7D (8.0ns device)	SOT137-1

PIN LABEL DESCRIPTIONS

SYMBOL	DESCRIPTION
I1 – I11	Dedicated Input
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

OPERATING RANGES

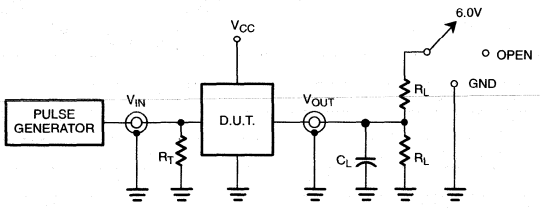
SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	+3.0	+3.6	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage[2]	–0.5	+4.6	V_{DC}
V_{IN}	Input voltage[2]	–0.5	7	V_{DC}
V_{OUT}	Output voltage[3]	–0.5	5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Except in programming mode.
3. Outputs can be pulled up to 7V via external pull-up resistor.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

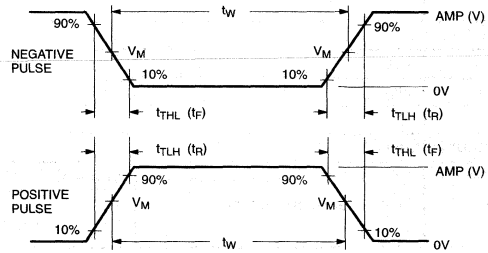
TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
LVT	3.0V	10MHz	500ns	2.5ns	2.5ns

SP00385

DC ELECTRICAL CHARACTERISTICS

Over operating ranges.

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS MIN	LIMITS MAX	UNIT
Input voltage						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V
V_I	Clamp	V_{CC} = MIN, I_{IN} = –18mA			–1.2	V
Output voltage						
V_{OH}	High-level output voltage	V_{CC} = MIN to MAX, V_I = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC}–0.2		V
		V_{CC} = MIN, V_I = V_{IH} or V_{IL}	I_{OH} = –16mA	2.0		V
			I_{OH} = –5.5 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN to MAX, V_I = V_{IH} or V_{IL}	I_{OL} = 100µA		0.2	V
		V_{CC} = MIN, V_I = V_{IH} or V_{IL}	I_{OL} = 32 mA		0.5	V
			I_{OL} = 16 mA		0.4	V
Input current						
I_{IL}	Low	V_{CC} = MAX, V_{IN} = 0.0V			–10	µA
I_{IH}	High	V_{CC} = MAX, V_{IN} = V_{CC}			10	µA
I_I	Max input current	V_{CC} = MAX, V_{IN} = 5.5V			10	µA
I_I	Pin 1 (program)	V_{CC} = MAX, V_{IN} = 5.5V			20	µA
I_{BHL}	Bus hold low sustaining current[2]	V_{CC} = 3V, V_I = 0.8V		75		µA
I_{BHH}	Bus hold high sustaining current[3]	V_{CC} = 3V, V_I = 2V		–75		µA
I_{BHLO}	Bus hold low overdrive current[4, 9]	V_{CC} = 3.6V		500		µA
I_{BHHO}	Bus hold high overdrive current[5, 9]	V_{CC} = 3.6V		–500		µA
Output current						
I_{OFF}	Output off current	V_{CC} = 0V, V_I or V_O = 0 to 4.5V			±10	µA
I_{EX}	Current into an output in high state when V_O > V_{CC}	V_O = 5.5V, V_{CC} = 3.0V			±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[8]	V_{CC} <1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; OE/$\overline{OE}$ = X			100	µA
		V_{CC} = MAX				
I_{OZH}	Output leakage[6]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 5.5V			10	µA
I_{OZL}	Output leakage[6]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} =0V			–10	µA
I_{SC}	Short circuit[7]	V_{OUT} = 0.5V		–30	–220	mA
I_{CC}	V_{CC} supply current	V_{CC} = 3.6V, Outputs enabled, V_I = V_{CC} or GND; I_O = 0			170	mA
Ground/V_{CC} Bounce				**MIN**	**TYP**	**MAX**	**UNIT**
V_{OHV}	Maximum dynamic V_{OH}	V_{CC} = 3.0V, 25°C, C_L = 50pF (including jig capacitance)		2.2	2.3		V
V_{OLP}	Maximum dynamic V_{OL}	V_{CC} = 3.3V, 25°C, C_L = 50pF (including jig capacitance)	LVT22V10-7		0.7	1.1	V
			LVT22V10B7		1.0	1.1	V

NOTES:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} MAX. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} MAX.
3. The bus hold circuit can source at least the minimum high sustaining current at V_{IH} MIN. I_{BHL} should be measured after raising V_{IN} to V_{CC} and then lowering it to $V_{IH\ MIN}$.
4. An external driver must source at least I_{BHLO} to switch this node from low to high.
5. An external driver must sink at least I_{BHHO} to switch this node from high to low.
6. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
7. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
8. This parameter is valid for any V_{CC} between 0V and 1.2 V with a transition time up to 10 mS. From V_{CC} = 1.2 to V_{CC} = 3.3V ±0.3V a transition time of 100 µS is permitted. X = Don't care.
9. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where input current may be affected.

AC ELECTRICAL CHARACTERISTICS

Over commercial operating temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP	MAX	
t_{PD}	Input or feedback to non-registered output[2] PLCC package	Active-LOW				7.5	ns
		Active-HIGH				7.5	ns
	Input or feedback to non-registered output[2] DIP and SOL packages	Active-LOW				8.0	ns
		Active-HIGH				8.0	ns
t_S	Setup time from input, feedback or SP to Clock			5.5			ns
t_H	Hold time			0			ns
t_{CO}	Clock to output					5.0	ns
t_{CF}	Clock to feedback[3]					3.0	ns
t_{AR}	Asynchronous Reset to registered output					12.0	ns
t_{ARW}	Asynchronous Reset width			5.0			ns
t_{ARR}	Asynchronous Reset recovery time			5.0			ns
t_{SPR}	Synchronous Preset recovery time			5.0			ns
t_{WL}	Width of Clock LOW			3.0			ns
t_{WH}	Width of Clock HIGH			3.0			ns
f_{MAX}	Maximum frequency; External feedback $1/(t_S + t_{CO})$[4]			95			MHz
	Maximum frequency; Internal feedback $1/(t_S + t_{CF})$[4]			118			MHz
t_{EA}	Input to Output Enable[5]					8.5	ns
t_{ER}	Input to Output Disable[5]					8.5	ns
Capacitance[6]							
C_{IN}	Input Capacitance (Pin 1)	V_{IN} = 2.0V	V_{CC} = 3.3V, T_{amb} = 25°C, f = 1MHz		6		pF
	Input Capacitance (Others)	V_{IN} = 2.0V			6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V			8		pF

NOTES:

1. Test Conditions: R_1 = 500Ω, R_2 =500Ω
2. t_{PD} is tested with switch S_1 open and C_L = 50pF (including jig capacitance). V_{IH} = 3V, V_{IL} = 0V, V_T = 1.5V.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.3V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.3V)$ level with S_1 closed.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

PRODUCT FEATURES

Low Ground Bounce

The Philips Semiconductors BiCMOS QUBiC process results in exceptional noise immunity. Ground bounce is noise that is generated on a non-switching active low output when other outputs on the device switch from high to low. The worst case condition occurs when 9 outputs simultaneously switch from high to low and the tenth output is active low. The ground bounce on this tenth output for Philips LVT22V10 is typically less than 0.7V.

V_{CC} Bounce

V_{CC} bounce occurs on a non-switching active high output when other outputs are making a low to high transition. This specification is important to consider in 3.3V designs because of the reduced noise margin between V_{CC} and V_{OH} of only 1.3V relative to the traditional 5V system's noise margin of 3V. The Philips LVT22V10 V_{CC} bounce of an output held high while the remaining 9 outputs switch from low to high is typically less than 1.0V in magnitude.

Live Insertion/Extraction Capability

There are some inherent problems associated with inserting or extracting an unpowered module from a powered-up, active system. The LVT22V10 outputs have been designed such that any chance of bus contention, glitching or clamping is eliminated.

Detailed information on this feature is provided in an application note AN051: *Philips PLDs Support Live Insertion Applications.*

Bus Hold Input Structure

Bus Hold is a feature that maintains the input state of the device by incorporating a weak latch into the input structure. This latch maintains the input state until a minimum level of current (called the overdrive current) is supplied to change the input state. This is useful in bus applications where the bus is placed into a high impedance state. The LVT22V10's inputs, in this high impedance situation, maintain valid logic levels until the bus is actively driven to a new state.

Improved Fuse Verification Circuitry Increases Reliability

Philips has developed a new means of testing the integrity of fuses, both blown and intact fuses, which insures that all the fuses have been correctly programmed and that each and every fuse – whether "blown" or "intact" – is at the appropriate and optimal fuse resistance. This dual verify scheme represents a significant improvement over single reference voltage comparisons schemes that have been used for bipolar devices since the late 1980s. Detailed information on this feature is provided in an application note entitled *Dual Verify Technique Increases Reliability of PLDs.*

Programmable 3-stage Outputs

Each output has a 3-Stage output buffer with 3-State control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macro cell output can be Active-HIGH or Active-LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the Output Macro Cell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be Active-HIGH ($S_0 = 1$).

Preset/Reset

For initialization, the LVT22V10 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW, independent of the clock.

Note that Preset and Reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the LVT22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1–10μs maximum.

Security Fuse

After programming and verification, LVT22V10 designs can be secured by programming the security fuse link. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The LVT22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies programmability and functionality of the device to provide the highest programming and post-programming functional yields.

Technology

The BiCMOS LVT22V10 is fabricated with the Philips Semiconductors process known as QUBiC. QUBiC combines an advanced, state-of-the-art 1.0μm (drawn feature size) CMOS process with an ultra fast bipolar process to achieve superior speed and drive capabilities. QUBiC incorporates three layers of Al/Cu interconnects for reduced chip size, and our proven Ti-W fuse technology ensures highest programming yields.

Programming

The LVT22V10 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ CUPL™ and PALASM® 90 design software packages also support the LVT22V10 architecture.

All packages allow Boolean and state equation entry formats, SNAP, ABEL and CUPL also accept, as input, schematic capture format.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

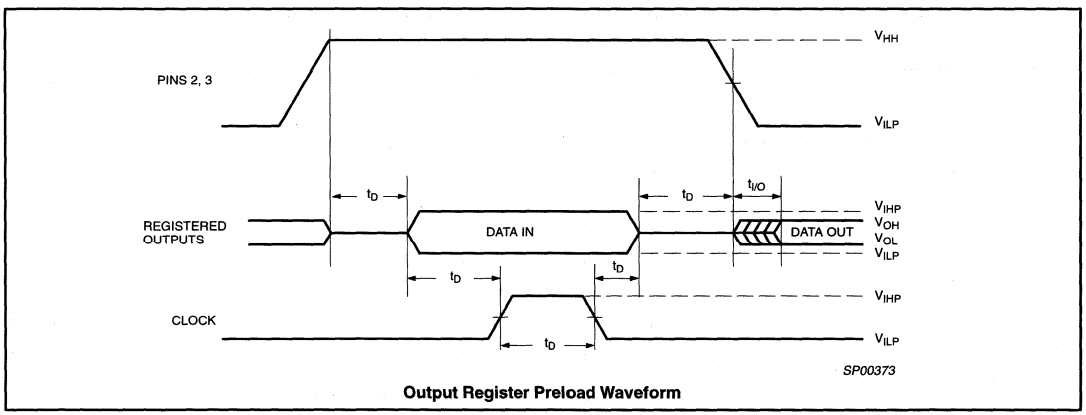
Output Register Preload

The register on the LVT22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. The procedure for preloading follows:

1. Raise V_{CC} to 3.3V ± 0.3V.
2. Set pin 2 or 3 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock Pin 1 from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower pin 2 or 3 to V_{ILP}.
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

PRELOAD SET-UP

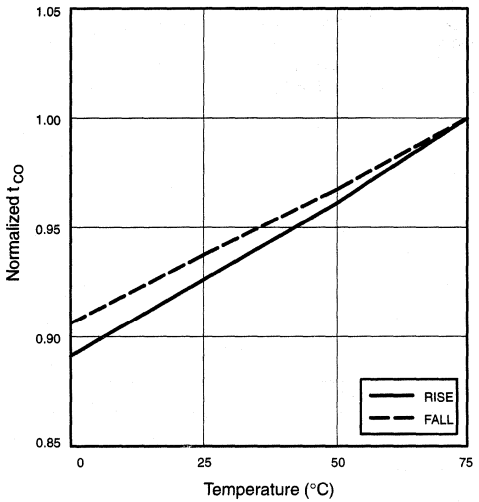
SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	REC	MAX	
V_{HH}	Super-level input voltage	9.5	9.5	10	V
V_{ILP}	Low-level input voltage	0	0	0.8	V
V_{IHP}	High-level input voltage	2.4	3.3	3.6	V
t_D	Delay time	100	200	1000	ns
$t_{I/O}$	I/O valid after Pin 2 or 3 drops from V_{HH} to V_{ILP}	100			ns



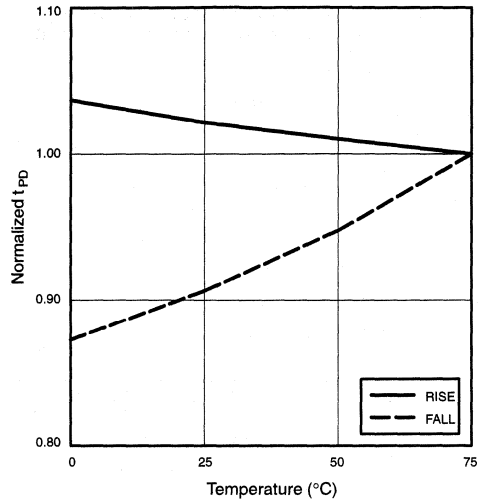
Output Register Preload Waveform

LVT22V10 TIMING CHARACTERIZATION

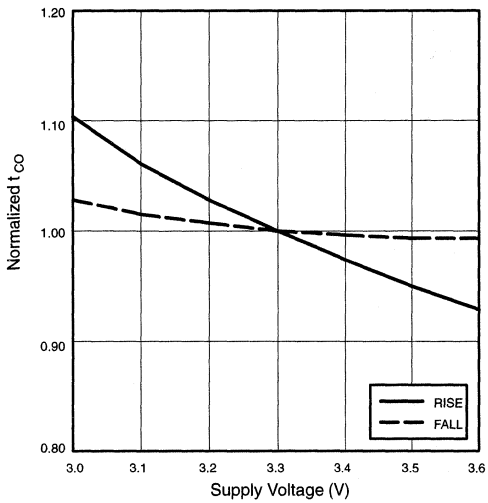
Normalized t_{CO} vs Temperature
(V_{CC} = 3.3V, output capacitance = 50pF, 5outputs switching)



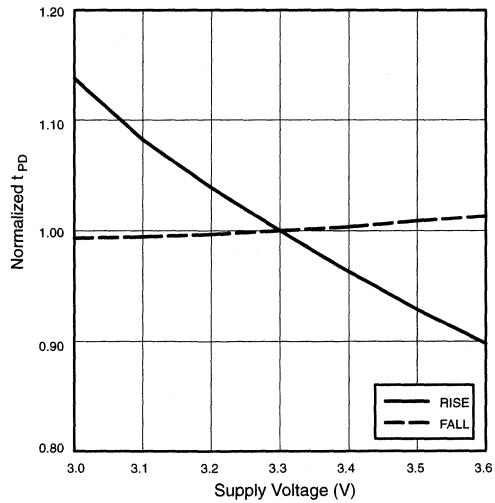
Normalized t_{PD} vs Temperature
(V_{CC} = 3.3V, output capacitance = 50pF, 5 outputs switching)



Normalized t_{CO} vs V_{CC}
(temp = 25°C, output capacitance = 50pF, 5 outputs switching)



Normalized t_{PD} vs V_{CC}
(temp = 25°C, output capacitance = 50pF, 5 outputs switching)

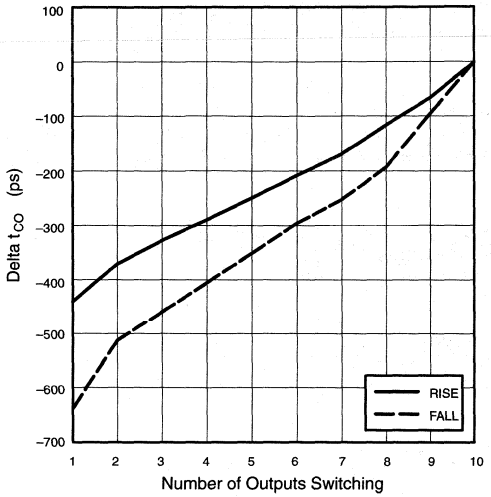


The timing characterization represents the average values of a representative sample for each parameter.
The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design.
Philips guarantees the MAX AC CHARACTERIZATION specifications.

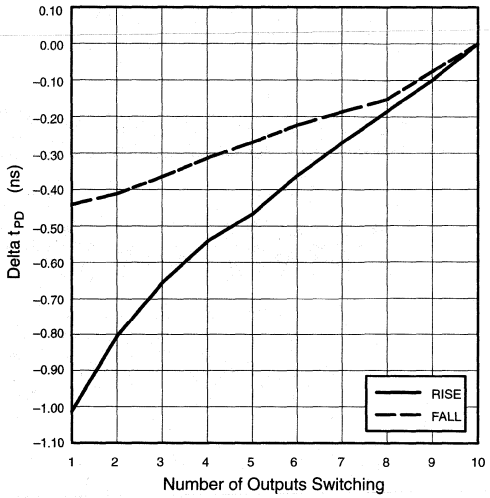
SP00386

LVT22V10 TIMING CHARACTERIZATION

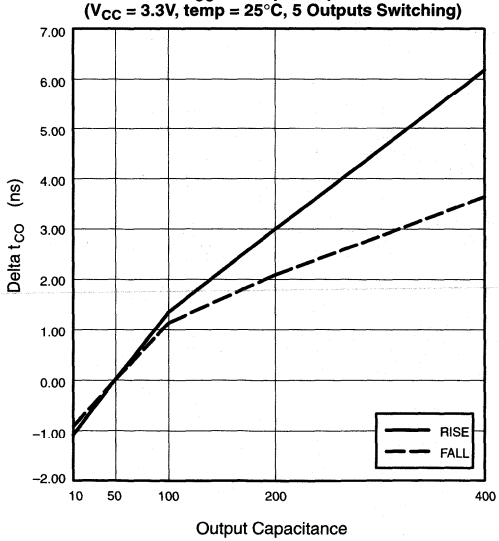
Delta t_{CO} vs Number of Outputs Switching
(V_{CC} = 3.3V, temp = 25°C, output capacitance = 50pF)



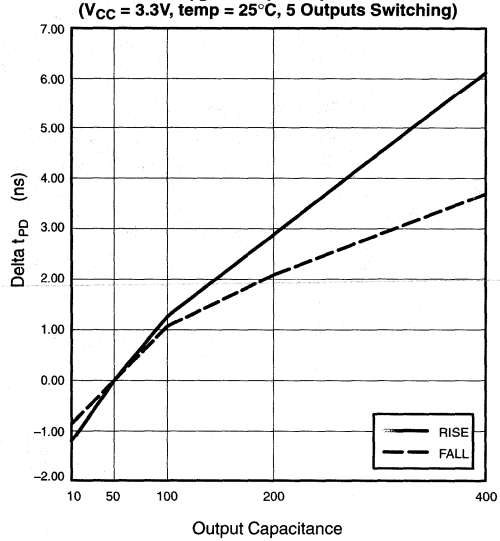
Delta t_{PD} vs Number of Outputs Switching
(V_{CC} = 3.3V, temp = 25°C, output capacitance = 50pF)



Delta t_{CO} vs Output Capacitance
(V_{CC} = 3.3V, temp = 25°C, 5 Outputs Switching)



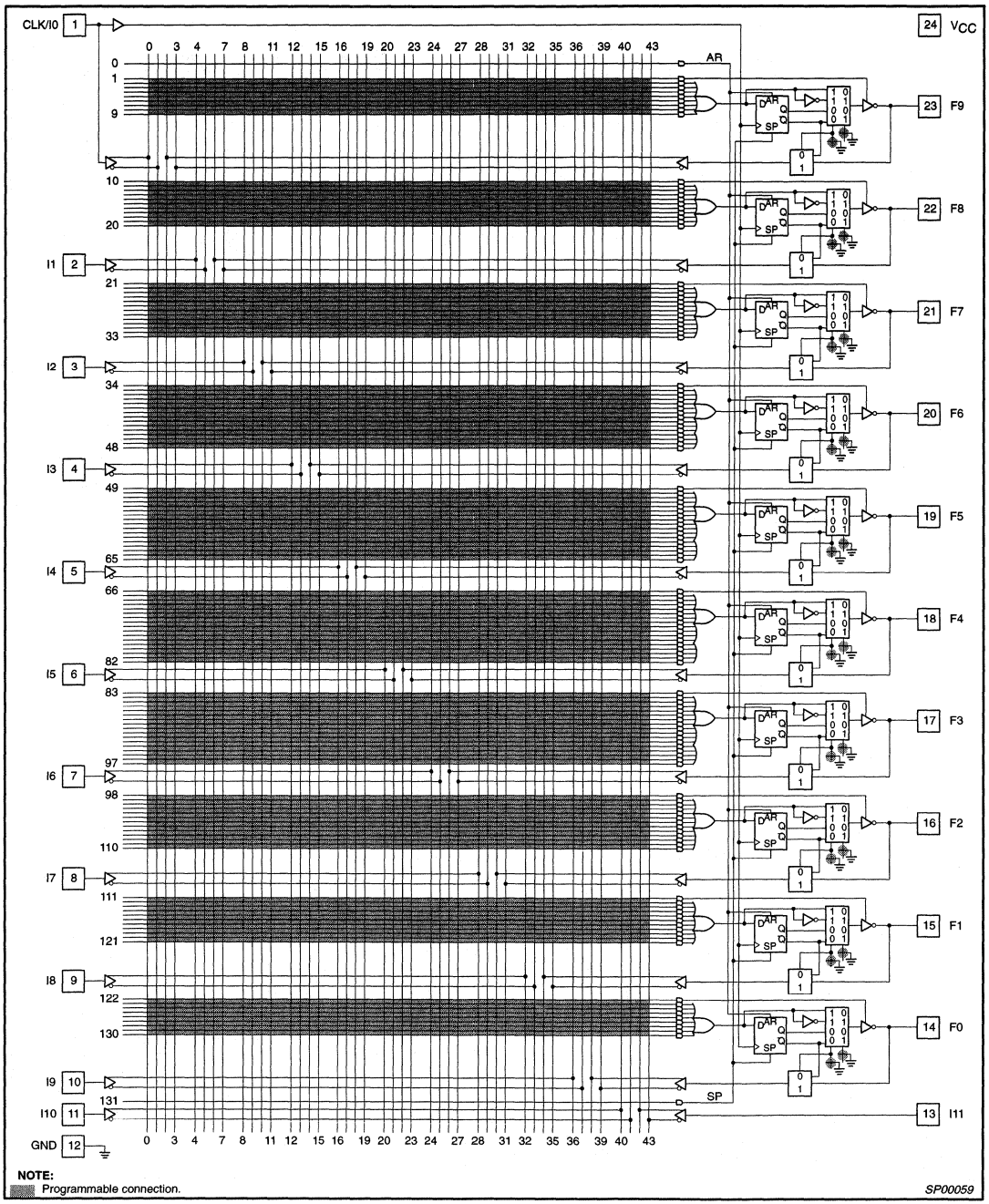
Delta t_{PD} vs Output Capacitance
(V_{CC} = 3.3V, temp = 25°C, 5 Outputs Switching)



The timing characterization represents the average values of a representative sample for each parameter.
The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design.
Philips guarantees the MAX AC CHARACTERIZATION specifications.

SP00387

LOGIC DIAGRAM



NOTE:
Programmable connection.

SP00059

FUNCTIONAL DIAGRAM

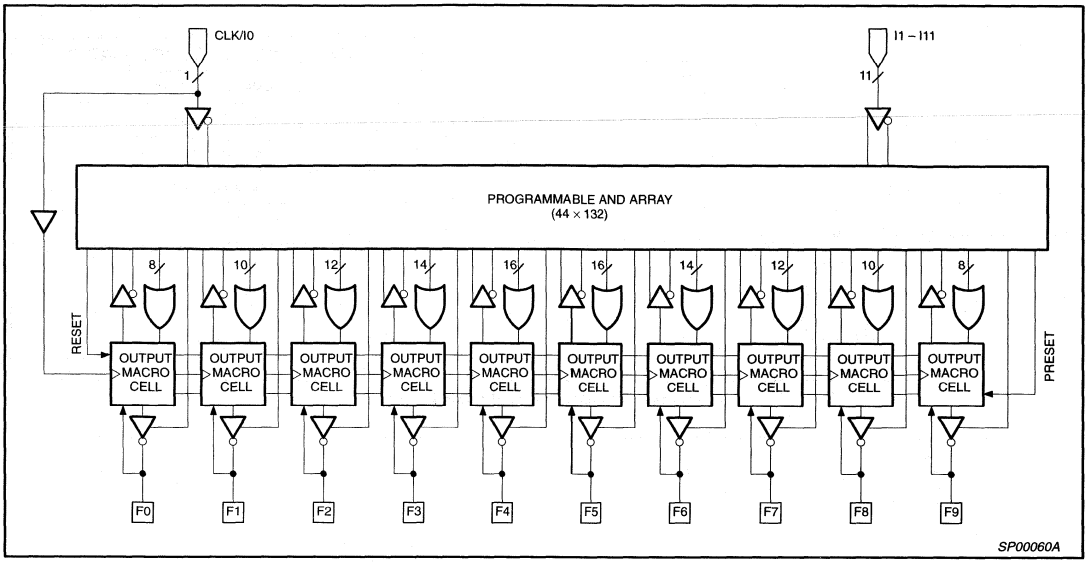


Figure 1. Functional Diagram

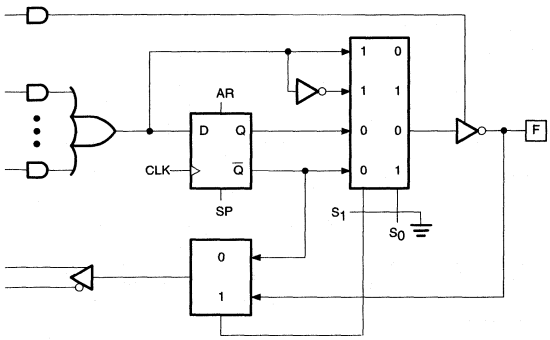
FUNCTIONAL DESCRIPTION

The LVT22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both True and Complement of any single input assume the logical LOW state.

The LVT22V10 has 12 inputs and 10 I/O Macro Cells (Figure 1). The Macro Cell allows one of four potential output configurations, registered output or combinatorial I/O, Active-HIGH or Active-LOW (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0–S_1. Multiplexer controls are connected to ground (0) through a programmable fuse link, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

OUTPUT MACRO CELL

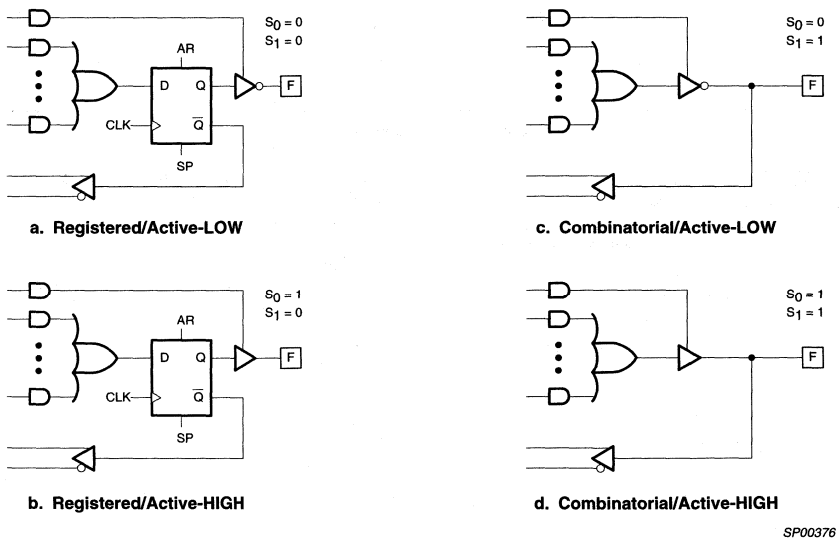


S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed fuse
1 = Programmed fuse

SP00375

Figure 2. Output Macro Cell Logic Diagram



SP00376

Figure 3. Output Macro Cell Configurations

Registered Output Configuration

Each Macro Cell of the LVT22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any Macro Cell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration, the feedback is from the pin.

Variable Input/Output Pin Ratio

The LVT22V10 has twelve dedicated input lines, and each Macro Cell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity.

INTERFACING IN MIXED 3V/5V SYSTEMS

3V Logic Driving 5V Logic

The LVT family has outputs that swing virtually between the power supply rails, thereby allowing direct interfacing with TTL switching levels.

When interfacing the outputs of any of our 3V logic ICs with standard TTL-level logic inputs (bipolar or CMOS HCT), the output levels from the 3V logic are sufficient to directly drive the 5V logic.

When driving CMOS-level devices (such as HC or AC), the output voltage from the 3V logic is insufficient to ensure reliable operation. This problem can be easily resolved by using a pull-up resistor at the interface.

5V Logic Driving 3V Logic

Since the LVT ICs do not have protection diodes between their inputs and V_{CC}, the inputs of these devices can therefore withstand higher levels than the supply voltage, and they can be directly connected to 5V CMOS logic outputs. For the LVT family, the combination of low power dissipation with the live insertion feature, bus hold and full 5V input/output capability make this logic ideal for 3.3V backplane interfacing.

INTERFACING 3 VOLT AND 5 VOLT LOGIC

	FROM	TO	METHOD
3V to 5V	LVT Output	TTL Inputs	Direct
		CMOS inputs	Pull-up
5V to 3V	CMOS Rail	LVT Input	Direct
	Totem-Pole	LVT Input	Direct
	Open Drain	LVT Input	Pull-up

LVT22V10 METASTABLE HARDENED CHARACTERISTICS

Metastable Hardened Characteristics

What is metastable hardened? Philips Semiconductors uses the term "metastable hardened" to describe a combination of two characteristic features. The first is a patented Philips circuit that prevents the outputs from glitching, oscillating, or remaining in the linear region under any circumstances, including setup and hold time violations. The second is the flip-flops' inherent ability of resolving the metastable condition. Philips provides complete data on the LVT22V10's metastable characteristics

With the LVT22V10, any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flop, the only outward manifestation of the event will be an increased clock-to-Q delay. This delay is a function of the metastability characteristics of the device, defined by τ and T_O as described below. Since the outputs never glitch, oscillate, or remain in the linear region, the only metastable failure that can propagate further into the system is when the next flip-flop in the system samples the LVT22V10's output at precisely the same time it is making a logic transition. By allowing sufficient time for any increased clock-to-Q delay, propagation of metastable failures can be avoided. The following design example illustrates this concept.

Design Example

Suppose a designer wants to use the LVT22V10 for synchronizing asynchronous data that is arriving at 2MHz (as measured by a frequency counter), in a 3.3V system that has a clock frequency of 33MHz, at an ambient temperature of 25°C. She has decided that she would like to sample the output of the LVT22V10 15ns after the clock edge to ensure that any clock-to-Q delays that were the result of the LVT22V10 internal metastability resolution circuitry have completed and the outputs have transitioned. The MTBF for this situation can be calculated by using the equation below:

$$MTBF = e(t'/\tau)/T_O F_C F_1$$

In this formula, F_C is the frequency of the clock, F_1 is the average input event frequency, and t' is the time after the clock pulse that the output is sampled ($t' > T_{CO}$). T_O and τ are device parameters provided by the semiconductor manufacturer (refer to the following table for the LVT22V10 metastability specifications). T_O and τ are derived from tests and can be most nearly be defined as follows: τ is a function of the rate at which a latch in a metastable state resolves that condition. T_O is a function of the measurement of the propensity of a latch to enter a metastable state. T_O is also a normalization constant, which is a very strong function of the normal propagation delay of the device.

In this situation the F_1 will be twice the data frequency, or 4MHz, because input events consist of both of low and high transitions. Thus, in this case, F_C is 33MHz, F_1 is 4MHz, τ is 317ps, t' is 15ns, and T_O is 4.27×10^{-3} seconds. Using the above formula the actual MTBF for this situation is 1.26×10^9 seconds or 39 years for the LVT22V10.

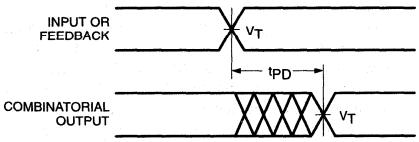
Summary

The Philips LVT22V10 has on-chip circuitry that completely eliminates any output glitches, oscillations, or other output anomalies associated with metastable conditions. For outputs that are then used to generate clocks, control signals or other asynchronous data this represents an unparalleled level of reliability in a PLD. In addition, a complete set of metastability data is provided, that allows designers the ability to design robust systems where data is synchronously pipelined.

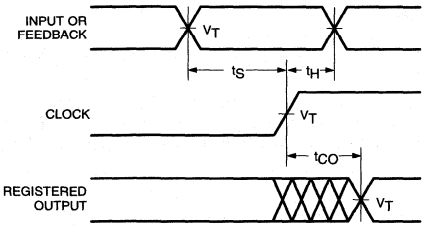
LVT22V10 VALUES FOR τ AND T_O

V_{CC}	0°C		25°C		75°C	
	τ	T_O	τ	T_O	τ	T_O
3.0V	829.00ps	1.16E–08	691.00ps	1.09E–07	429.00ps	2.27E–04
3.3V	358.00ps	2.36E–04	317.00ps	4.27E–03	329.00ps	5.75E–03
3.6V	237.00ps	2.66E–01	230.00ps	6.47E–01	250.00ps	1.13E+00

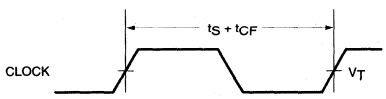
SWITCHING WAVEFORMS



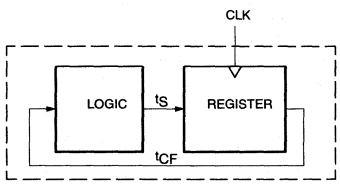
Combinatorial Output



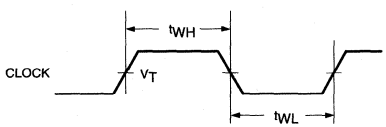
Registered Output



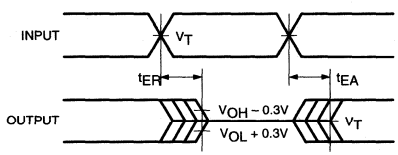
Clock to Feedback (f_{MAX} Internal)
(See Path at Right)



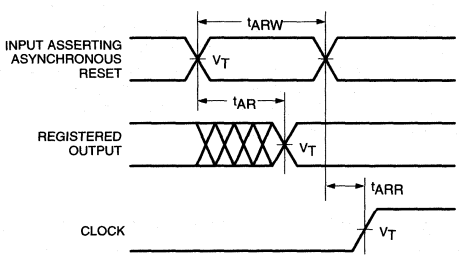
Clock to Feedback



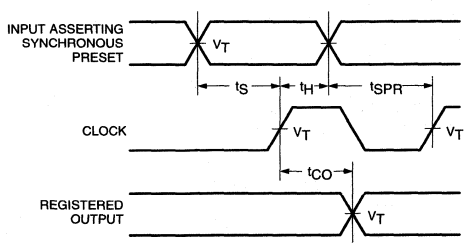
Clock Width



Input to Output Disable/Enable



Asynchronous Reset

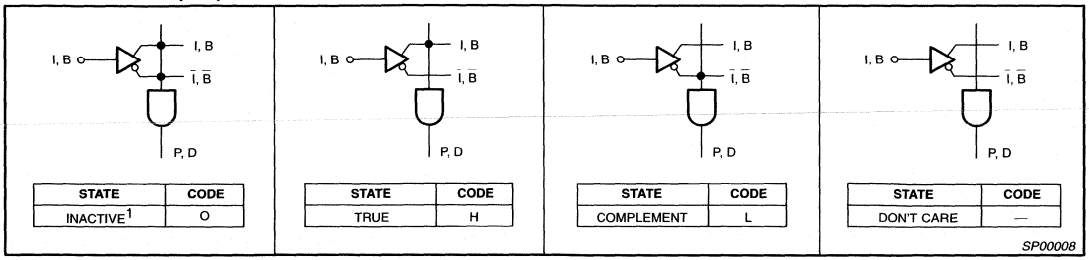


Synchronous Preset

SP00388

NOTES:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 1.5ns max.

"AND" ARRAY – (I, B)

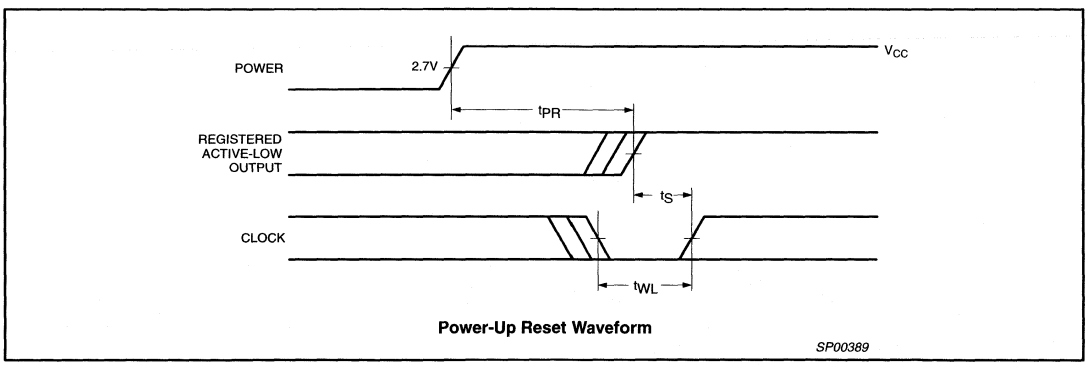


NOTE:
1. This is the initial state.

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.



Power-Up Reset Waveform

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{PR}	Power-up Reset Time		1	µs
t_S	Input or Feedback Setup Time	See AC Electrical Characteristics		
t_{WL}	Clock Width LOW			

Section 7
Package Information

BiCMOS Bus Interface Logic

CONTENTS

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when though-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1. Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260°C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24V) to the lead(s) of the package, below the seating plane or not more than 2mm above it. If the temperature of the soldering iron bit is less than 300°C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400°C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2. Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be indluenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapor phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250°C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45°C.

Table 3. Suitability of surface mounted packages for various soldering methods

Rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder theives at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at and angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, only consider wave soldering for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4mm**, *e.g.*, SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2 and SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260°C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150°C within 6 seconds. Typical dwell time is 4 seconds at 250°C.

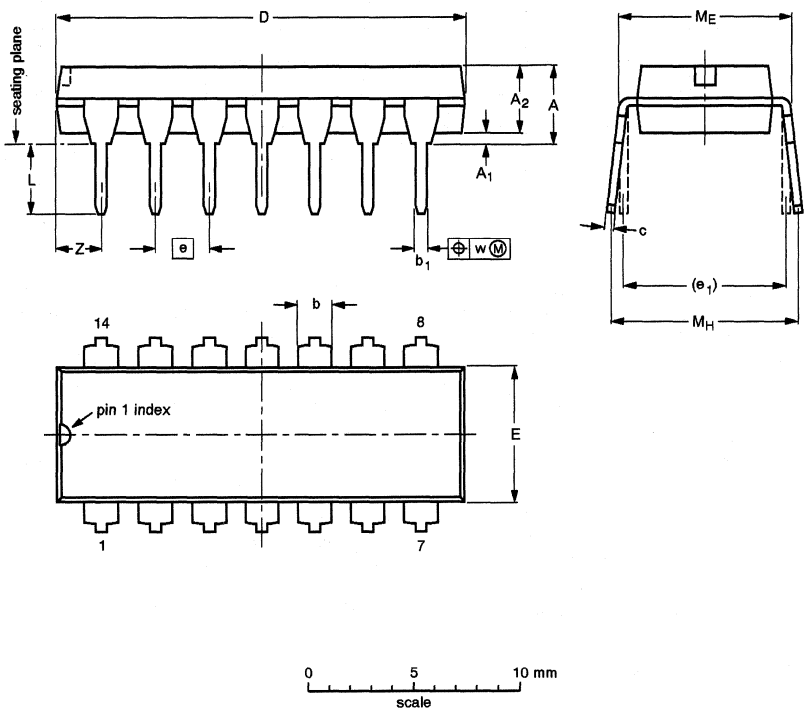
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320°C.

Package outlines

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

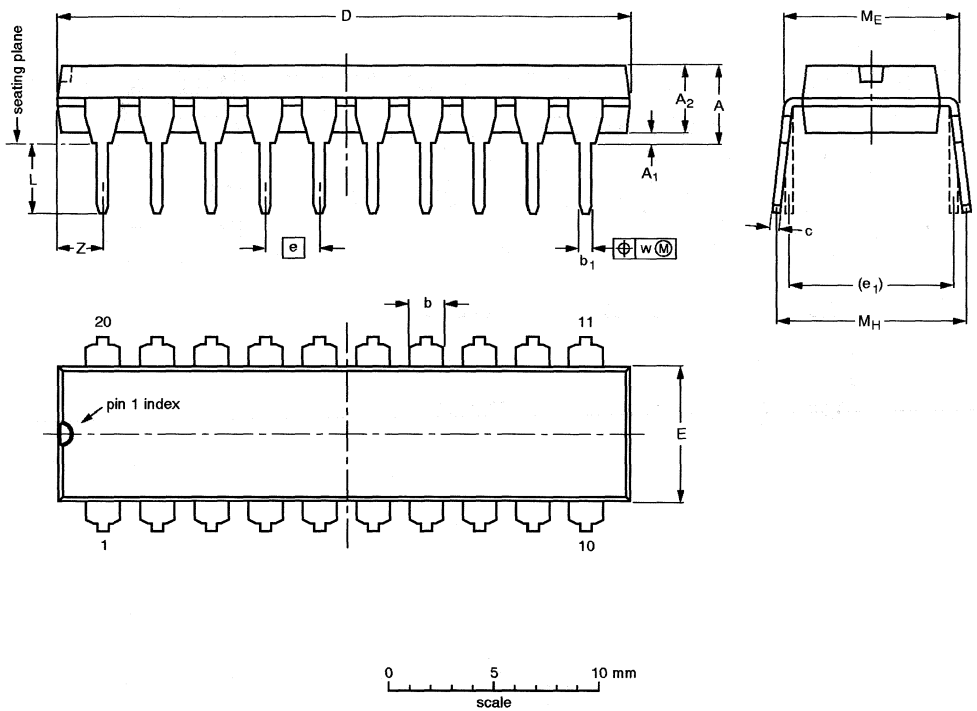
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

Package outlines

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

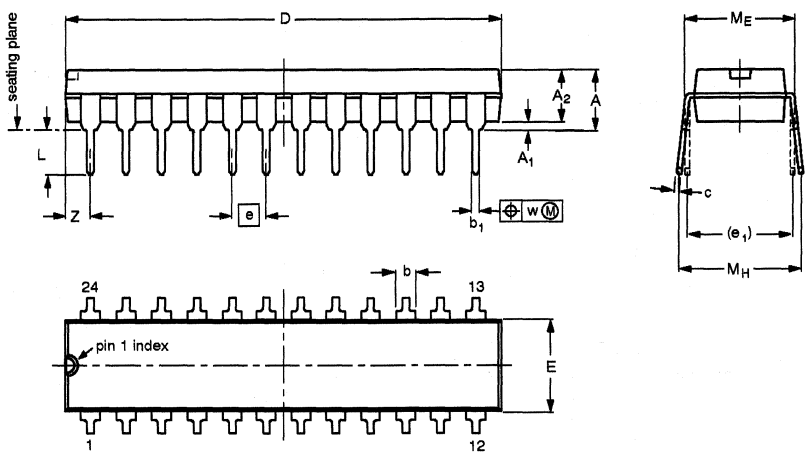
Note

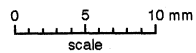
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

Package outlines

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

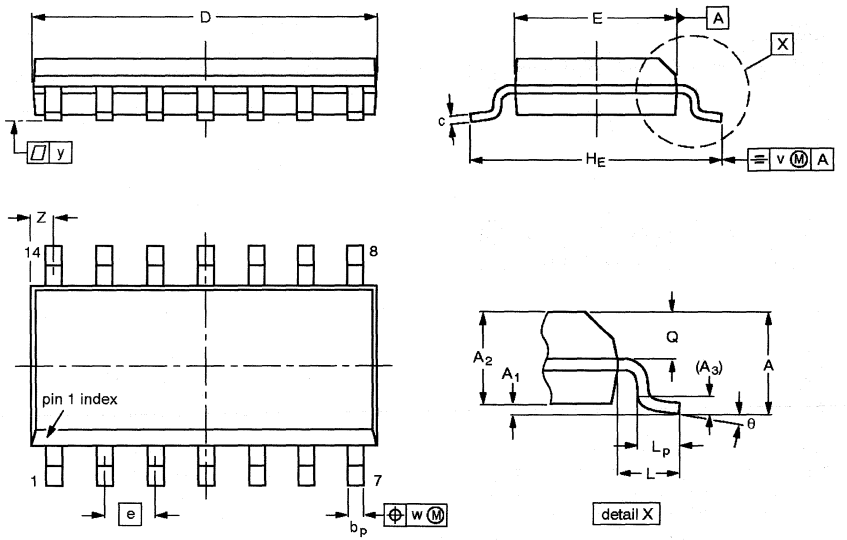
Note

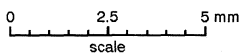
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

Package outlines

SO14: plastic small outline package; 14 leads; body width 3.9 mm — SOT108-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

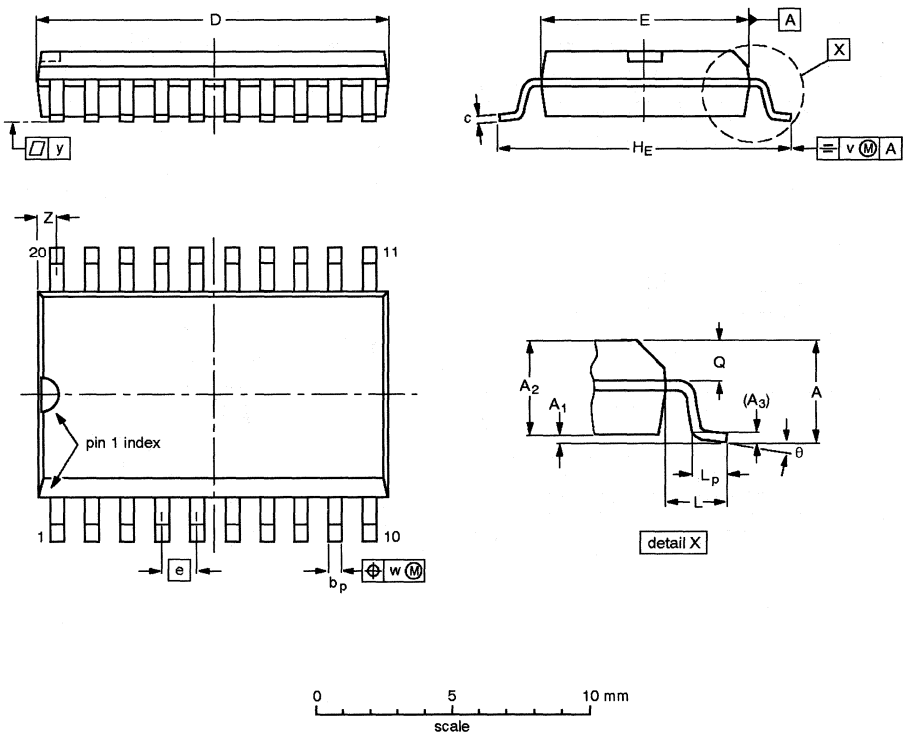
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

Package outlines

SO20: plastic small outline package; 20 leads; body width 7.5 mm — SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

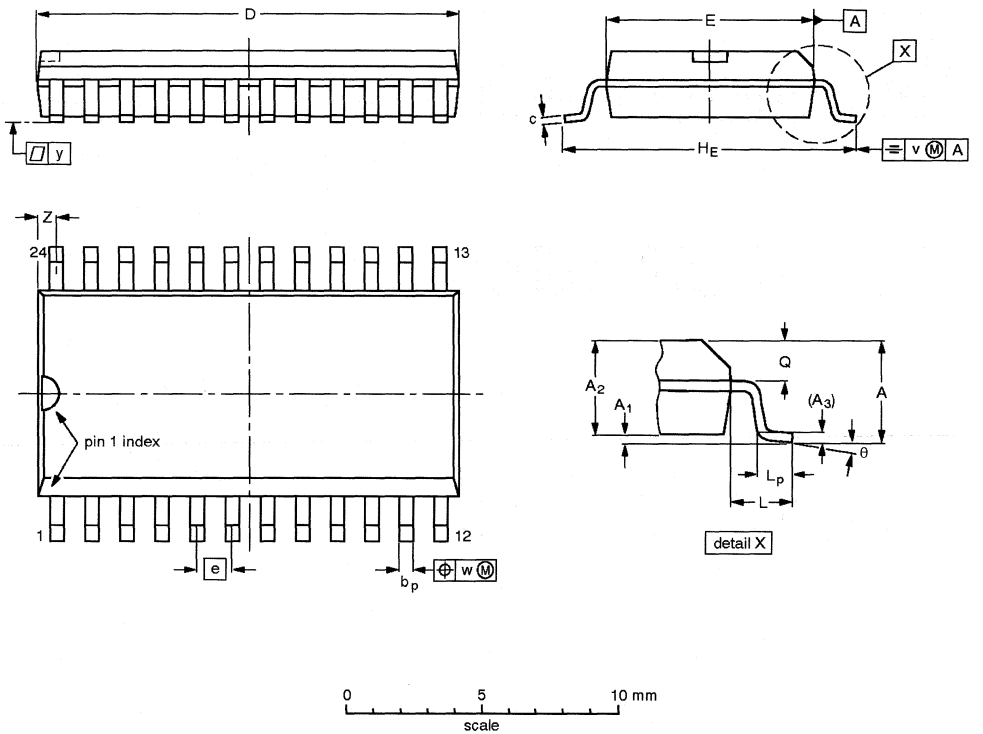
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

Package outlines

SO24: plastic small outline package; 24 leads; body width 7.5 mm — SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

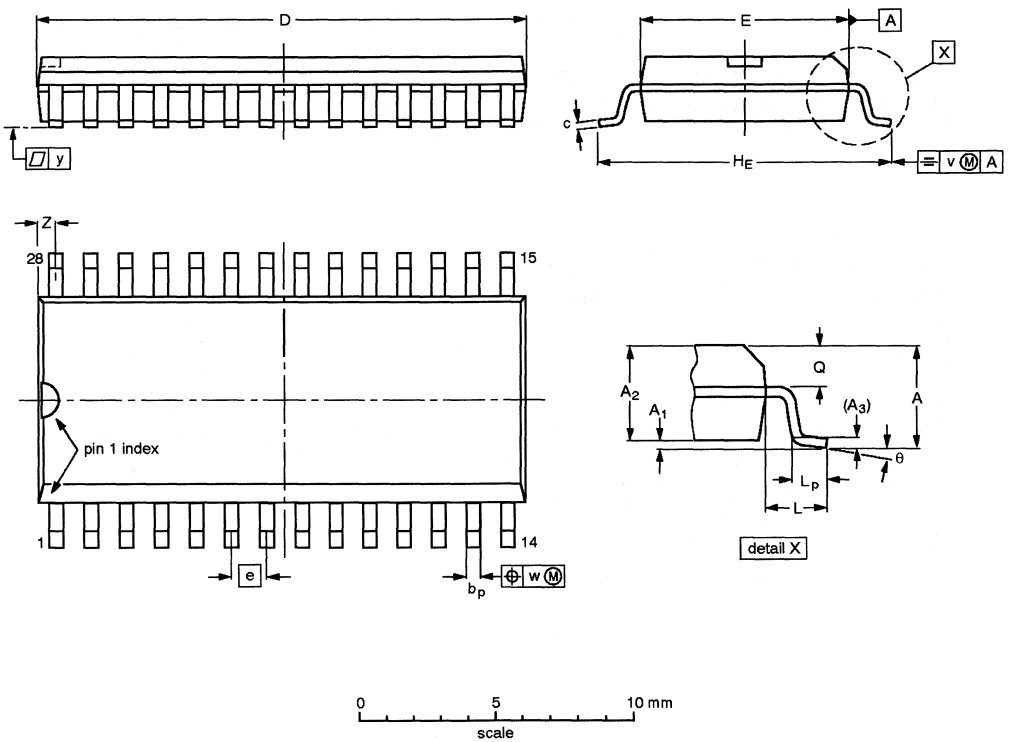
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

Package outlines

SO28: plastic small outline package; 28 leads; body width 7.5mm — SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

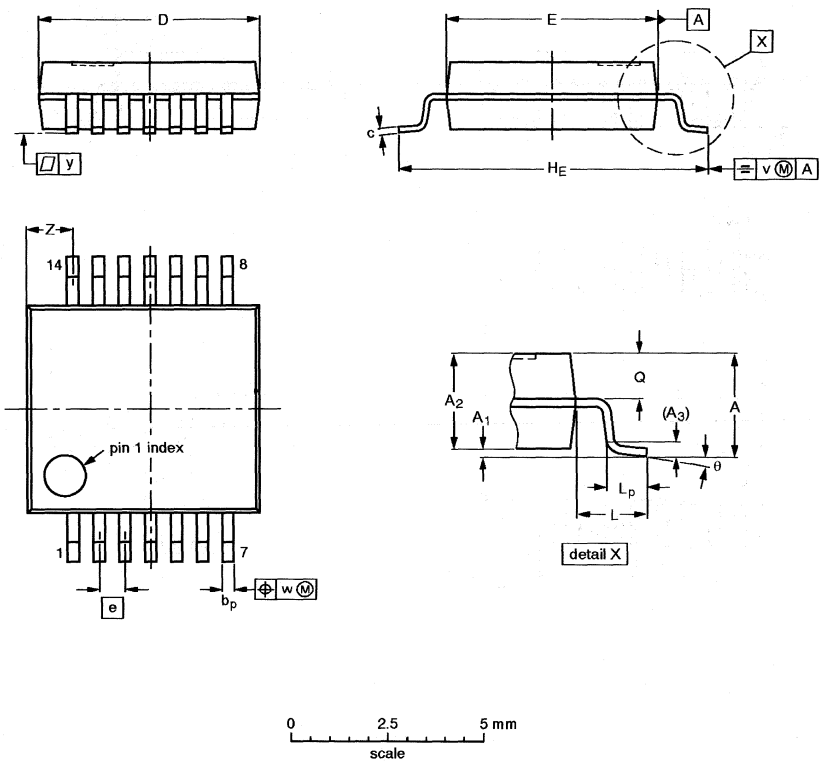
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

Package outlines

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm — SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

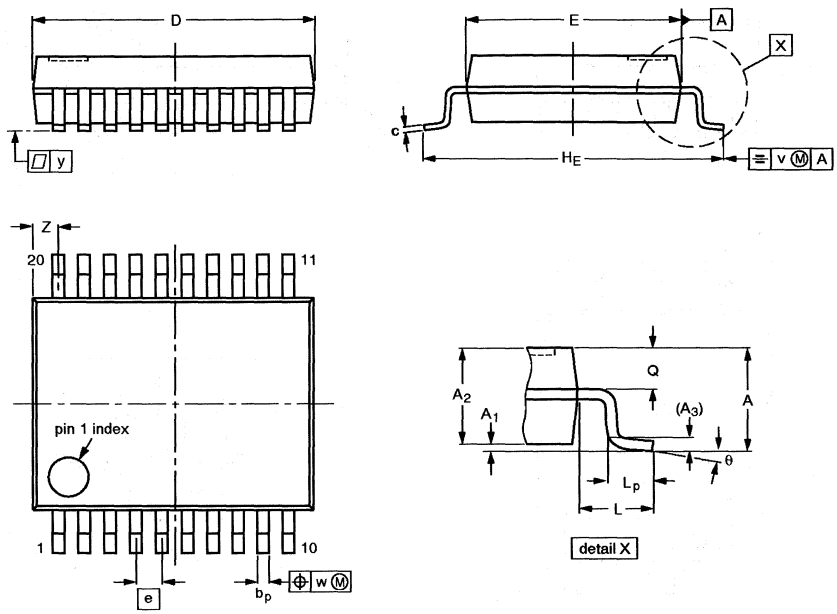
Note

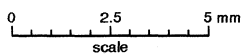
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-18

Package outlines

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm — SOT339-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

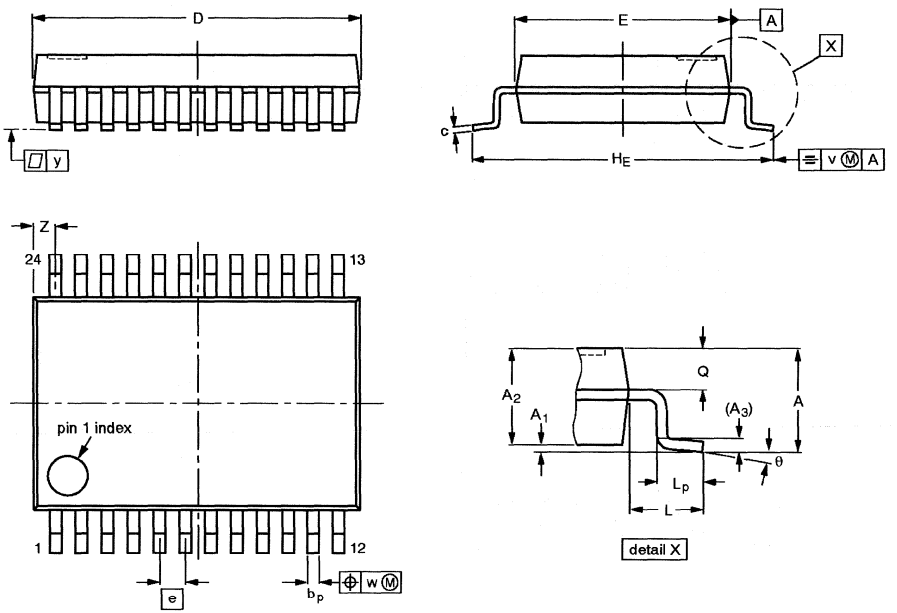
Note

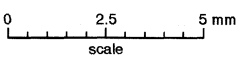
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

Package outlines

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm — SOT340-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

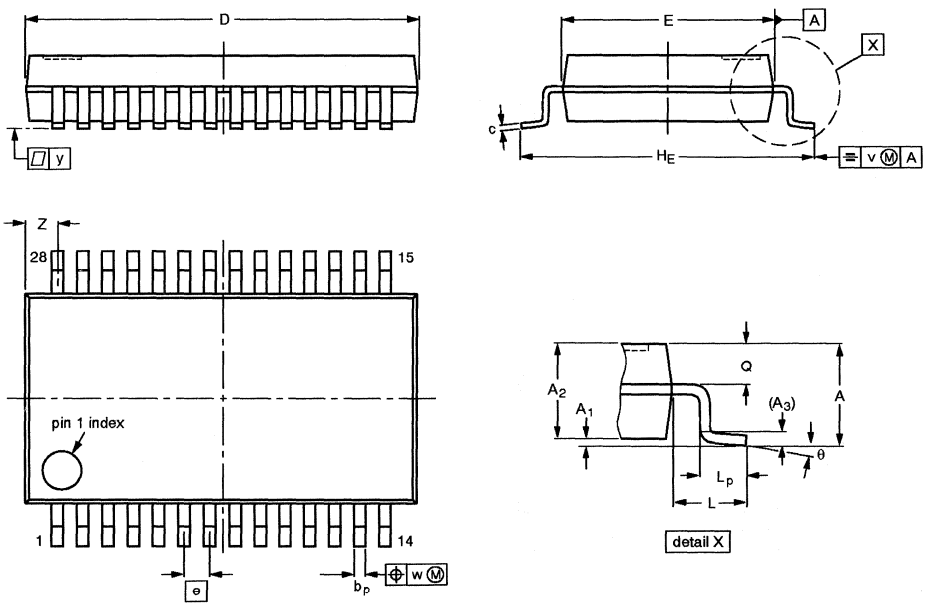
Note

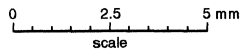
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

Package outlines

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3mm — SOT341-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

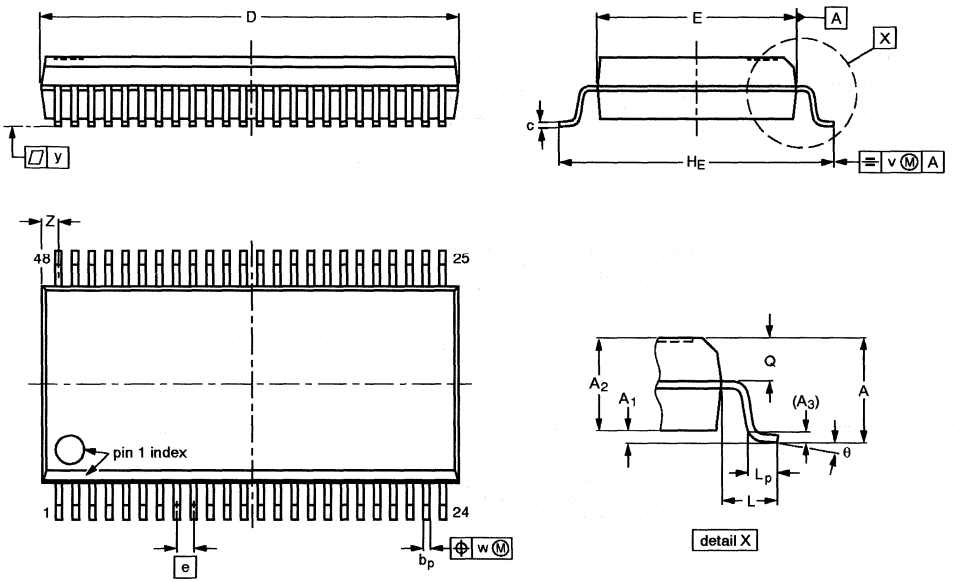
Note

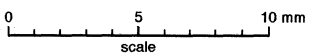
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

Package outlines

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm — SOT370-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

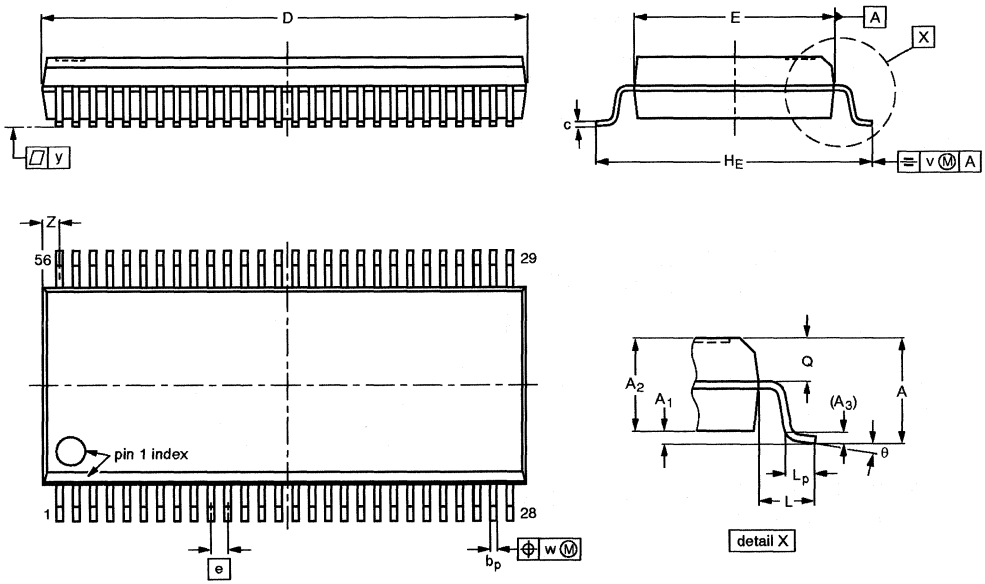
Note

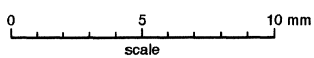
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

Package outlines

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm — SOT371-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

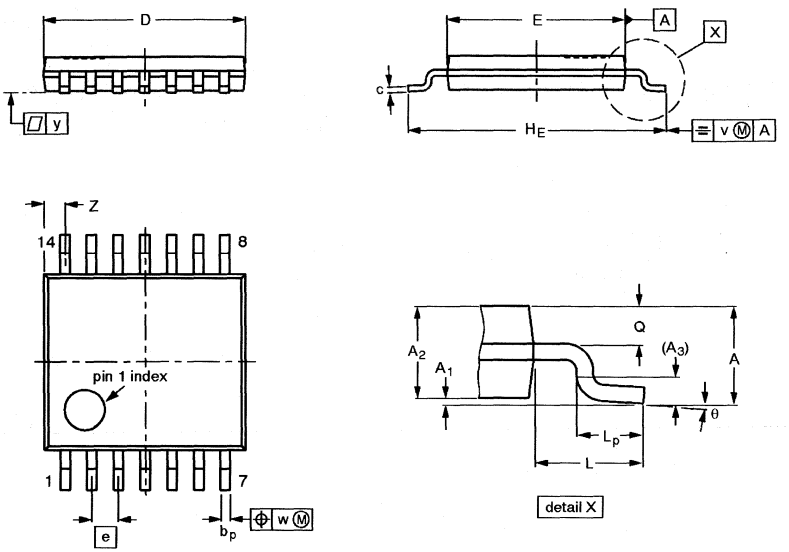
Note

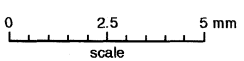
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

Package outlines

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm SOT402-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

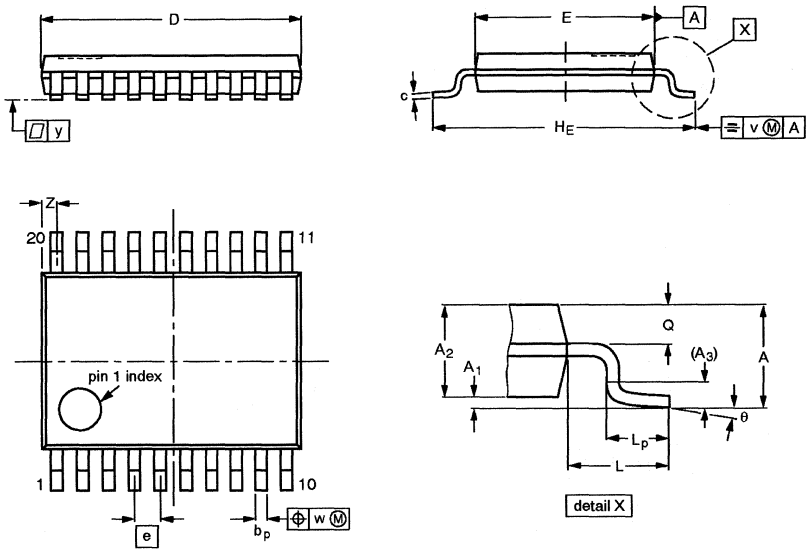
Notes

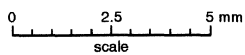
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

Package outlines

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm — SOT360-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

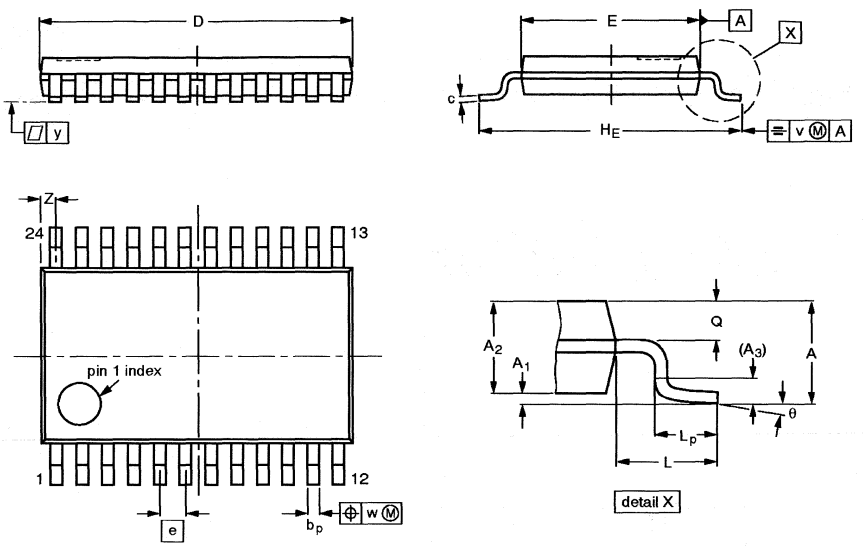
Notes

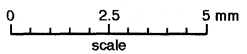
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

Package outlines

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm — SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

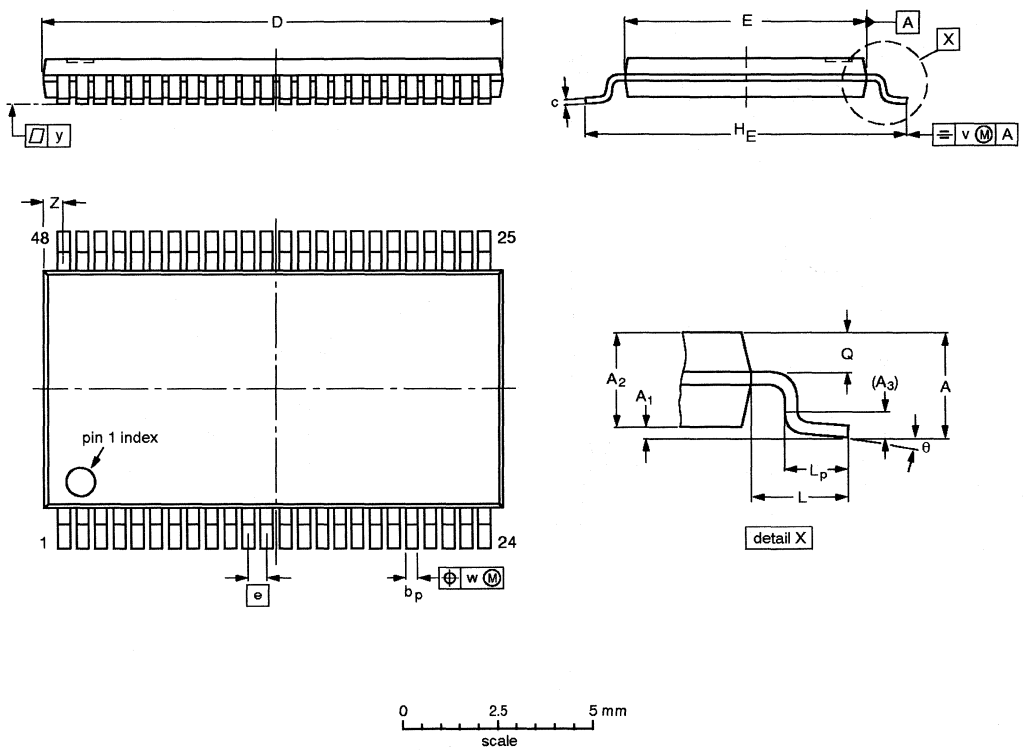
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

Package outlines

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

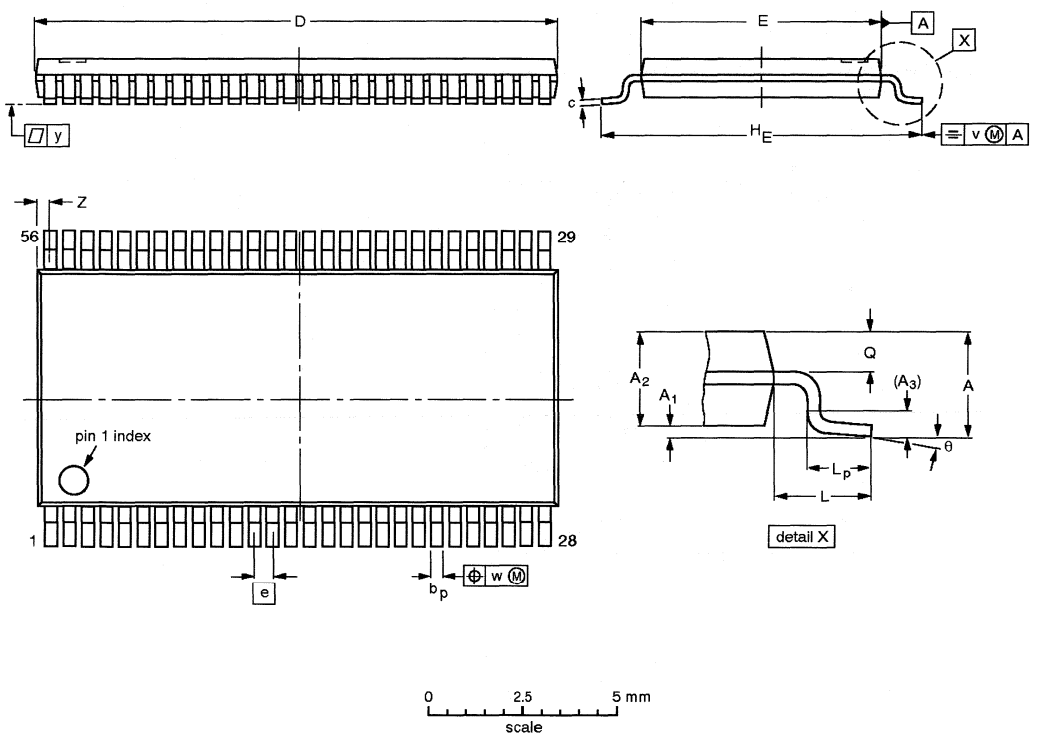
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

Package outlines

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm — SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

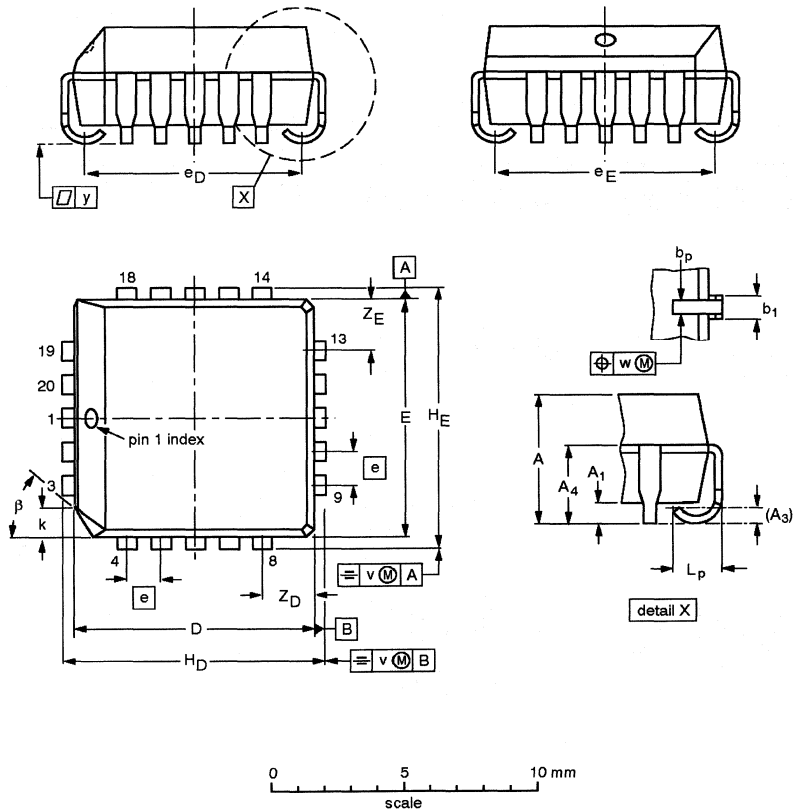
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153EE					~~93-02-03~~ 95-02-10

Package outlines

PLCC20: plastic leaded chip carrier; 20 leads — SOT380-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	9.04 8.89	9.04 8.89	1.27	8.38 7.37	8.38 7.37	10.03 9.78	10.03 9.78	1.22 1.07	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.356 0.350	0.356 0.350	0.05	0.330 0.290	0.330 0.290	0.395 0.385	0.395 0.385	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

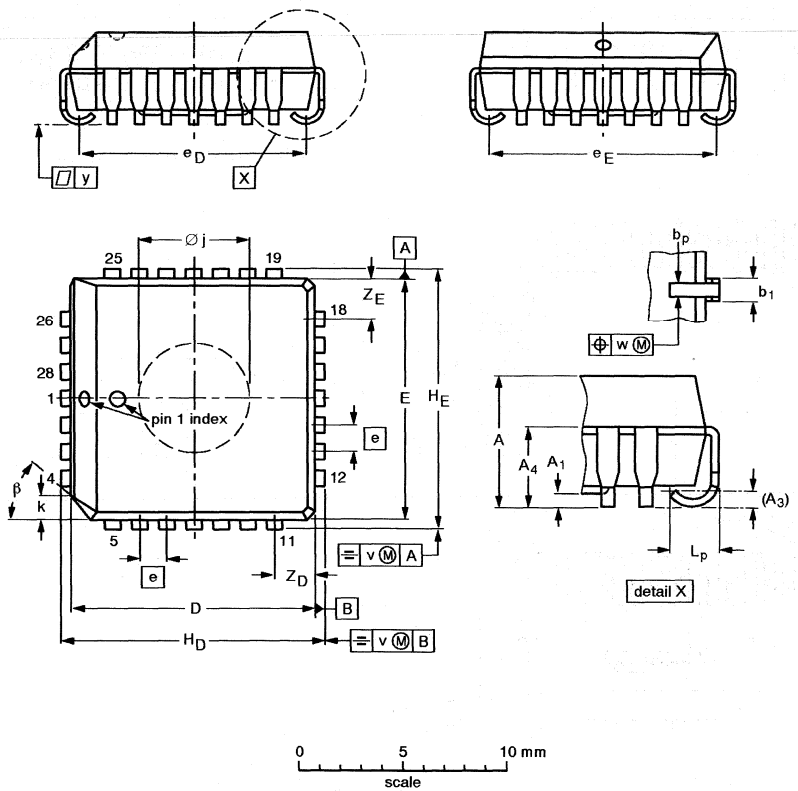
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT380-1		MO-047AA				~~95-02-25~~ 97-12-16

Package outlines

PLCC28: plastic leaded chip carrer; 28 leads; pedestal — SOT261-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

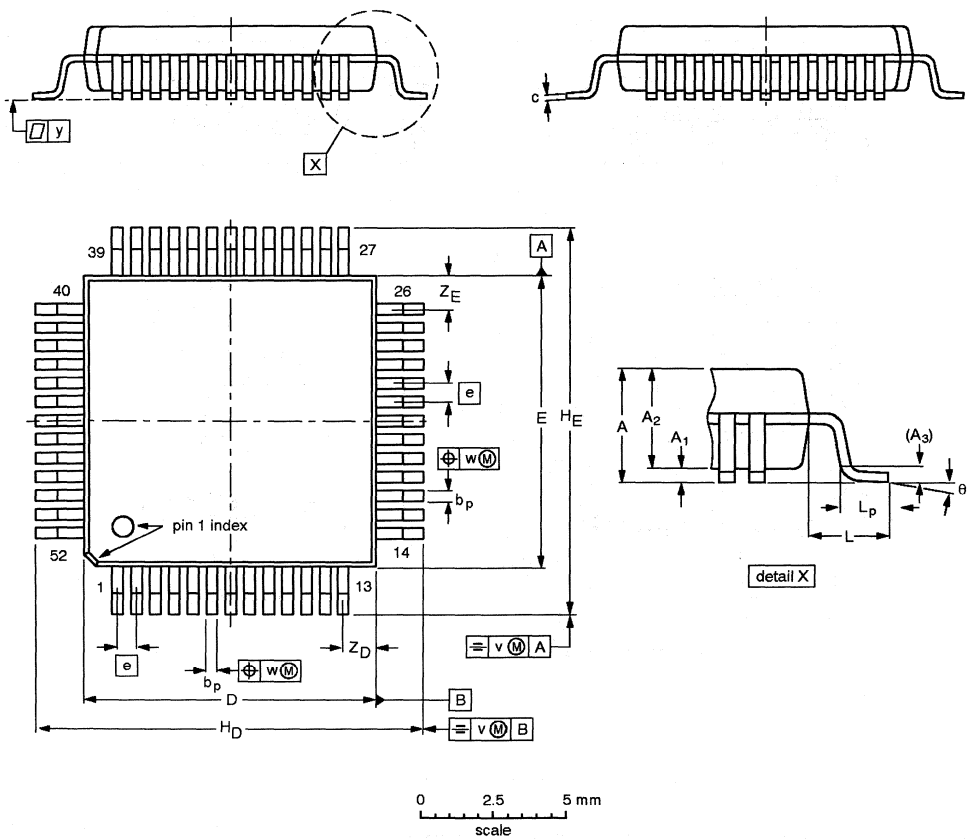
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-3		MO-047AB				~~95-02-25~~ 97-12-16

Package outlines

QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm SOT379-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.60	0.95 0.65	0.20	0.12	0.10	1.24 0.95	1.24 0.95	7° 0°

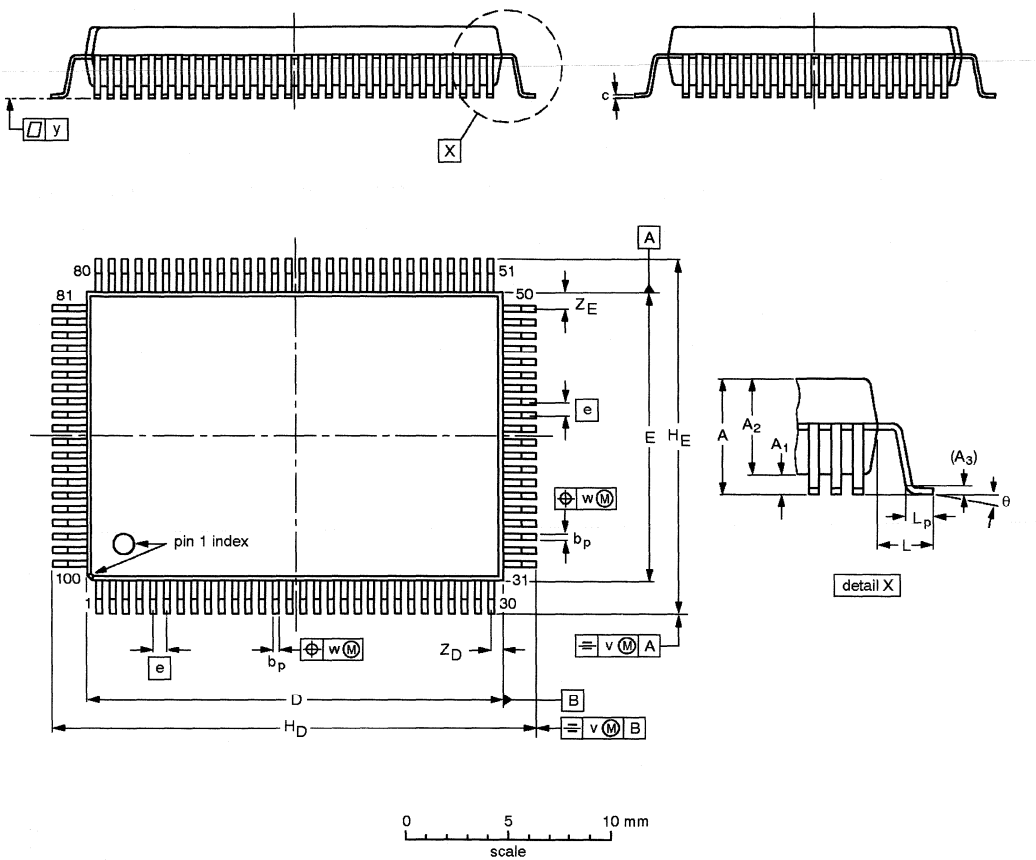
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT379-1		MO-108				~~95-02-04~~ 97-08-04

Package outlines

QFP100: plastic quad flat package; 100 leads (lead length 1.6 mm); body 14 x 20 x 2.8 mm SOT382-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.40	0.60 0.25	3.05 2.55	0.25	0.38 0.22	0.23 0.13	20.1 19.1	14.1 13.9	0.65	23.45 22.95	17.45 16.95	1.60	1.03 0.73	0.20	0.12	0.10	0.68 0.45	0.68 0.45	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT382-1		MO-108CC-1				~~95-02-04~~ 97-08-04

APPENDIX A

DATA HANDBOOK SYSTEM

Data handbook system — Appendix A

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

Our data handbook titles are listed here.

Integrated Circuits

Book	*Title*
IC01	Semiconductors for Radio, Audio and CD/DVD Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Wired Telecom Systems
IC04	HE4000B Logic Family CMOS
IC05	Advanced Low-power Schottky (ALS) Logic
IC06	High-speed CMOS Logic Family
IC11	General-purpose/Linear ICs
IC12	I^2C Peripherals
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IC15	FAST TTL Logic Series
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IC17	Semiconductors for Wireless Communications
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IC19	ICs for Data Communications
IC20	80C51-based 8-bit Microcontrollers
IC22	Multimedia ICs
IC23	BiCMOS Bus Interface Logic
IC24	Low Voltage CMOS & BiCMOS Logic
IC25	16-bit 80C51XA Microcontrollers (eXtended Architecture)
IC26	Integrated Circuit Packages
IC27	Complex Programmable Logic Devices

Discrete Semiconductors

Book	*Title*
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SC02	Power Diodes
SC03	Power Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Video Transistors and Modules for Monitors
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC13a	Power MOS Transistors including TOPFETs and IGBTs
SC13b	Small-signal and Medium-power MOS Transistors
SC14	RF Wideband Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors
SC18	Discrete Semiconductor Packages
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DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC04	Colour Monitor and Multimedia Tubes
DC05	Wire Wound Components

Magnetic Products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

Passive Components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA06a	Surface Mounted Ceramic Multilayer Capacitors
PA06b	Leaded Ceramic Capacitors
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PA10	Quartz Crystals
PA11	Quartz Oscillators

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